A New Transverse and Longitudinal Bunch by Bunch Feedback Processor

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Abstract and Context

Abstract We describe the development of firmware to support Longitudinal Bunch by Bunch Feedback at Diamond Light source. As well as feedback, the system supports complex experiments and the capture of detailed electron beam diagnostics. In this paper we describe the firmware development and some details of the processing chain. We focus on some of the challenges of FPGA development from the perspective of a software engineer.

We are transitioning from Libera Bunch-by-Bunch platform (based on 15 year old Virtex-II Pro FPGA) to MicroTCA, which provides access to more up to date hardware.

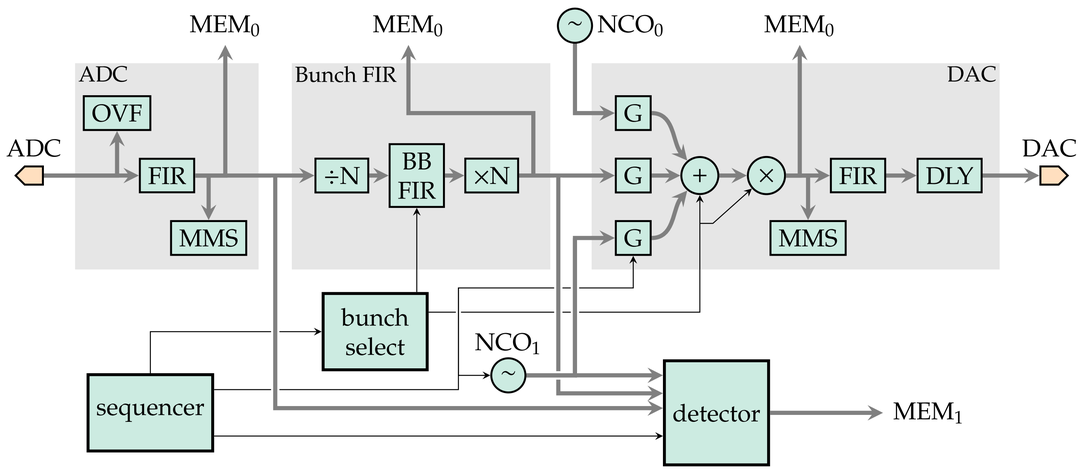
New Hardware Platform

Here we see the chosen hardware platform, with a 500 MSPS ADC/DAC FMC card at top right, and a Virtex-7 690 FPGA under the heatsink at bottom left.

FMC-500M High Pin Count FMC providing dual channel 500 MS/s 14-bit ADC and dual channel 1230 MS/s 16-bit DAC. This will support bunch-by-bunch operation at our machine RF frequency of 500 MHz.

AMC525 Double width AMC card with two HPC FMC slots, 2 GB of fast on board DRAM and 128 MB of slower DRAM connected to a Virtex-7 690 FPGA, supporting an 8 lane gen3 PCIe connection over the MicroTCA backplane. This is where all the FPGA firmware will run, and the fast backplane connection will allow us to do a lot of data processing in the associated CPU.

Data Processing Paths through Bunch-by-Bunch Processor

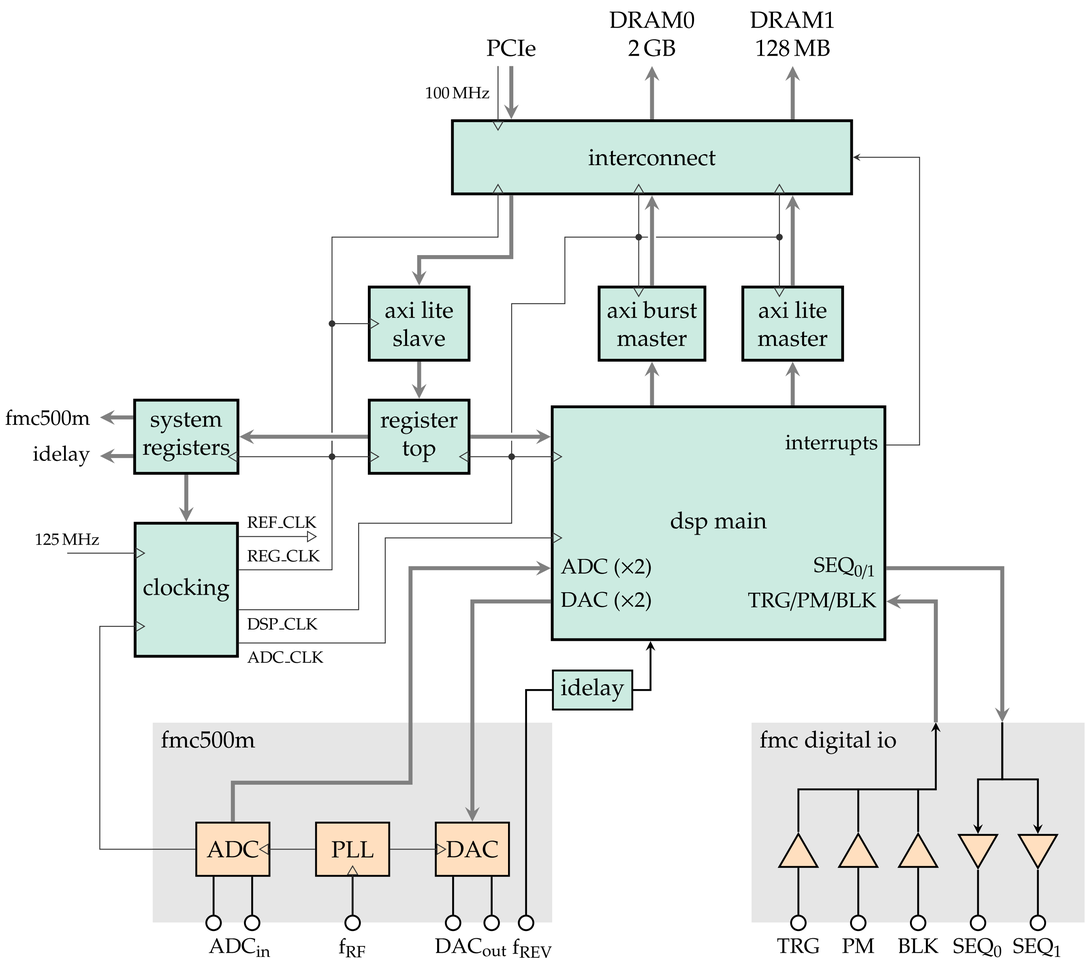


This figure shows the data processing for a single LMBF/TMBF channel:

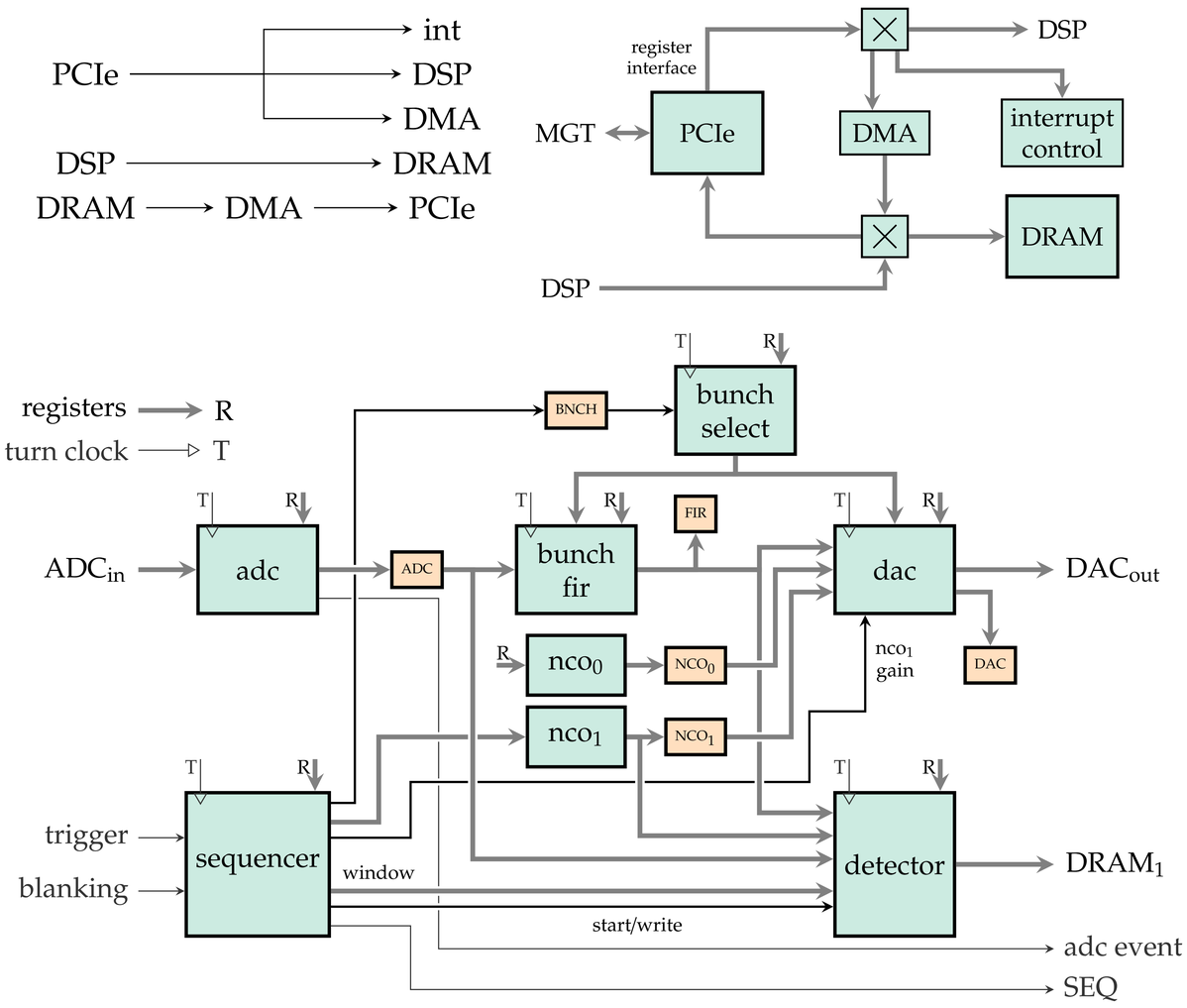
- OVF — ADC input overflow detection (programmable threshold)
- FIR — I/O compensation filter (8 tap FIR)
- MMS — bunch position and motion measurement, measures min/max/sum and sum of squares
- ÷N — bunch by bunch decimation (average over programmable count)
- BB FIR — bunch by bunch filter (8 tap FIR per bunch)
- ×N — bunch by bunch interpolation
- G — gain control (scale by power of 2)
- DLY — output alignment delay
- ~ — controllable oscillator (NCO)

Overflow detection and saturation is implemented at each point where overflow can occur.

Overview of Implementation



Overview of top level FPGA design.
The "interconnect" at the top connects to all of the hardware resources provided by the AMC525 carrier card, including 8-lane PCIe and 2 GB of fast DRAM. The rest of the this figure shows connections to the FMC cards, clocking and control, and the data processing core "dsp main".



Overview of data processing implementation for a single channel.
The symbol ADC represents points were data is interchanged with the other channel depending on whether TMBF or LMBF mode has been selected.

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