OPTIMISATION OF A LOW-NOISE 1.3 GHz PLL FREQUENCY SYNTHESIZER FOR THE EUROPEAN XFEL

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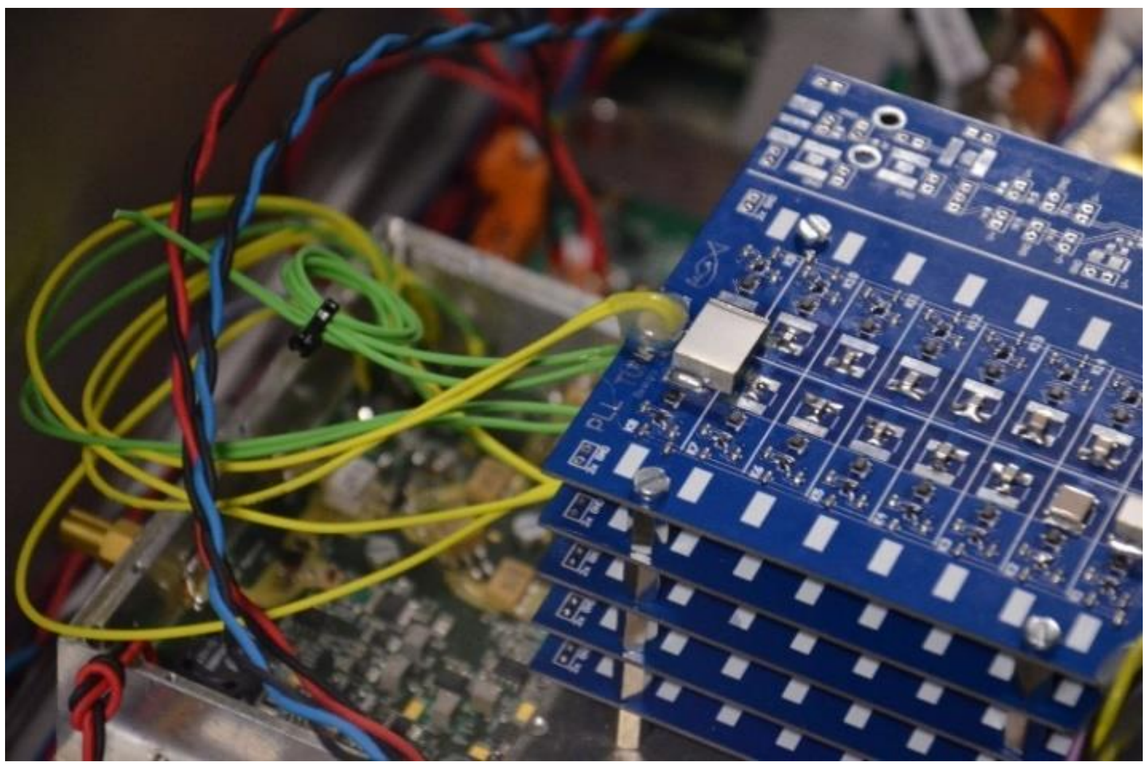
ABSTRACT

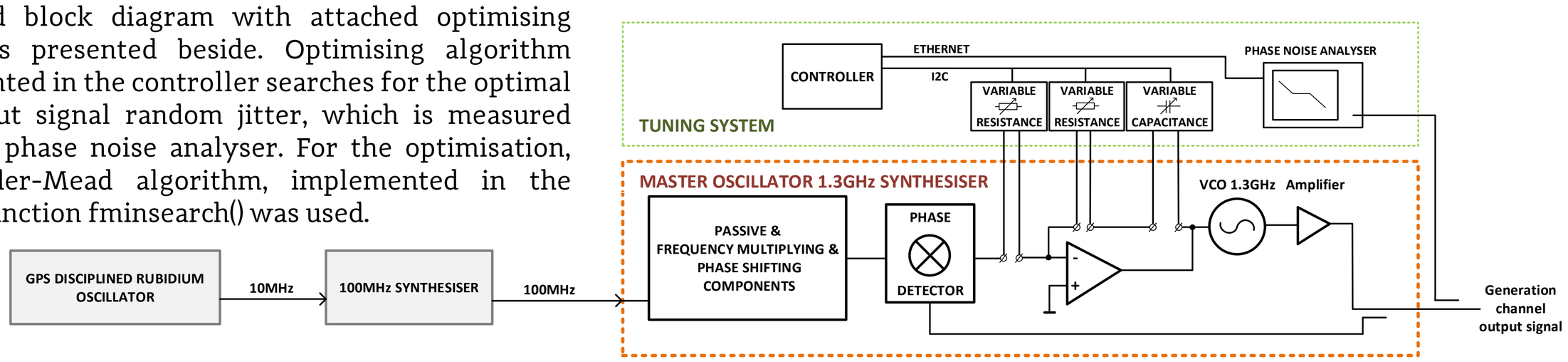
The Master Oscillator system of the European XFEL was built using frequency synthesis techniques that were found to have the best phase noise performance. This includes low noise frequency multipliers and non-multiplying phase lock loops, incorporated in the system to shape its output phase noise spectrum. Jitter of the output signal strongly depends on phase noise transmittance of the PLL and suboptimal design can worsen it by orders of magnitude. Taking into consideration that the PLL open loop transmittance usually can be shaped in multiple ways, and that the accurate phase noise measurements can easily take more than 30 minutes, designing an automated tool becomes a necessity. For this purpose an approach to the tuning system construction was chosen in order to make the phase noise optimisation process simpler. This paper describes the optimisation of PLL synthesizer phase noise, done to improve the performance of the European XFEL MO. We present the phase noise optimisation process and achieved results.

TUNERS ATTACHED TO THE PLL



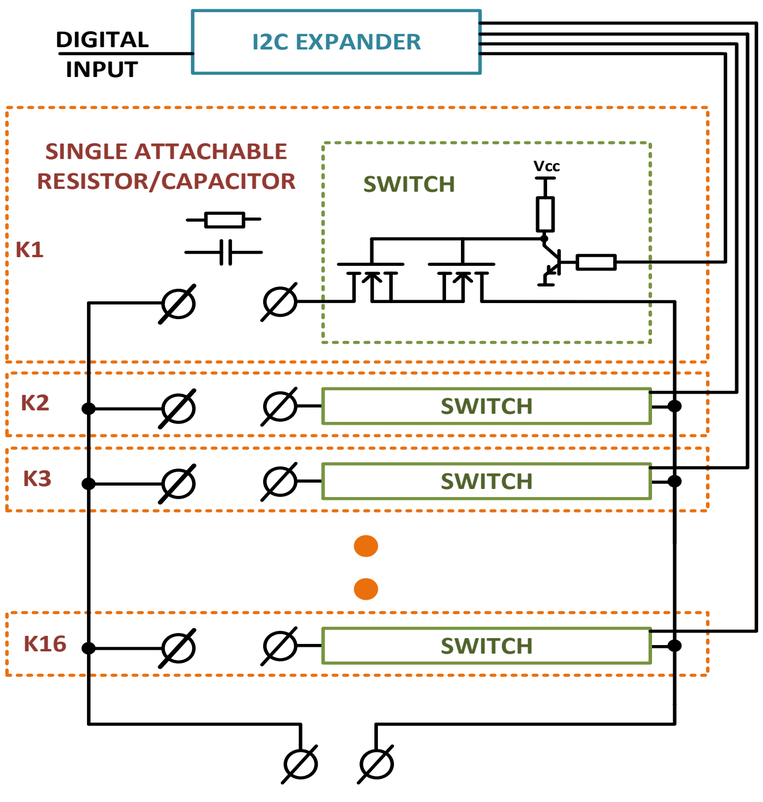
OPTIMISING SYSTEM BLOCK DIAGRAM

The Master Oscillator 1.3GHz Synthesiser simplified block diagram with attached optimising system is presented beside. Optimising algorithm implemented in the controller searches for the optimal PLL output signal random jitter, which is measured with the phase noise analyser. For the optimisation, the Nelder-Mead algorithm, implemented in the Matlab function fminsearch() was used.



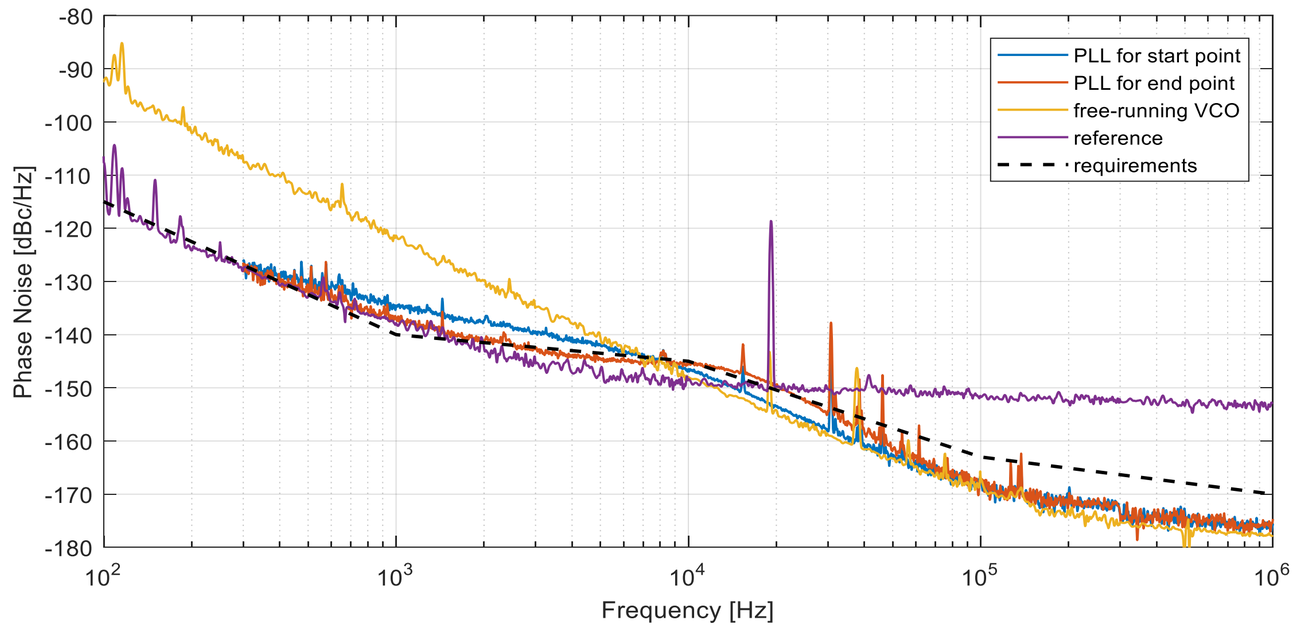
PLL TUNER DESIGN

- Variable resistance and capacitance tuners consists of discrete resistors/capacitors, switched with MOS transistors
- One tuner consist of 16 switches



OPTIMISATION RESULTS

- Optimiser improved the PLL output signal random jitter measured in 300Hz...1MHz bandwidth from 2.21fs to 1.98fs.
- The spurious lines are expected to have their origin in EMI problems introduced by connecting the external tuners to sensitive nodes in the PLL, although, they do not distort the optimisation .



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