

A time stamping TDC for SPEC and ZEN platforms based on White Rabbit

M. Brückner^{1*}, R. Wischnewski² 1-Paul Scherrer Institut, Villigen, Switzerland

* martin.brueckner@psi.ch

2-DESY, Zeuthen, Germany

Wir schaffen Wissen - heute für morgen

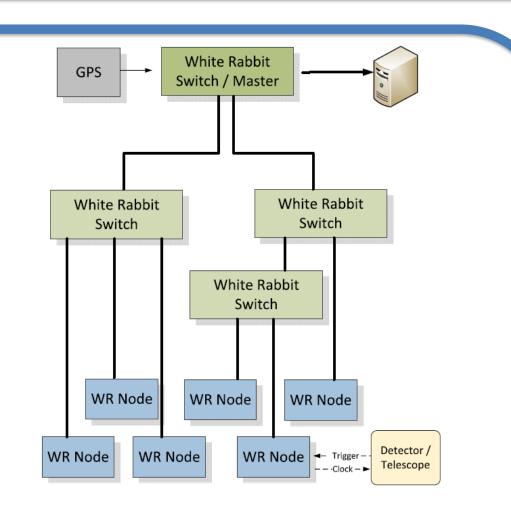
Sub-nsec precision time synchronization is requested for data-acquisition components distributed over up to tens of km2 in modern astroparticle experiments, like upcoming Gamma-Ray and Cosmic-Ray detector arrays, to ensure optimal triggering, pattern recognition and background rejection. The White Rabbit (WR) standard for precision time and frequency transfer is well suited for this purpose. We present two multi-channel general-purpose TDC units, which are firmware-implemented on two widely used WR-nodes: the SPEC (Spartan 6) and ZEN (Zynq) boards. Their main features: TDCs with 1 nsec resolution (default), running deadtime-free and capable of local buffering and centralized level-2 trigger architectures. The TDC stamp pulses are in absolute TAI. With off-the-shelf mezzanine boards (5ChDIO-FMC-boards), up to 5 TDC channels are available per WR-node. Higher density, customized simple I/O boards allow to turn this into 8 to 32-channel units, with an excellent price to performance ratio. The TDC units have shown excellent long-term performance in a harsh environment application at TAIGA-HiSCORE/Siberia, for the Front-End DAQ and the central GPSDO clock facility.

White Rabbit

- Sub nanosecond precision timing system
- Delivers absolute TAI time at every WR node
- Fully deterministic Ethernet-based network for data transfer and synchronization

White Rabbit Switch with 18 ports

Open Source Hard-, Firm-, and Software



The White Rabbit [1] network: made up of WR-switches (WRS), Grand

Master and normal WRS, and of WR-nodes. The WR-nodes deliver clock-

signals to, and/or extract time-stamp signals from the associated detectors

(or telescopes), as symbolized for the lower-right WR-node.

White Rabbit Nodes SPEC and ZEN

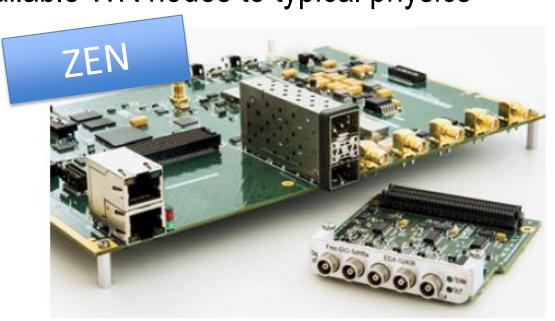
We focus on firmware implementation of commercially available WR nodes to typical physics

applications for time stamping and DAQ control

SPEC (Simple PCIe FMC carrier) board with Spartan 6 FPGA, PCIe and FMC slot

FMC slot used for the 5Ch DIO FMC card



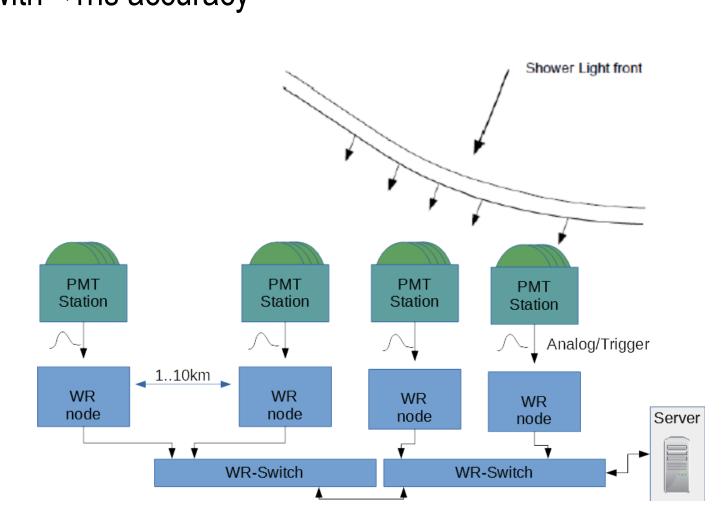


With 2 SFP modules for WR daisy chaining

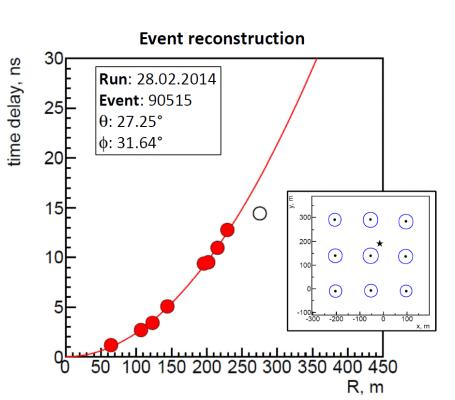
5 input or output channels and adjustable input discriminator

Field Application: TAIGA HiSCORE

- Cosmic- and gamma rays emit Cherenkov light detectable on ground
- Multiple detectors distributed over a large area 1km²-10km²
- 28 station prototype (0.25km²) operating in Tunka, Siberia Each station detects Cherenkov light with 4 PMTs
- Astronomical pointing of <0.1° requires pulse timestamps with <1ns accuracy



PMT stations in the field connected to White Rabbit nodes. The nodes themselves are connected over long fibers to the DAQ center with WR switches server PCs



Shower front fit residuals 13.4/12 **Ξ** 3500 2500 2000 1500 Data <u>--</u>мс 1000

HiSCORE-28 layout

Upgrade to >60 stations in 2018

EAS shower reconstruction [4] with WR. Left: Arrival time delay vs distance R from the shower axis; for an event. Red/white dots: stations retained/excluded in the final fit; red line: reconstructed shower profile. Small panel: Reconstructed core position (black star), the area of the circles is proportional to log(A), with A the station signal amplitude. Right: Distribution of fit residuals after shower reconstruction. Black dots: data; Red line: simulated events; Blue line: Gaussian data fit.

Conclusions

- Basic implementation of a 1 ns TDC: Deadtime free, absolute TAI, no trigger necessary
- Integrated in 3 different variations: single channel TDC w/ DAQ control, 4 channel TDC, and 1 channel 0.25ns sampling TDC on the SPEC WR node
- Easily extendable to more channels with a simple custom board
- 1 ns TDC implemented and running in HiSCORE
- 4 channel TDC as White Rabbit timing monitoring system

White Rabbit Nodes: TDC Firmware Design

Basic TDC design

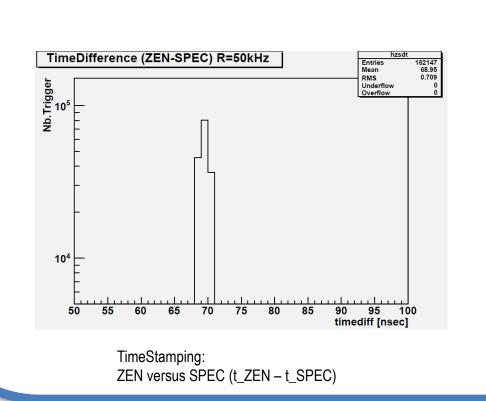
- Developed a 1ns sampling TDC
- 5Ch DIO has adjustable input thresholds for analog input options
- On input signal save time stamp in a CPU accessible FIFO
- Delivers deadtime free TAI time stamps
- No external trigger needed
- Easy to implement
- Input/Output channels can easily be adapted for any trigger and DAQ control requirements

TDC Implementation: SPEC WR node

- TDC attached to the Wishbone bus
- Softcore Im32 CPU assembles UDP packets
- Time stamp read out rate at 1kHz
- Used in several DAQs systems

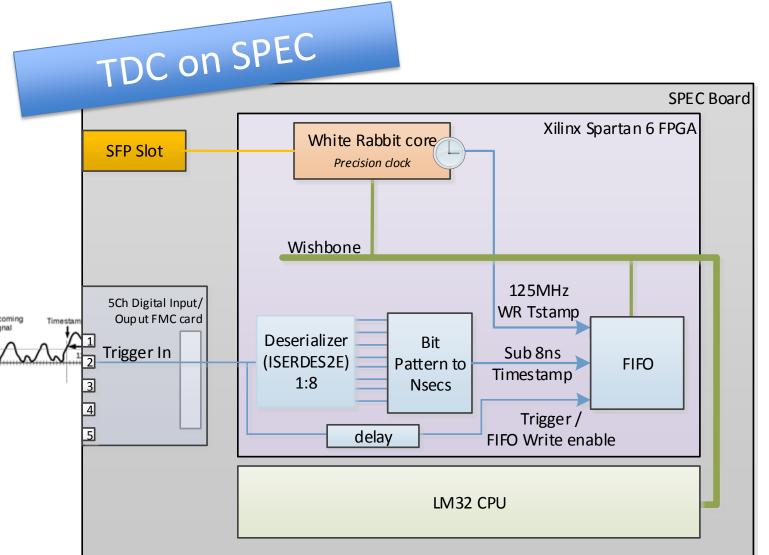
TDC Implementation: ZEN WR node

- Linux running ARM core reads out FIFO
- Software assembles UDP Packets
- High time stamp read out rate of >100 kHz
- Default TDC sampling rate 1ns (Speed Grade -3) and 2ns (-2)

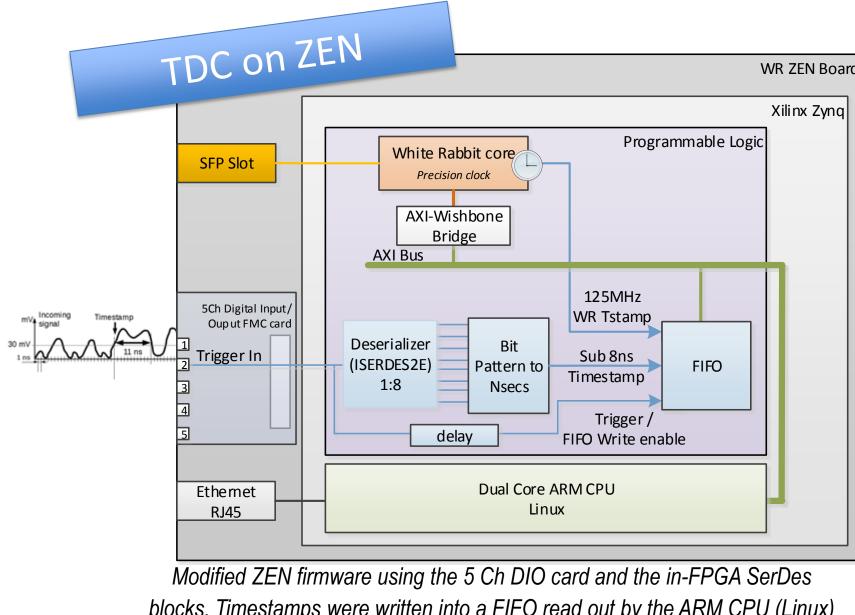


Sub 8ns Trigger In

Basic 1ns TDC design using ISERDES blocks of the FPGA and the White Rabbit timing system



Modified SPEC firmware using the 5 Ch DIO card and the in-FPGA SerDes blocks. Timestamps were written into a FIFO read out by the LM32 CPU.



blocks. Timestamps were written into a FIFO read out by the ARM CPU (Linux)

Multichannel TDC

4 Channel TDC

- 4 TDC integrated in the SPEC FPGA
- Timestamp independently for each channel
- Realized with SPEC board
- Easily extendable to more TDC channels with a simple custom DIO board

4 Channel TDC SPEC Board Xilinx Spartan 6 FPGA White Rabbit core LM32 CPU Wishbone 5Ch Digital Input/ Incoming Timestamp signal 11 ns mV₁ Incoming Timestamp signal 30 mV 11 ns ncoming Timestamp signal 11 ns mV Incoming Timestamp signal 30 mV 11 ns SPEC firmware with TDC units to timestamp 4 input signals

WR node

WR switch

WR switch

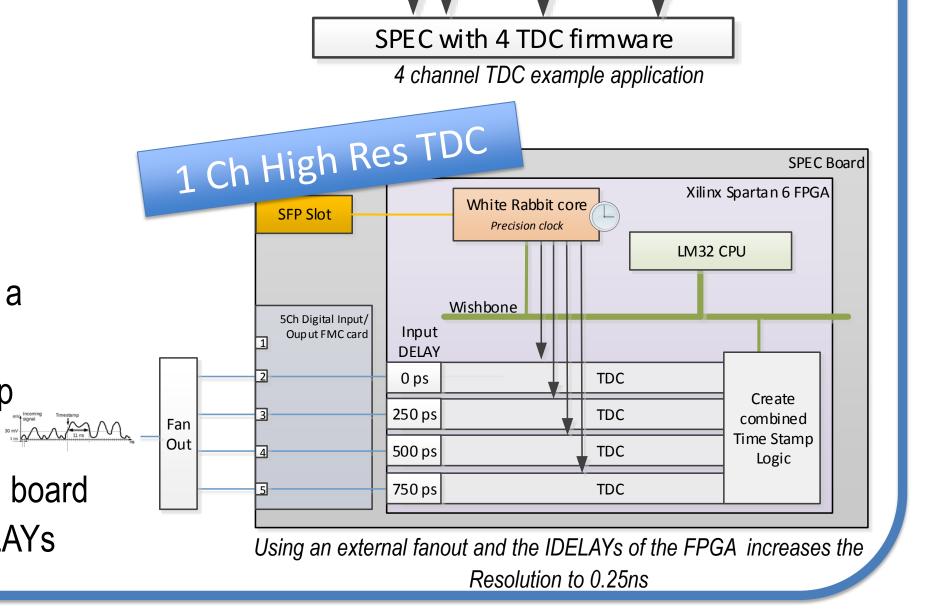
WR switch

4 TDC Example Application

- Easy White Rabbit System Monitoring
- Sample PPS signals of several WR devices
- Multiple clock verification

High Resolution TDC

- Split incoming signal and feed it into 4 individually delayed TDCs
- External fanout can be implemented in a simple DIO card
- Logic creates high resolution timestamp
- Implemented with SPEC board
- Expected better performance with ZEN board due to temperature compensated IDELAYs



References

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