LO BOARD FOR 704.42 MHz CAVITY SIMULATOR FOR ESS

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Abstract

This contribution describes the requirements, architecture, and measurements results of the Local Oscillator (LO) generation board prototype. The design will provide low phase noise clock and heterodyne signals for the 704.42 MHz Cavity Simulator for the European Spallation Source. RF signal detection has critical influence on the simulation's performance and its quality depends on the quality of the two aforementioned signals. The clock frequency is a subharmonic of the reference frequency and choice of the frequency divider generating the clock signals is discussed. The performance of selected dividers was compared. The LO frequency must be synthesized and frequency synthesis schemes are investigated. Critical components used in the direct analog scheme are identified and their selection criteria were given.

Requirements

- Input reference frequency: 704.42 MHz.
- Clock to reference frequency ratio: 1/6 (117.40 MHz).
- IF to reference frequency ratio: 1/28 or 1/22 (25.16 / 32.02 MHz).
- Signals' shape: sine waves with maximum harmonic spurious level of -60 dBc.
- Nonharmonic spurious < -60 dBc for clock and < -50 dB for LO.
- VSWR (on each port): ≤ 1.5.

Clock Frequency Synthesis

- Subharmonic of the fundamental frequency.
- Systematic frequency error in DDS.
- Frequency Divider comparison.

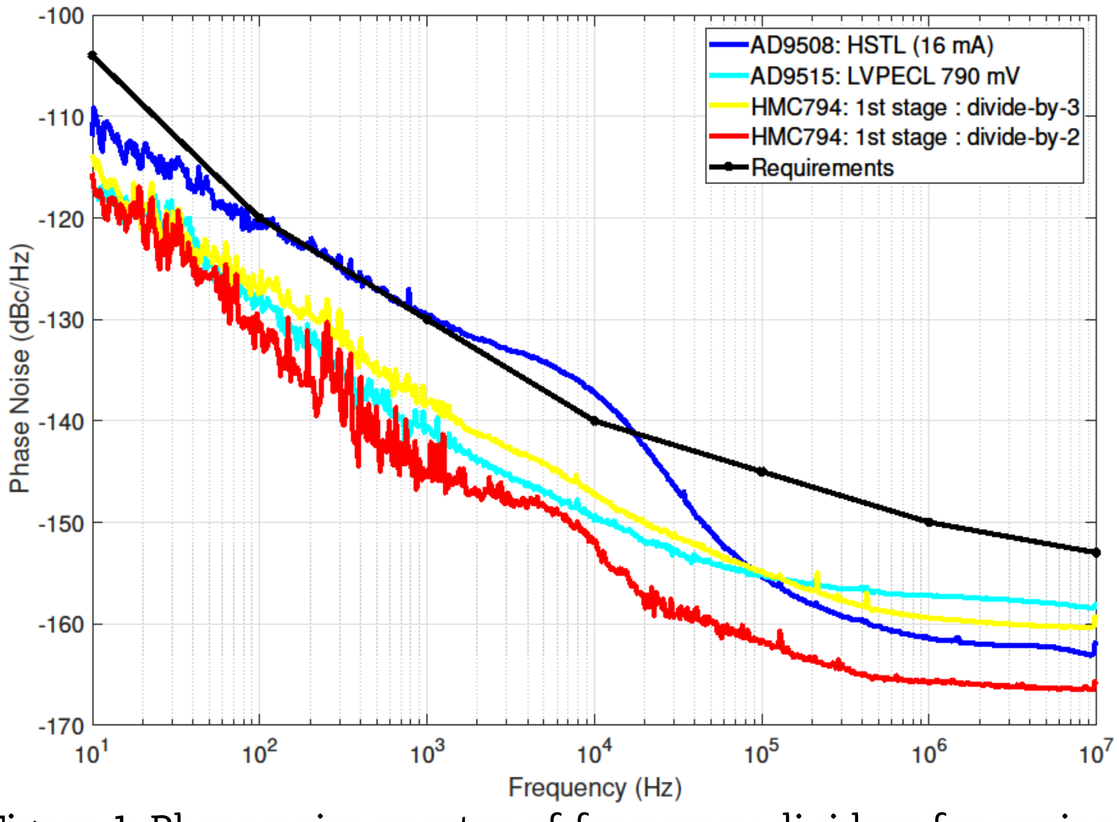

Figure 1: Phase noise spectra of frequency dividers for various output signaling standards and types of dividers.

Acknowledgment

Work supported by Polish Ministry of Science and Higher Education, decision number DIR/WK/2016/03.

ICALEPCS2017
Barcelona · Spain, October 8-13 · Palau de Congressos de Catalunya

LO Frequency Synthesis

- Synthesis scheme: Direct Analog (reduction of far from carrier uncorrelated phase noise).
- Investigation of frequency dividers.
- Sideband selection.
- Mixer selection criteria: isolation.
- Filter selection criteria: loss, matching.
- IF Divider comparison.

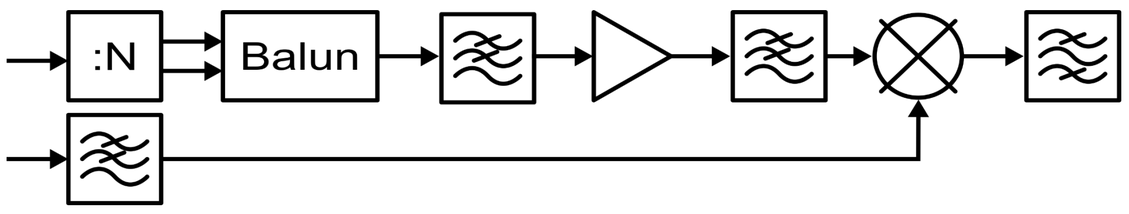

Figure 2: Block diagram of the LO synthesis circuit.

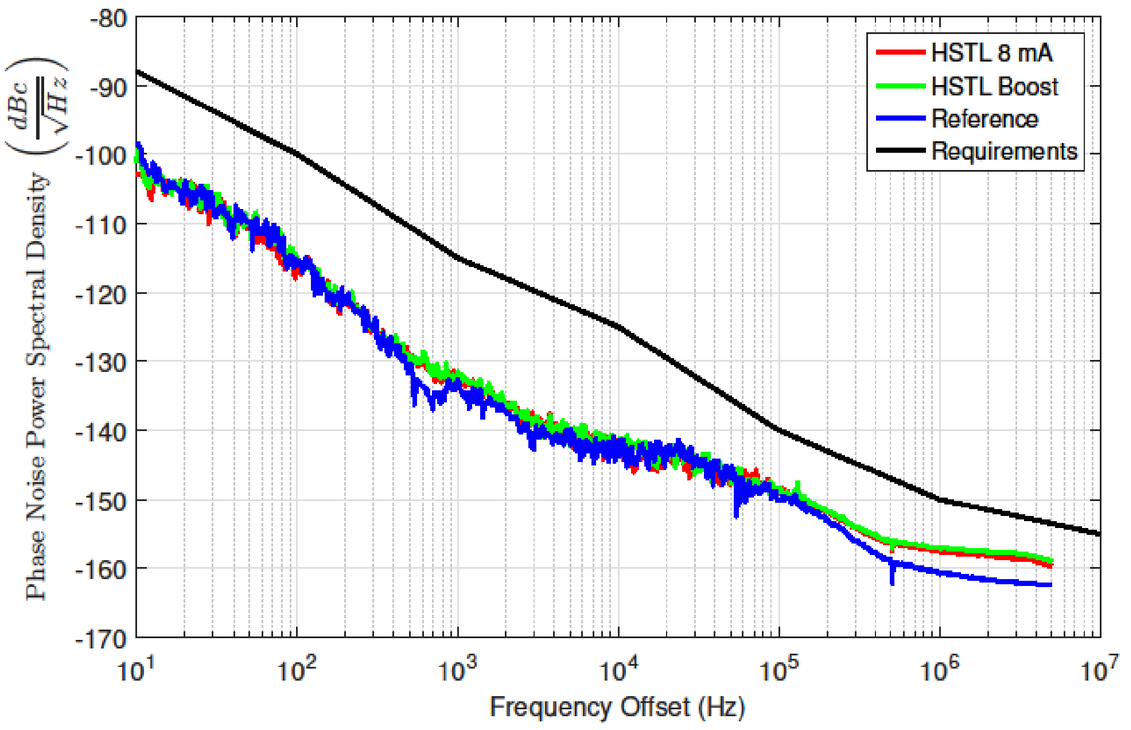

Figure 3: Phase noise spectra of the LO signal for two signaling standards and an ideally converted reference signal. Division ratio: 22, input frequency: 704.42 MHz.

Measurements

- The clock ports' matching doesn't meet the requirements.
- The LO ports' matching meets the requirements with a very small margin.

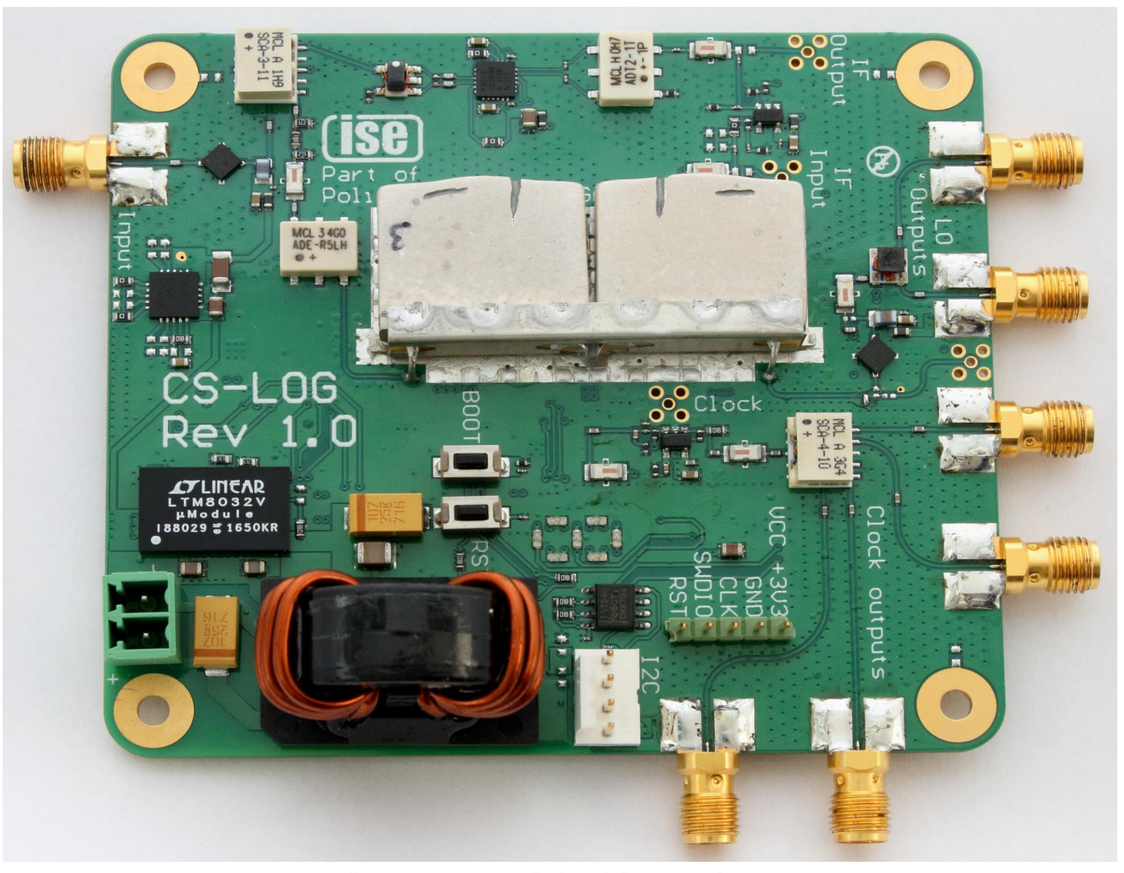

Figure 4: Picture of an assembled board.

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