FPGA-based BPM Data Acquisition for LCLS-II

SLAC NATIONAL ACCELERATOR LABORATORY

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Motivation

The LCLS-II facility will be capable of delivering an *electron beam* at a *rate* of up to almost *1MHz*. The BPM system (and other diagnostics) are required to acquire time-stamped readings for each individual bunch. The high rate mandates that the processing algorithms are implemented with *FPGA technology*.

LCLS-II BPMs

Two different types of Beam-Position Monitors are used at LCLS-II:

Stripline and Button BPMs estimate position by measuring the amplitudes of signals induced by the beam at pickup electrodes which are located at opposite walls.

Fig. 1: Stripline BPM

Cavity BPMs use a resonant mode which is excited by the beam with coupling depending on beam position.
Reference cavity provides beam-charge and -phase reference.

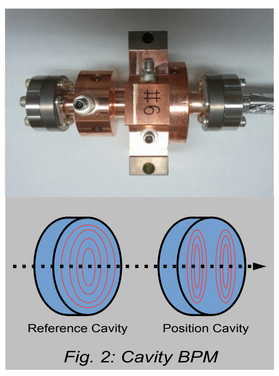

Fig. 2: Cavity BPM

Each type requires specific processing:

- Stripline: amplitude detection sufficient; critical: small difference of big numbers.
- Cavity: higher resolution, low SNR – synchronous detection necessary.

Hardware

Stripline BPMs

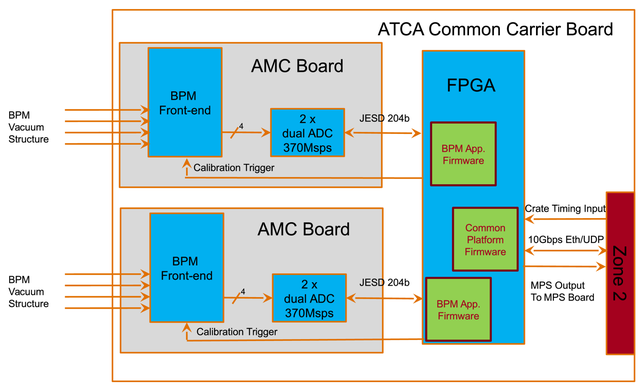

Fig. 4: Stripline BPM DAQ System

- SLAC common ATCA carrier with FPGA
- Special-purpose AMCs (gain/attenuator, stripline calibration circuit)

Cavity BPMs

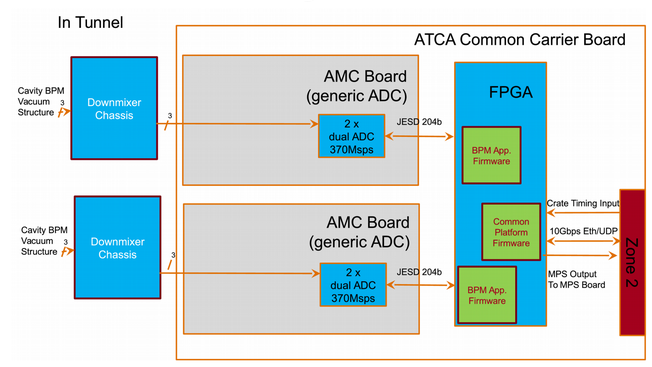

Fig. 5: Cavity BPM DAQ System

- SLAC common ATCA carrier with FPGA
- Generic SLAC high-speed ADC AMC
- X-band downmixer chassis in tunnel

Communication

Most communication with FPGA is 10GbE:

- Control-system access for (slow) monitoring and controls.
- Fast communication with FPGA on other blades via switched ATCA backplane.

BPM Firmware

Fig. 7: BPM-specific FW block diagram; stripline "plugin" shown

BPM-FW is modular; generic blocks (blue):

- Post-processing (incl. coordinate transform)
- Data fanout
- Triggering

Specific algorithm (stripl/cavity) is a 'plugin' module.

Stripline Algorithm

Amplitude detector → difference-over-sum (see Fig.7, turqoise)

Cavity Algorithm

More demanding synchronous detection. Correlate pos. and ref. signals in freq. domain (Goertzel-DFT) and normalize to reference amplitude.

$$\hat{u} = \frac{U * \overline{U}}{R * \overline{R}}$$

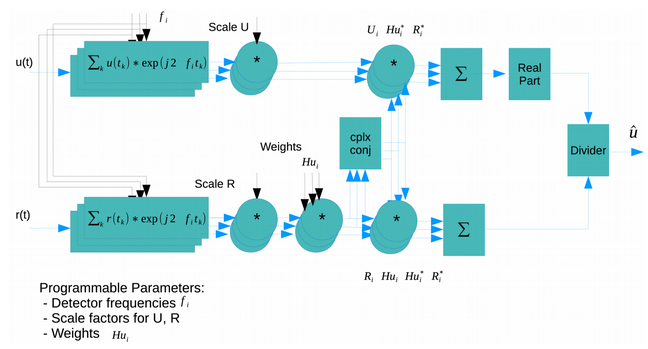

Fig. 8: Cavity BPM Processing Algorithm

The DAQ System

The DAQ System requires

- Front-end (analog; depends on BPM type). Contains gain/attenuation, filters, down-mixer (cavity BPM only) etc.
- High speed digitizer (370MSPS)
- FPGA with connectivity to the control system and other high-performance systems (HPS – i.e., subsystems with must process 1MHz beam in real-time).

Fig. 3: DAQ System

The *SLAC Common Platform* (see THMPL08) provides a powerful framework with most of the necessary hard- and firm- and software components.

- ATCA based
- 10GbEthernet technology
- FPGA on std. carrier; std. or specific AMCs

Firmware

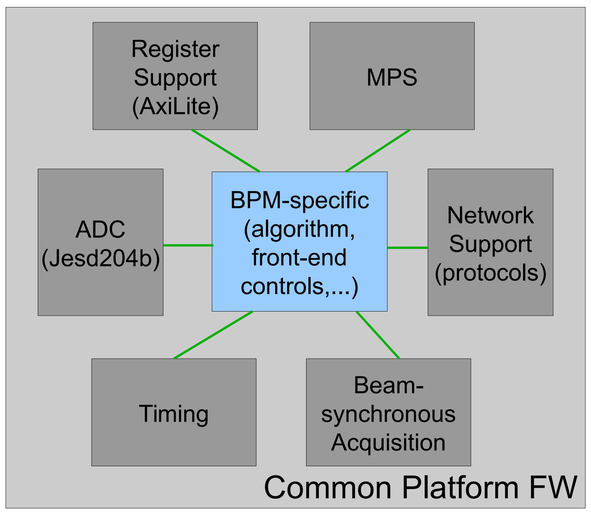

Fig. 6: Firmware Overview. Grey boxes are common-platform components.

BPM firmware integrates with SLAC common-platform firmware. BPM is the 'application' block:

- Process raw-samples into position readings
- Forward to multiple data sinks (BSA, software, MPS, …) using interfaces defined by the common platform (green).

Software

Slow controls (including raw diagnostic wave-forms) easily integrated into existing BPM soft-ware.

Readout of fast buffers (BSA) uses a new common library.

(On-line 1MHz data processing is intra-firm-ware only.)

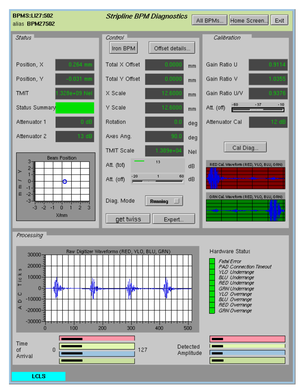

Fig. 9: EPICS Diagnostic Screen

Acknowledgment

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