A Position Encoder Processing Unit

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A Position Encoder Processing Unit able to handle multi-encoder, multi-protocol configurations has been developed at the ESRF. The unit has embedded calculation capabilities to process the incoming data for positioning control feedback and metrological applications. It interfaces with quadrature signalling, and SSI, BiSS-C, EnDat and HSSL protocols.

Introduction

High-accuracy positioning systems require **multi-sensor** devices to correct the actuator position for external factors.

Typical sensors are **position encoders** but other physical quantities sensors can be used, e.g., room temperature.

Position encoders can transmit data with different protocols: **SSI**, **BiSS-C**, **EnDat**, and **HSSL** and **quadrature** signals.

Data from sensors must be **processed** and the feedback information be **emulated** to the motion controller.

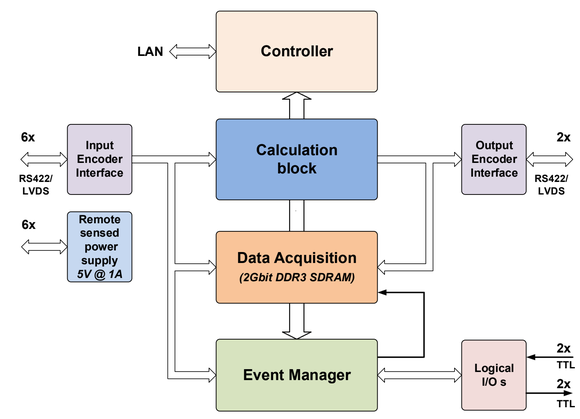
Capability to **capture and transfer data** to a host computer for subsequent treatment is fundamental for these applications.

The unit presented here **features all these aspects** and perfectly integrates into the ESRF control environment.

Functional description

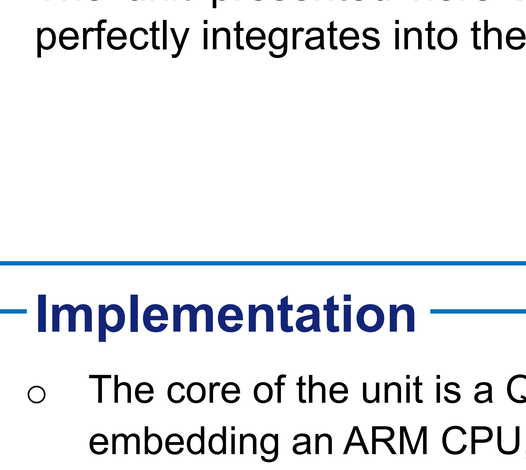
The ESRF Position Encoder Processing Unit, PEPU, features:

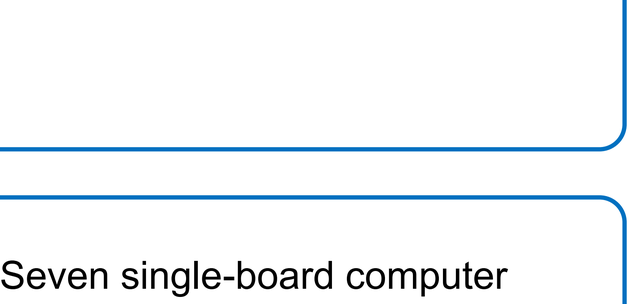
- A controller module for communication and remote control functions through the network (Ethernet)
- A configurable calculation block that processes the incoming data
- Six configurable input channels that power and interface with the most common encoders
- Two configurable output channels that emulate encoders
- A data acquisition mechanism for metrological application
- An event manager to handle the synchronization aspects



Implementation

- The core of the unit is a QSeven single-board computer embedding an ARM CPU, and a Xilinx Kintex-7 FPGA
- The FPGA implements a highly configurable interfacing to support the most common protocols
- The calculation block in the current implementation is limited to linear combinations but a software plug-in can be used for more complex functions
- The embedded buffer is based on a 2 Gbit DDR3 SDRAM
- The synchronization digital signals are capable to handle 50-Ohm loads or termination
- The unit is presented in a rack-mountable 1U enclosure





Example of application

The example below illustrates the PEPU main capabilities:

- **Data acquisition**
  - relevant data can be stored in the embedded fast-access buffer for subsequent transfer to the host
- **Multi-protocol interfacing, processing and emulation**
  - interface to BiSS, EnDat, HSSL, and SSI
  - processing of inputs 1, 2, 3 and 4 in this example
  - emulation of encoder on output 7
- **Protocol conversion**
  - SSI on input 4 → quadrature on output 8

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