PandABlocks Open FPGA Framework and Web Stack

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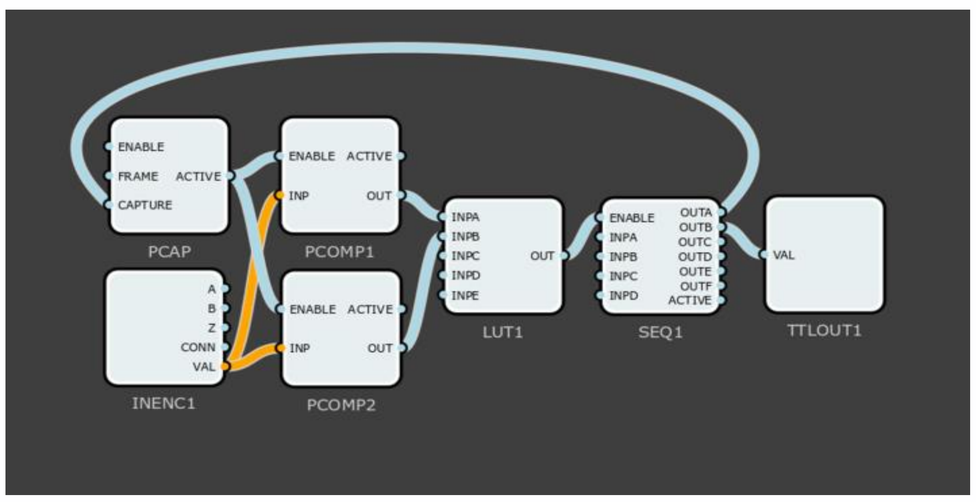
Abstract

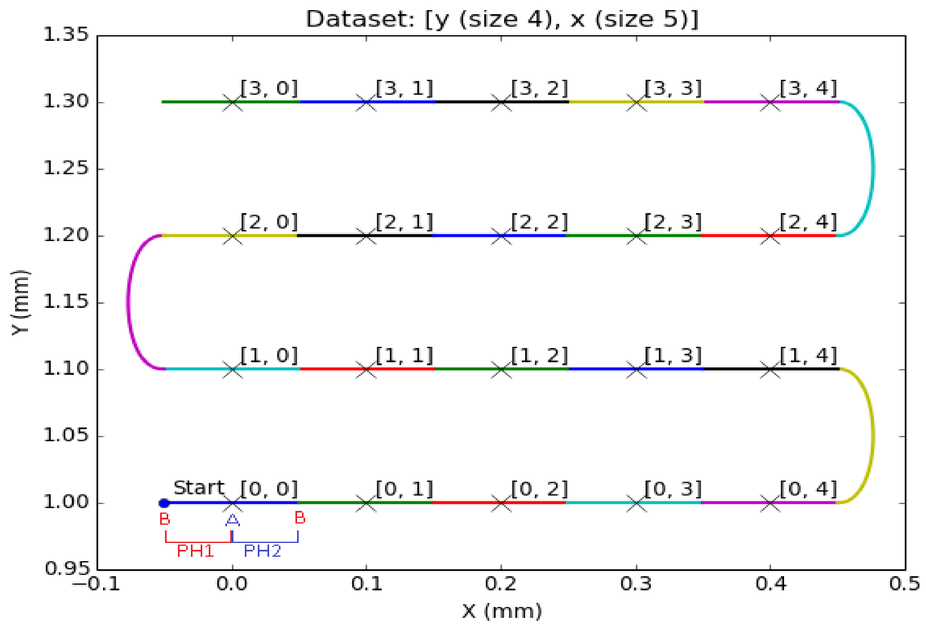
PandABlocks is the open source firmware and software stack that powers PandABox, a Zynq SoC based "Position and Acquisition" platform for delivering triggers during multi-technique scanning. PandABlocks consists of a number of FPGA functional blocks that can be wired together at run-time according to application specific requirements. Status reporting and high speed data acquisition is handled by the onboard ARM processor and exposed via a TCP server with a protocol suitable for integration into control systems like "EPICS" or "TANGO". Also included in the framework is a webserver and web GUI to visualize and change the wiring of the blocks. The whole system adapts to the functional blocks present in the current FPGA build, allowing different FPGA firmware be created to support new FMC cards without rebuilding the TCP server and webserver. This paper details how the different layers of PandABlocks work together and how the system can be used to implement novel triggering applications.

Example Applications



Block setup on web GUI for snake scan with time-based pulses

A snake scan with time based pulses can be set up by triggering position compare blocks at the start of each run. Two position compare blocks are used, one for each direction, a sequencer block is then used to generate the frame pulses which trigger the detector on “TTLOUT1”, and also generates the capture pulse. This allows the possibility to detect the start of the row and produce time based exposure triggers for the camera and capture in the middle of those frames. This is done for each row in both the forward and reverse directions.

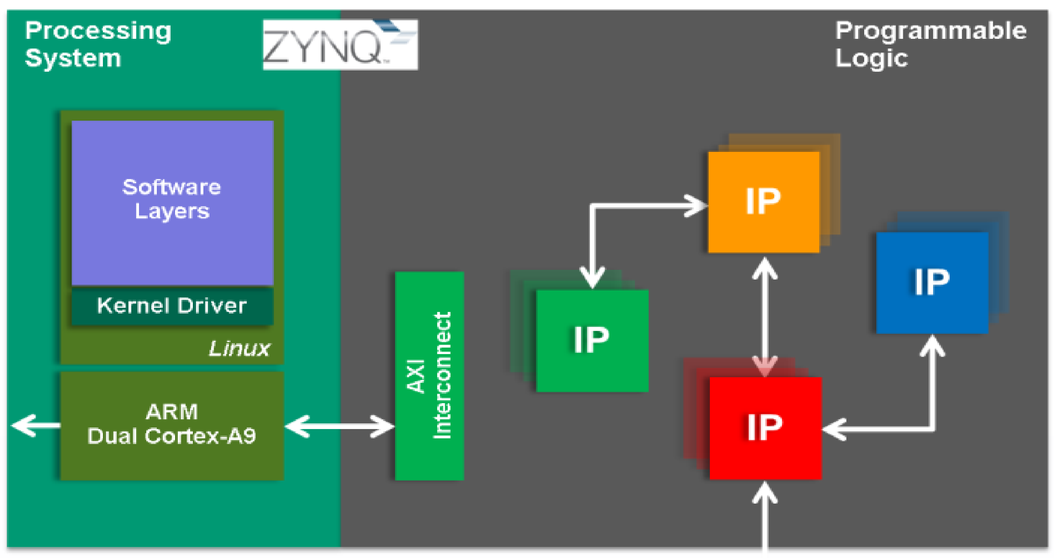


Ph1 t	Ph1 Out		Ph2 t	Ph2 Out	
(ms)	A	B	(ms)	A	B
100	0	1	100	1	0

Snake scan with time based pulses

FPGA Architecture

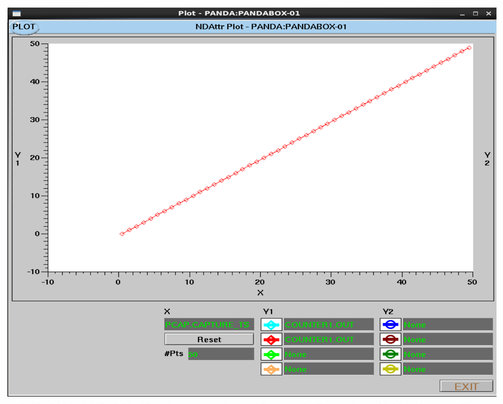
A customised Linux XiLinx kernel with busy-box is deployed on the ARM dual Cortex-A9. Specific types and quantities of different IP blocks, both standard and customised, can be loaded on the FPGA and then wired together at runtime to achieve overall functionality for specific applications. Individual IP blocks for use on PandABox are defined in a configuration file and are instantiated when building the system. Once built and installed, the number and type of blocks are fixed on the system with the routing/ signal flow fully configurable between them at run time. It is possible to install different types of FMC cards on the board, writing new IP blocks to work with them. This also facilitated by the customisable, flexible nature of the system.
The Processing system communicates with these IP blocks via the AXI Interconnect register interface for the ARM processor.



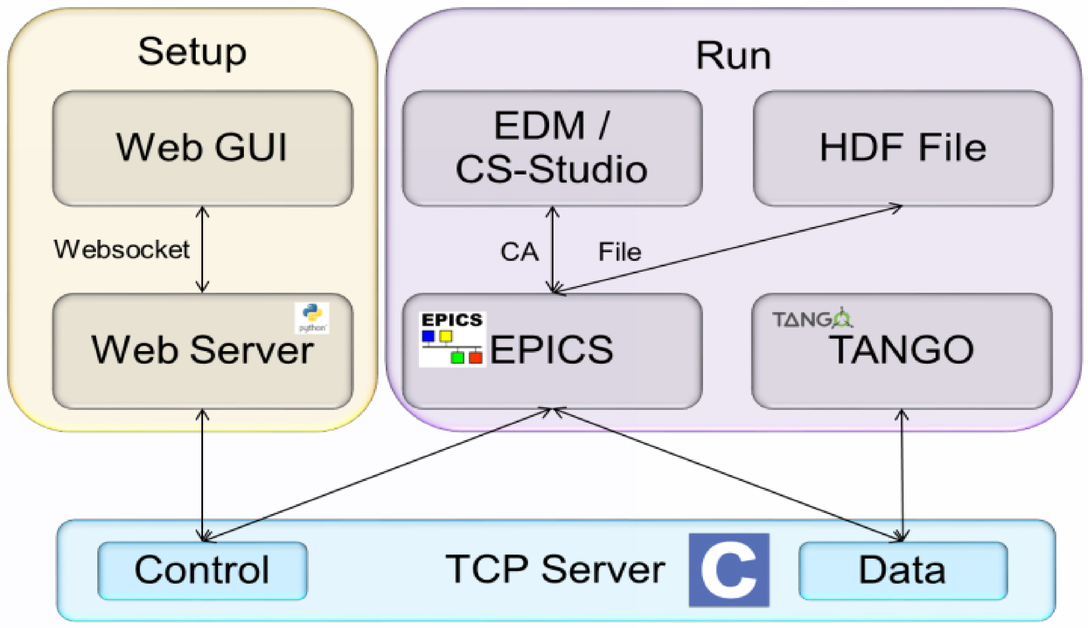
PandABlocks FPGA architecture

Software Architecture

The general use case is to configure the PandABox via the web GUI. The experiment can then be executed with control and monitoring through the TCP server with a standard EPICS areaDetector driver. It is possible to create custom applications which can be loaded onto the PandABox for reusability. EPICS Channel Access client applications like EDM or CS-STUDIO can then be created to interact with these specific configurations. This allows only exposing a subset of controls and configuration settings to the user via EPICS as required for the particular experiments.



EPICS NDAttrPlot showing PandABlocks COUNTER block output



PandABlocks software layers

For more information please contact Chris Turner at chris.j.turner@diamond.ac.uk