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RECENT UPDATE OF THE RIKEN RI BEAM FACTORY CONTROL SYSTEM

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Abstract

The RIKEN Radioactive Isotope Beam Factory (RIBF) is a cyclotron-based heavy-ion accelerator facility. A major part of the components of the RIBF accelerator complex is controlled by the Experimental Physics and Industrial Control System (EPICS). A homemade beam interlock system (BIS) plays an essential role of safely delivering high-power heavy-ion beams. In this paper, we discuss the recent upgrade of the existing beam interlock system to a new beam interlock system (BIS2). Like BIS BIS2 is based on a programmable logic controller (PLC). It has a multi-CPU configuration with a Linux-based PLC-CPU on which EPICS programs can be executed in addition to a sequence CPU. The design of BIS2 and its offline tests in which its basic performance was verified are presented. We plan to expand BIS2 as a successor to the existing BIS that has been operating for over 10 years.

INTRODUCTION

The RIKEN Radioactive Isotope Beam Factory (RIBF) began operation in 2006 and has provided the world's most intense beams of unstable nuclei for nuclear physics studies. RIBF was constructed as an extension of our old facility (RARF) by adding three new cyclotrons, one of which is the world's first superconducting ring cyclotron (SRC). RIBF consists of two heavy-ion linear accelerator (LINAC) injectors and five heavy-ion cyclotrons. Various acceleration modes can be achieved by changing the combination of the accelerators used, and one of them is chosen according to beam energy and the ion species required by users. For example, a uranium beam, which is suited to produce very neutron-rich medium-mass ions, can be accelerated up to 345 MeV/nucleon by using a new LINAC injector and four ring cyclotrons. On the other hand, the K = 70 MeV Azimuthally Varying Field (AVF) cyclotron accelerates low-energy light-ion beams and provides them with its own experimental courses [1].

The components of the RIBF accelerator complex, such as magnet power supplies, beam diagnostic devices, and vacuum systems are controlled by the Experimental Physics and Industrial Control System (EPICS) [2] with a few exceptions, such as the control system dedicated to all the radio frequency systems of RIBF. However, all the essential operation datasets of EPICS and other control systems are integrated into the EPICS-based control system [3]. In addition, two types of interlock systems that are independent of the accelerator control systems are in operation in the RIBF facility: a radiation safety interlock system for human protection [4], and a beam interlock system (BIS) that protects the hardware of the RIBF accelerator complex from potential damage from the high-power heavy-ion beams [5]. In order to ensure safety, we implemented a dual interlock by inputting some signals to both systems. Figure 1 gives an overview of the RIBF control system.

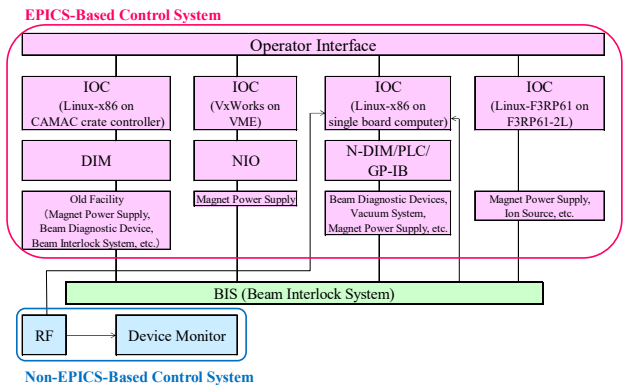

Figure 1: Overview of the RIBF control system.

EXISTING BEAM INTERLOCK SYSTEM

The existing BIS was designed to stop beams within 10 ms after receiving an alarm signal. On receiving an alarm signal, BIS outputs a signal to one of the beam choppers installed immediately below the ion source that deflects the beam immediately. Many accelerator and beam-transport-line components are registered to BIS and alarm signals sent to BIS are both digital and analog signals that show the abnormal behaviors of the components, such as an error in a magnet power supply or an overly high beam loss detected by baffle slits installed at various places on the RIBF accelerators and their beam transport lines.

One important function of the RIBF BIS is flexibility to impose appropriate interlock conditions according to each beam condition required by users. As mentioned previously, various beams (high power or low power) are accelerated by adopting various combinations of the accelerators. Hence, both the components relevant to the acceleration mode at that time and alarm levels have to be specified; for example, the allowable beam losses at baffle slits according to the actual beam power. To realize the flexibility required by daily RIBF operations, various interlock condition files in which the interlock signal pattern and alarm levels are specified are prepared in advance. BIS then downloads one of these interlock condition files appropriate to the experiment to be

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performed. Another important feature of BIS is utilization of multiple beam stoppers. When BIS detects an alarm signal of a component used in beam acceleration, it stops the beam immediately using a beam chopper and also inserts the beam stopper (Faraday cup) specified in the interlock condition file and installed upstream of the problem component. After inserting the relevant beam stopper, the beam chopper can be switched off and beam delivery resumed up to the inserted beam stopper. This feature is especially useful during beam tuning because beam tuning is conducted in a step-by-step manner, from an injector to a final-stage accelerator. The inserted beam stopper can be extracted from the beam line after the problem is fixed.

The hardware configuration of BIS is shown in Fig. 2. BIS was developed based on programmable logic controllers (PLCs) manufactured by Mitsubishi Electric Corporation (hereafter, Melsec PLCs). All of the interlock signals are connected to the I/O modules of the Melsec PLCs.

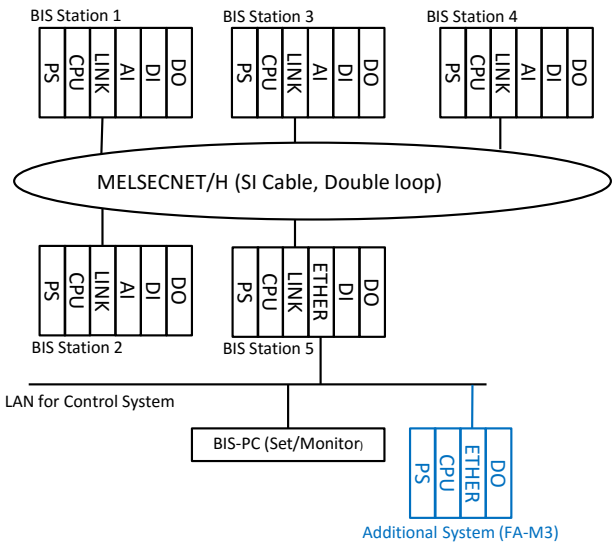

Figure 2: Example of the hardware configuration of BIS. At present, two BISs are in operation at the RIBF facility. The BIS shown here covers a high-energy part of the RIBF facility. It has an additional branch (shown in blue) that uses FA-M3.

As stated above, the RIBF accelerator complex consists of two LINAC injectors, five cyclotrons, many experimental ports, and beam transport lines connecting them to each other. These are broadly distributed in three buildings. The new building houses two new ring cyclotrons, including SRC and large experimental setups. The two old buildings house injectors, other intermediate-stage cyclotrons, and experimental setups dedicated to low-energy heavy-ion beams. In order to secure the response speed required by BIS, two BISs were introduced, one covering the new building and the other the old buildings. The two BISs have the same system with the same configuration and each has its own PC for setting interlock conditions and monitoring interlock signals. In addition, each BIS is divided into five stations of Melsec PLCs that are connected to each other through the MELSECNET/H network system—an optical loop system. All signal information is summarized in one of the five stations that contains an Ethernet module. This station with the Ethernet module communicates with the BIS PC. Each BIS has approximately 300 digital input signals, 70 analog input signals, and 30 digital output signals.

DEVELOPMENT OF NEW BEAM INTERLOCK SYSTEM

The existing BIS began operation in 2006, concomitant with RIBF operation. BIS has played an essential role for safety operation of high-intensity heavy-ion beams, such as a 345-MeV/nucleon ^{238}U beam of 58-pnA and a 345-MeV/nucleon ^{48}Ca beam of more than 700 pnA. The beam power has already exceeded 10 kW, and beam operation at the level of several tens of kW is expected in the near future [6]. To handle higher-power beams more safely, a much higher response speed is required of the BIS in order to mitigate hardware damage caused by higher-power beams to the present level. In addition, a greater number of components than those included in the present BIS have to be carefully monitored because subtler failures potentially cause severe accidents in the case of very high-power beams. However, there is a limit to how high the response speed can be increased to by increasing the associated components in the existing BIS. Therefore, we started development of the next-generation BIS (hereafter, BIS2) last year, which is designed to have more advanced performance and convenience compared to BIS.

BIS2 implements interlock logic that is fundamentally equivalent to those of the existing BIS. Based on the operation experience of more than 10 years of BIS, we believe the following points are important in the BIS2 development:

1. All the development of BIS2, such as module selection and program development, should be performed by ourselves from scratch. Because we outsourced program development of the existing BIS, we often felt inconvenienced when we needed to make minor modifications during beam operation.
2. Reducing the amount of data shared between different stations is essential in BIS2 in order to reduce the time to stop the beam after receiving the interlock signal. Because too much information is shared among all the stations through optical links in the existing BIS, for example, the information of setting patterns of the input signals and the information on the signal output destinations, the time required for stopping the beam is 15–20 ms, which is greater than its design value of 10 ms. Taking this into account, only the output signal status is shared among stations in BIS2.

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As a device satisfying all the above requirements, we adopted the PLC system manufactured by Yokogawa Electric Corporation (hereafter, FA-M3). The most important advantage of the present choice is that we can use the Linux-based CPU manufactured by Yokogawa Electric Corporation (hereafter, F3RP61 CPU) in combination with the FA-M3 system. We have sufficient experience executing EPICS programs on the F3RP61 CPU. A new control system for ion sources [7] and the control system of a part of the magnet power supplies adopt the F3RP61 CPU. We plan to have coupled operation of BIS2 to the main RIBF control system based on EPICS, especially in setting and monitoring interlock signals using EPICS.

Figure 3 shows the hardware constitution and process flow of the BIS2 prototype now under development. Note that we adopt here the two-station configuration, but there is no technical limit to the number of stations and the number of I/O points included in BIS2. A list of the modules used in BIS2 is also given in Table 1.

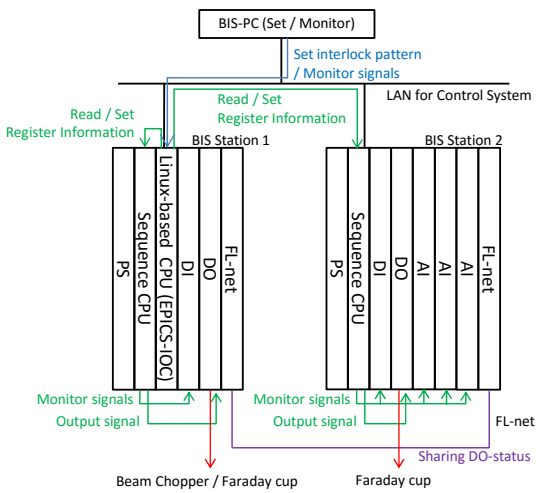

Figure 3: Hardware constitution and process flow in BIS2. Blue lines signify communication via Ethernet, green lines signify communication via PLC bus, and Purple lines signify communication via FL-net.

Table 1: FA-M3 Modules Used with BIS2

Type	Product	Note
CPU1	F3SP71-4S	Sequence CPU
CPU2	F3RP61-2L	Linux-based CPU
DI Module	F3XD32-3F	
DO Module	F3YD14-5A	Transistor contact
AI Module	F3AD08-1V	
FL-net Module	F3LX02-1N	Transmission speed: 10 Mbps

The system employs a multi-CPU configuration; the sequence CPU, F3RP61 CPU, I/O modules, and FL-net module are mounted on one station (station-1), and the sequence CPU, I/O modules, and FL-net module are mounted on the other station (station-2). Interlock logic is implemented in the sequence CPU because high-speed processing and high reliability are required. Such high-speed processing is not necessary for setting and monitoring the interlock signal; these functions are implemented in the F3RP61 CPU. We execute EPICS on the F3RP61 CPU and access it from the upper-level PC in the control room via Ethernet. The F3RP61 CPU reads the status of the input and output signals of the I/O modules indirectly via the internal devices of the sequence CPU because the master of the I/O modules is the sequence CPU and direct access from the F3RP61 CPU is forbidden. Communication between the F3RP61 CPU and the sequence CPU in the same station is via the PLC bus. Communication between the different stations is via the network using a netDev program developed by the control group of KEK and RIKEN Nishina Center in 2004 with the aim of controlling various kinds of PLCs and the in-house controller developed by RIKEN Nishina Center [8]. On the other hand, the interlock signal information transfer between two stations is performed through FL-net—an open network protocol used for interconnection between controllers.

PERFORMANCE TESTS OF BIS2

We plan to apply the BIS2 prototype under development to a small part of the RIBF facility, namely the AVF cyclotron and its low-energy experimental facility, as a first step in the RIBF BIS upgrade in the near future. Simulating the AVF cyclotron facility, we conducted basic performance tests, in which we registered 18 digital inputs, no analog input, and seven digital output signals to the I/O modules in station-1, and 25 digital inputs, 23 analog inputs, and no digital output signal to the I/O modules in station-2. First, we verified that the BIS2 prototype outputs signals correctly when changing the pattern of the input signals. Next, we measured the signal transmission speed in the system, which is one of the most important performance factors. In our case, the transmission data size between the two stations via FL-net is designed to be four words for the link relay area and zero word for the link register area at the FL-net module, F3LX02-1N. According to the technical data published in the F3LX02-1N catalog, data communication through FL-net requires approximately 4 ms at 10 Mbps when the allocation size per station is 4 (link relay area) + 64 (link register area) words, the same data capacity is allocated to each FL-net module at each station, and the number of connected stations is two, as in the BIS2 prototype. Naturally, the transmission speed in the FA-M3 system using FL-net depends on the size of the transmitted data per station and the number of stations (common memory size being used) [9]. The transmission speed decreases with the transmission data size and number of connected stations.

The obtained results for the transmission speed between two stations are shown below. First, we measured the response time within the same station using an oscilloscope. Figure 4 shows an example, in which the

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yellow line shows the input signal and the green line shows the output signal. In this measurement, we set the sampling period of the input signal to minimum at the DI module. The average response time in the same station after five measurements was approximately 1.4 ms. Figure 5 shows the same examples as in Fig. 4. However, in this case, the data are transmitted through the FL-net because signal input and output are carried out at different stations. The averaged response time was approximately 3.8 ms. Thus, the time used for data transmission through the FL-net is 2.4 ms, which is consistent with the specification listed in the catalog. The measured response speed is greater than the specification requires in BIS2 development.

We have successfully confirmed the basic performance of BIS2, and online operation of the BIS2 prototype at the AVF site is scheduled for this fiscal year. Subsequently, we plan to replace the very old beam interlock system of our LINAC facility with BIS2 by increasing the number of nodes of the BIS2 prototype. The LINAC facility is a part of RIBF and consists of one LINAC injector and its own experimental courses. One of the issues we are also interested in is use of Ethernet for control automation technology (EtherCAT) as a communication method between stations instead of 10-Mbps FL-net. We have started related testing and expect higher speed performance. In addition, we will test a new DO module that has response speed 10 times higher than the present F3YD14-5A as soon as module delivery starts.

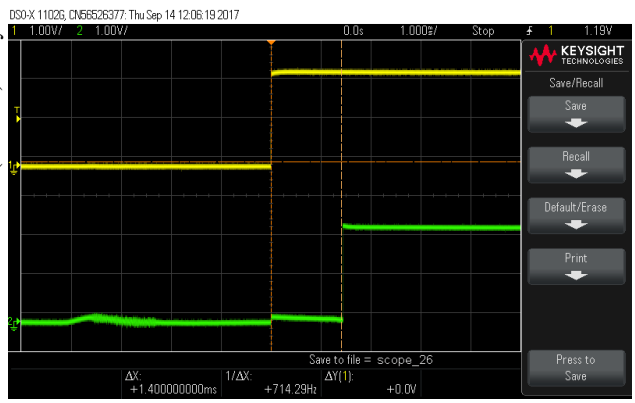

Figure 4: Signal output timing at BIS2 (within the same station, 1.40 ms).

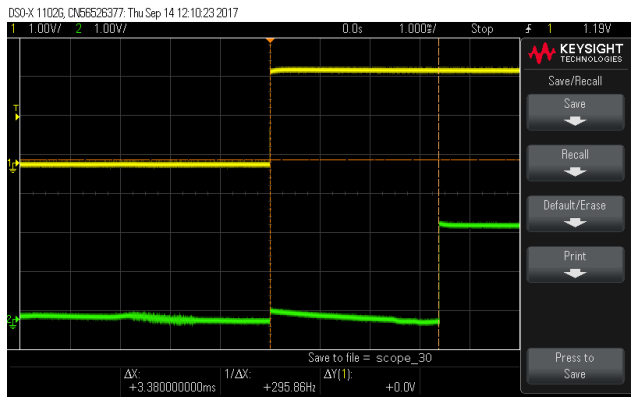

Figure 5: Signal output timing at BIS2 (between separate stations, 3.38 ms).

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