ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUCPL01

REFURBISHMENT OF THE ESRF ACCELERATOR SYNCHRONISATION SYSTEM USING WHITE RABBIT

G.Goujon†, N.Janvier, A.Broquet ESRF, Grenoble, France

Abstract

The ESRF timing system, dating from the early 90's and still in operation, is becoming obsolescent and needs complete refurbishment. The White Rabbit timing system -developed by CERN- offers many attractive features for the implementation of a synchrotron synchronisation and timing system, the key one being the possibility to carry RF over the White Rabbit optical fibre network. CERN having improved the feature to provide network-wide phase together with frequency control over the distributed RF, the whole technology is now mature enough to propose a White Rabbit based solution for the replacement of the ESRF system, providing flexibility and accurate time stamping of events. The paper provides details on the renovation project and describes the WHIST instrument that is being designed to that purpose.

ESRF SYNCHRONISATION SYSTEM

The current accelerator synchronisation system was developed at the construction phase of the ESRF, and is still in operation. This very reliable system is built around a centralized Radio Frequency (RF) driven sequencer distributing synchronization signals along copper cables. The analogue RF clock is broadcast over a separate copper network. The main characteristics of the ESRF accelerators are provided in Table 1.

Characteristics	
Radio Frequency (RF)	352 MHz ; 2.84 ns period
Booster	352 buckets; 1 MHz revolution frequency
Storage Ring (SR)	992 buckets; 355 kHz revolution frequency
Injection Sequences	4 Hz; 10 Hz

Table 1: ESRF Accelerator Characteristics.

This centralized "Bunch Clock" system (Figure 1), based on a top-down architecture, ensures the correct operation of the accelerators, delivering distributed triggers following a specific sequence which is basically detailed below.

The whole sequence is initiated with a so-called T0 trigger, generated by the Booster magnet power supply at start of ramping.

The RF synchronised Bunch Clock then provides sequentially:

- A programmable delay (1 ms minimum) to align the booster magnet energy to the LINAC output energy.
- A "gun trigger" (1) to generate an electron bunch at the LINAC input.
- An "Injection trigger" (2), to transfer a bunch from the Linac into the Booster. Optionally up to 5 bunches, properly spaced, can be launched in a row.
- An "Extraction trigger" (3), to extract the bunch from the Booster into the Storage Ring at the end of acceleration. A precise synchronization occurs in order for the bunch to be transferred at the programmed position in the SR (4).
- The whole sequence starts again at the reception of a new T0 trigger.

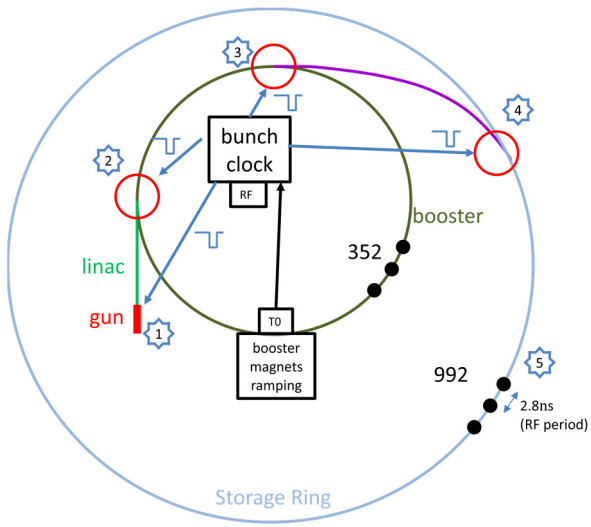

Figure 1: ESRF – Synchronisation system.

The system also provides additional triggers and clocks such as SR revolution frequency, that can be used for Diagnostic purposes and also by the Beamlines.

SYSTEM REFURBISHMENT GOALS AND CHALLENGES

The present system is stable, proven to be highly reliable but is becoming obsolescent. It also shows several heavy technical limitations. Based on a cabled logic centralized sequencer, it offers almost no possibility to add new features. The fixed copper cable distribution of signals makes combinations, as simple as gating, very difficult to implement. The addition of new signals to the existing architecture is impossible without adding cables, contributing to increase complexity of the system and, to a certain point, downgrade its maintainability.

The system by itself does not offer precise time-stamping capability, while the demand for such a feature

† goujon@esrf.fr

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUCPL01

is significantly growing for diagnostic and experiment purposes.

The uneasy provision of timing signals to Beamlines, when demands for synchronous detection or gated data acquisition are growing up is also a significant drawback of the current system.

All these concerns were at the origin of the decision to proceed with a refurbishment of the current system.

The replacement of an already existing system under operation cannot be considered the same way as a new installation. Moreover, the refurbishment of the timing system takes place in the context of the EBS project [1] which involves the replacement of a large part of the existing accelerator during a long shut down scheduled in 2019.

It was clearly impossible, due to its present complexity, to replace the whole system in one move and to ensure operation at the same time. The new system had to be tested in a progressive way, outside user mode during specific allowable time, with restoration of the present cabling at each end of test.

It was thus decided to operate the transition in three phases:

1) Replacing the core "Bunch Clock" in order to solve the obsolescence issues as quick as possible. This phase was also necessary to check the retrieval of the current features and performances to allow the smooth operation of the accelerators.

2) Install the new system, flexible and scalable enough to be operated in parallel to the existing. This in order to allow an easier transition during operation.

3) Further extend the new system to Beamlines.

Another aspect to be carefully dealt with is the involvement in the project and the information of the different users, including the operators, and staff knowing about the current system, using it or having contributed to its development or continuous evolution. Efficient communication with these stakeholders is mandatory, in all phases of the project, from the specification until the operation phase.

In that respect, the ESRF set up a Working Group dedicated to the project and bringing together with the project manager, experts from the Accelerator division (RF, Diagnostics), the operation manager, the technical staff in charge of the new development (hardware, software) and engineers from the support teams.

In term of time schedule, the decision was made to decouple as far as possible this refurbishment from the new storage ring installation project. More precisely, the objective is to start operating at least part of the new timing system before the EBS shutdown, so to mitigate the risks at the restart in 2020.

Taking all constraints into account, the following planning was decided to set-up the refurbishment:

- Test and validation of a suitable technical solution.
- Replacement of the "Bunch Clock" module while preserving the existing cabling in order to definitely validate the technical solution. Preserve the possibility to switch to the old system as a backup during the validation process. The main goal is to have the new "Bunch Clock" running before the EBS long shut down.
- Installation of the whole new system in parallel to the existing during the EBS long shutdown.
- Restart the EBS with the validated synchronization system, then step by step replace the old cabling with the new one.

WHITE RABBIT BASED TECHNICAL SOLUTION

After an exploratory phase during which different solutions had been studied, the team made the decision to more deeply focus and evaluate one specific technical option based on the CERN White Rabbit Timing system [2][3]. White Rabbit can synchronize over 1000 nodes with sub-ns accuracy over optical fibre lengths of up to 10 km. These characteristics were ideal for the ESRF size and its time stamping requirements.

The whole ESRF synchrotron timing system is based on the 352 MHz RF, whereas WR only distributes UTC. Both clock domains are therefore fully asynchronous, and moreover, the RF is continuously trimmed around the 352 MHz value as the tuning parameter in the "fast orbit feedback" process.

The key element for eventually selecting WR as our technical solution was the availability of the so-called "RF over ETHERNET" (RFoE) feature based on the Distributed Direct Digital Synthesis (D3S or DDS) technology [4].

A SPEC mother board [5] equipped with an FMC-DDS mezzanine [6] implementing this technology, both available from the open hardware platform, made up the necessary setup for quick testing. Those boards are available from several manufacturers, which are listed on the same platform.

Thanks to a strong support from CERN, the RFoE function was refined to provide in phase locking of the distributed RF on all modules in a WR network. This allowed us to devise a consistent proposal for the new ESRF timing system.

The possibility to develop our custom solution in the Open Hardware environment [7] was also a strong incentive, combined with the flexibility offered by the SPEC FPGA.

The contemplated architecture for the ESRF system based on a WR network is shown Figure 2.

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUCPL01

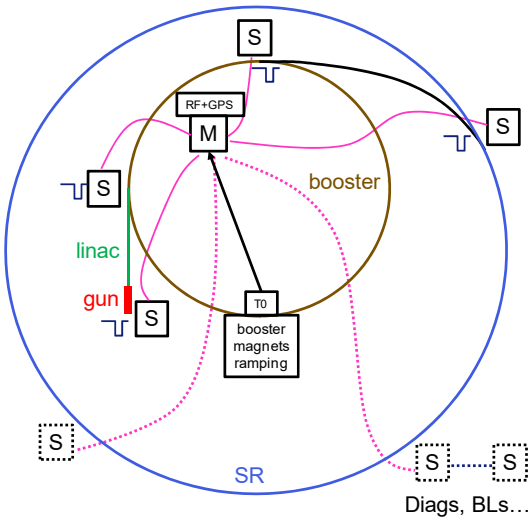

Figure 2: White Rabbit - ESRF Architecture.

The system is composed of several WR modules, one of those being a "master module" (M), while all the others are "slave modules"(S).

The modules are connected together through a dedicated White Rabbit network independent from other networks in the institute. Specific switches [8] can also be used to interconnect several modules to one fibre, if needed (WR switches are not shown in figure 2, for the sake of simplicity).

All WR modules are based on a SPEC board operated in standalone mode, coupled to a DDS mezzanine.

The master module is the one managing the analogue RF signal (352 MHz) and which receives the T0 trigger. Slaves can locally reconstruct both WR and RF time domains, and therefore duplicate the "Bunch Clock" sequencer with the same precision as in the master.

As proof of concept, we used a test vehicle made of three off-the-shelf SPEC boards associated with FMC-DDS blocks. Those boards were plugged to an already existing optical fibre network.

The master was directly connected to the RF source in the control room, while the T0 was provided by a 100 Hz generator (instead of the 4-10 Hz "true" T0 trigger). The two slaves were installed at maximum distance from the master, and programmed to deliver outputs from their locally duplicated sequencer. Outputs from both slaves were continuously cross-time-stamped, and recorded values continuously checked, along with corresponding values at master. The test ran for more than 6 months without fault.

This encouraging result led us to validate this technical solution and the development phase of the project was launched.

ESRF IMPLEMENTATION: WHIST

The main function of the synchronization and timing system is to deliver, site wide, an important number of programmable signals derived from the "Bunch Clock" sequencer.

The existing hardware (FMC-DDS mezzanine) provides only one single output.

It has been thus decided to develop a specific module, WHIST (White RabbIt Synchronisation and Timing), fitting ESRF needs. Its main characteristics are:

- Architecture based on a SPEC board coupled to a mezzanine card such as the FMC-DDS board.
- Implementation of the DDS function on a larger board than the standard FMC-DDS, with up to 12 programmable outputs. These outputs can be of two different types: either pulses with programmable delay and width or clocks with programmable phase. The new outputs are obtained by reallocating a few pins from the FPGA Mezzanine Card (FMC) connector located on the SPEC board, at the expense of increasing the on board I2C bus.
- The ESRF "Bunch Clock" sequencer and all associated logic from RF clock domain are implemented in the SPEC board FPGA. To fulfil our need in term of FPGA resources, a special version of the SPEC board, embedding a SPARTAN XC6S1X100T from Xilinx was necessary.
- A dedicated LM32 Softcore accessible through the Etherbone bus is implemented to manage application specific features like T0 broadcast, RF counters synchronization for all modules… This softcore is of the same kind as those used for the WR and RFoE protocols.

The SPEC board is used in standalone mode, i.e. without connection to the PCIe bus. The full control is achieved through the optical fibre. The programming of the FPGA –i.e. the flashing of its associated nvram- can also be performed via the WR network.

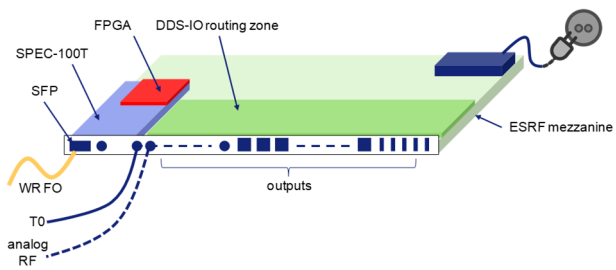

Figure 3: WHIST – overview.

The boards are embedded, together with a dedicated power regulator, in a 19 inch 1U case. The module can then easily be integrated in standard 19"cabinets at different locations of the institute, close to the equipment to be synchronised.

The current version of the WHIST module is designed to be easily interconnected to the existing timing system, in the idea to proceed to an incremental refurbishment. In that perspective, the electrical format of WHIST Inputs and Outputs are also compatible with what is in use in the existing system. WHIST (Figure 4) offers:

- One input dedicated to RF (used for the master module).

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUCPL01

- Four inputs (2xSMA; 2xLEMO) supporting time stamping in the RF or WR clock domains. In "master" configuration, one of these inputs is allocated to the T0.
- Two outputs delivering RF and RF/n clocks. n being programmable.
- 12 programmable outputs in ECL (sma) or TTL (lemo) formats. Some of the outputs are duplicated and available in both ECL and TTL.

Figure 4: WHIST module.

The pulses delivered by WHIST are programmable on the following parameters: polarity, width and delay with respect to T0, Injection or Extraction.

The architecture of the WHIST-based timing and synchronization system is detailed Figure 5.

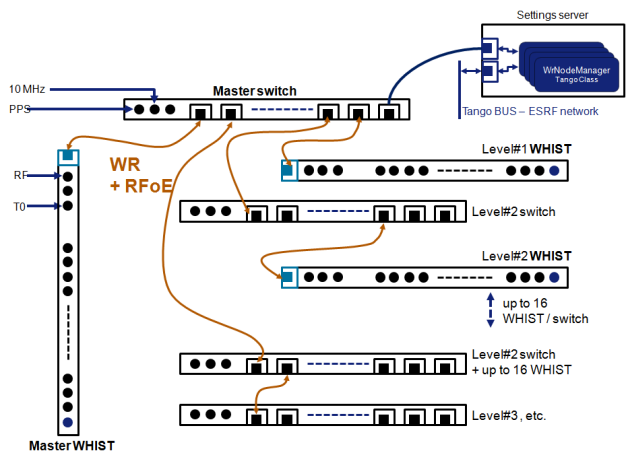

Figure 5: ESRF – considered WR network.

The master switch can optionally be connected to a GPS or any other reference source for UTC. The WR network can be extended, as needed, with the use of several switch levels (3 levels shown on Figure 5).

The master WHIST (and only this module) receives RF and T0. In phase RF is distributed over the network through the DDS hardware implemented in all modules. All slaves run the same "Bunch Clock" sequencer in phase with the master.

The typical T0 sequence is:

- Booster magnet power supply issues a T0 trigger at start of ramping. The delay for the booster acceleration energy to match the LINAC output energy is 1.5 ms minimum. This value (T0_delay) is programmed and broadcast in all slaves as part of the general system configuration.
- During the T0_delay, the master WHIST stamps T0 with its internal RF counter (T0_stamp) and broadcasts this stamped value over the network. Slaves can then compute "T0_stamp + T0_delay" in order to get ready for the injection start.

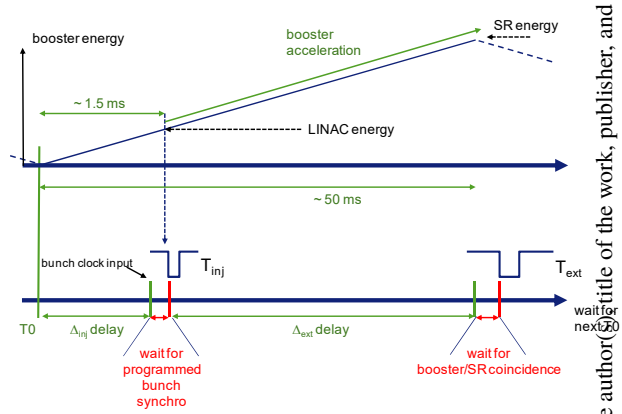

Figure 6: WHIST - typical T0 sequence.

- When all RF counters over the network match the computed "T0_stamp + T0_delay" value, all "Bunch Clock" sequencers start in phase and programmed pulses are locally delivered in due time.
- All sequencers run in parallel up to the extraction phase and "end of sequence" and then get ready for the next T0.
- If an output is programmed to deliver a clock instead of a sequencer related pulse, the clock phase can be adjusted.

The control of the whole system is performed through a Server which has a network interface connected to the grandmaster switch and another one connected to the ESRF network (Figure 5). The control system, TANGO based, interfaces and manages WHIST modules through the White Rabbit Network.

It allows at least the following operations:

- Management of correspondence between MAC and IP for all modules on the WR network embedding a SPEC board
- Configuration of the sequencer parameters
- Configuration of Master and Slave modules outputs
- Update of firmware of modules when needed
- System monitoring / RF consistency over the network

The Human Machine Interface of the Timing system is also being refurbished and will offer to the users and operators a new interface. On top of the configuration features listed above, the control system is also designed to offer a diagnostic and supervision module to be used during operation.

FIRST RESULTS & PERSPECTIVES

The first prototypes of WHIST modules were made available in the last quarter of 2016.

Phase noise measurements have been carried out with a RHODE & SCHWARTZ FSUP analyser on the reconstructed RF and other clocks. Results are all around 10 ps or less. The final performance will be evaluated on a next WHIST version under development. This version will implement a replacement of the currently used VCXO and its associated PLL for RF reconstruction.

A basic setup involving a Master WR switch, a Master WHIST and one Slave WHIST has been successfully connected to the ESRF accelerator during a "Machine

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUCPL01

Dedicated Time". We were able to inject bunches in the storage ring, in several modes, and using the new Tango control system.

More tests are still required to implement all storage ring filling patterns, check compatibility with more diagnostic equipment etc... The results obtained and the progresses in the project make us confident that our objective of running the accelerator with a new bunch clock in 2018 is reachable.

CONCLUSION

The ESRF has initiated the refurbishment of its obsolescent accelerator timing system. The new system which is being developed is based on the White Rabbit solution, developed by CERN. A specific module, WHIST, is being designed to that purpose. The first tests, including connection with the real machine, are positive and our goal remains to be ready with the core of the new system in user mode before ESRF EBS shutdown.

ACKNOWLEDGEMENT

The ESRF team would like to expressively acknowledge and deeply thank the CERN colleagues of the Hardware and Timing section for their very efficient support. Special thanks to Javier Serrano and T. Włostowski for the time they have dedicated to our project and for having made possible the use of White Rabbit for the synchronisation of Synchrotron Sources.

REFERENCES

[1] http://www.esrf.fr/about/upgrade

[2] https://www.ohwr.org/projects/white-rabbit

[3] J. Serrano, M. Cattin, E. Gousiou, E. van der Bij, T. Włostowski, G. Daniluk, M. Lipiński, "The White Rabbit Project" IBIC2013, Oxford, UK (2013)

[4] T. Włostowski, G. Daniluk, M.M. Lipinski, J. Serrano, and F. Vaga, "Trigger and RF Distribution Using White Rabbit", in *Proc. 15th Int. Conf. on Accelerator and Large Experimental Physics Control Systems (ICALEPCS'15)*, Melbourne, Australia, October 2015, paper WEC3O01, pp. 619-623, ISBN: 978-3-95450-148-9, doi:10.18429/JACoW-ICALEPCS2015-WEC3O01, 2015.

[5] https://www.ohwr.org/projects/spec/wiki

[6] https://www.ohwr.org/projects/fmc-dac-600m-12b-1cha-dds/wiki

[7] J. Serrano. Open Hardware and Collaboration. PCaPAC, 2016.

[8] https://www.ohwr.org/projects/wr-switch-hw/wiki