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CONCEPT OF CAVITY SIMULATOR FOR EUROPEAN SPALLATION SOURCE*

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Abstract

At the European Spallation Source it is foreseen to use around 120 superconducting cavities operating at 704.42 MHz. Each cavity will require an individual LLRF control system, that needs to be tested before the installation inside the accelerator.

Testing of all systems using the real superconducting cavities would be very expensive and in case of a failure can lead to serious damages. To lower the testing cost and avoid potential risks it is planned to design and build a device that simulates the behavior of a superconducting cavity.

The cavity simulator will utilize fast data converters equipped with an RF front-end and a digital signal processing unit based on a high performance FPGA. In this paper conceptual design of hardware and firmware will be presented.

INTRODUCTION

Polish Electronics Group is a consortium of 3 Polish scientific institutes: National Centre for Nuclear Research, Warsaw University of Technology and Łódź University of Technology. It was established in order to contribute to the European Spallation Source project as an in-kind partner. PEG is responsible for assembly and installation of the LLRF control systems for superconducting elliptical cavities used in medium and high beta sections of the ESS linac. The consortium will also design and manufacture the following components of the systems: LO RTM, Piezo Driver, RTM Carrier and Cavity Simulator. [1].

The Cavity simulator is a device foreseen to test the LLRF control systems before they are commissioned in the accelerator. It simulates a behavior of a superconducting cavity together with a klystron/IOT RF power amplifier. The block diagram of the system simulated by the device is presented in Fig. 1 [2].

Basing on the input signals (RF drive and piezos' drive), the Cavity Simulator generates the following output signals:

- amplifier input,
- amplifier forward,
- amplifier reflected,
- cavity forward,
- cavity reflected,
- cavity probe,
- amplifier power supply modulator,
- piezo sensor.

The model of the cavity is implemented in a digital signal processing unit. Among others, the device simulates the following phenomena: cavity detuning, piezo compensation, Lorentz force detuning, beam current and influence of the amplifiers power supply modulator.

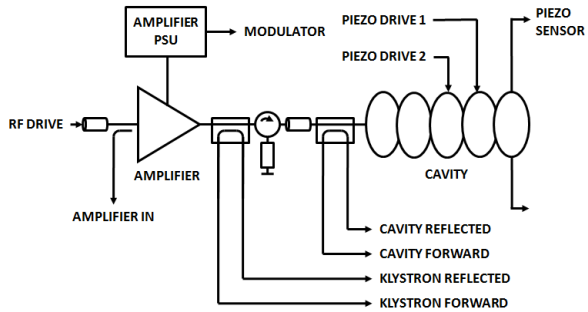

Figure 1: The block diagram of the system simulated by the Cavity Simulator

To operate with analog signals a set of data converters with a dedicated front-end is provided. The device is controlled remotely by a PC. The simplified concept of the Cavity Simulator is presented in Fig. 3.

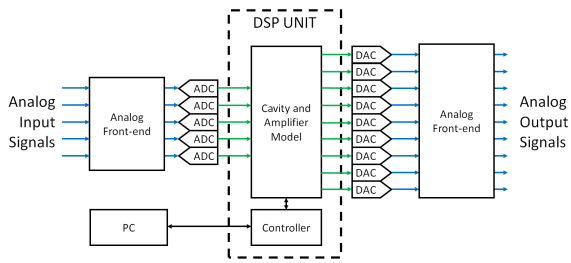

Figure 2: The simplified block diagram of the Cavity Simulator.

REQUIREMENTS

Based on the presented architecture and the specification of ESS LLRF control system a set of requirements for the Cavity Simulator was prepared.

The device shall operate at 704.42 MHz, the same reference frequency as the ESS LLRF control systems for medium and high beta cavities.

Three analog inputs are required: one for the RF drive signal and two for high voltage piezo actuator signals. The RF input must accept the maximum output power of a vector modulator module used in the ESS LLRF (Struck DWC8VM1 RTM). The maximum level of piezo driver input shall be ±100V. To simulate the impedance of the piezo actuator, each high voltage input shall have 2.2 uF input capacitance.

The Cavity Simulator shall have eight analog outputs: six RF outputs for the amplifier and the cavity signals, one for

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the amplifier power supply modulator and one for the piezo sensor. Each RF output shall have the maximum output power of +15 dBm, matching the input levels of the down-converter channels of the Struck DWC8VM1. The maximum output level of the power supply modulator output shall be ±1V. The piezo sensor output shall deliver ±10V signal and must be protected against the ±100V voltage.

The device shall be controlled remotely by a PC computer. The communication shall be realized using USB interface or Ethernet network.

The expected latency introduced by the cabling between the RF drive and the cavity probe in the real system is 350 ns [3]. This signal processing time of the Cavity Simulator shall be not greater than this value.

HARDWARE

The Cavity Simulator digitizes the RF drive and piezo signals coming from the LLRF control system. The signals are then processed by a DSP unit. The output signals are then converted to the analog format and they are fed back to the control system.

There are several ways to digitize the RF signals. Most common approaches are:

- direct sampling,
- analog IQ demodulation (Zero IF),
- down-conversion.

Each of this solutions require a dedicated analog front-end. The simplest circuit is needed for the direct sampling scheme, but it is also the most sensitive to the clock signal phase noise. Analog IQ demodulation needs two ADCs and is subject to a DC offset error. The down-conversion scheme requires the most complex analog frontend and generation of additional heterodyne (LO) signal, but offers the best performance, so it will be used in the design. Apart from the RF drive signal, the reference signal also must be digitized in order to be used as a phase reference for the firmware.

The simplest way to generate an RF signal is to use a DAC with a sampling frequency at least twice higher than output signal. For this application it means using data converter with sampling rate higher than 1500 MSPS. Such devices are available on the market and have integrated numerically controlled oscillators, that limit the required input data rate. Unfortunately, their digital latency is too high and they are not suitable for this application.

The other way to generate an RF signal is to modulate the reference signal with a vector modulator. This circuit requires two DACs to generate the base-band signals and a reference signal. In this solution converters with lower overall latency can be used.

The piezo and modulator signals can be generated and digitized directly by standard data converters. The piezo input, due to high voltage, requires additional protection circuit.

Based on the device requirements and the approach presented above, the block diagram of the Cavity Simulator hardware was prepared. It is presented in Fig. 3.

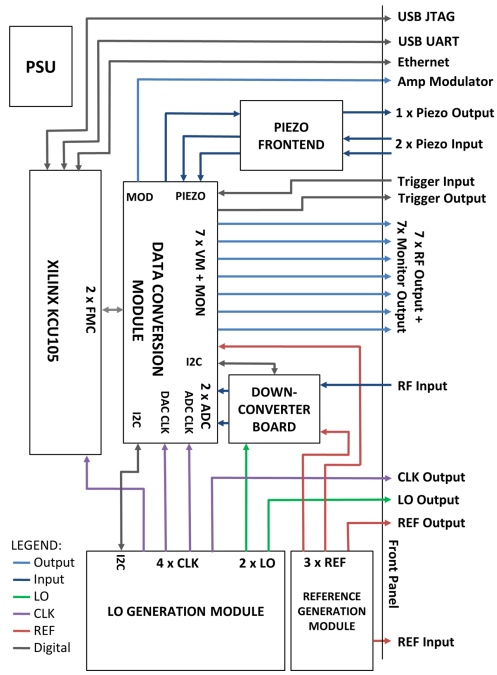

Figure 3: The block diagram of the Cavity Simulator Hardware

The Cavity Simulator is build from 7 different modules. Functionality and roles of the main components are presented below.

FPGA Processing Module

The FPGA Processing Module gathers the data from the ADCs, performs digital signal processing and feds the data to the DACs that generate the analog output signals. The module is also responsible for the control over the Cavity Simulator and communication with a PC.

To reduce the development time and cost it was decided to use an off-the-shelf FPGA module. KCU105 board from Xilinx was selected. Among others, it is equipped with a high performance Kintex Ultrascale FPGA, 2GB DDR4 RAM and 2 FMC connectors, which are used to connect with the Data Conversion Module.

Data Conversion Module

The Data Conversion Module is used to digitize and generate analog signals. All data converters used in the Cavity Simulator are integrated into this module. It is also used as a communication bridge between FPGA Processing Module and all other modules.

The RF drive and the reference signals require two channel down-converter circuit. It is included in the separate module, because it was decided to design the Data Conversion Module as wide-band as possible and the down-converters typically operate in very limited frequency range. The output signals from the down-converter are digitized by a dual channel, 16 bit 250 MSPS ADC.

Unlike the down-converter, it is relatively simple to design a wide bandwidth vector modulator. Therefore, it can

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be integrated into the Data Conversion Module. Another reason for integration of the vector modulator circuit and base-band DACs in a single board, is that any mismatch between the analog I and Q signals paths will highly affect the intermodulation performance. Six vector modulators are needed for the Cavity Simulator project, but additional 7th channel was added. It can be used for design debugging or generation of another, not yet specified, signal.

In order to reduce the risk of damaging the cavity simulator by a high voltage coming from the piezo driver, it was decided to build the piezo front-end as a separate module. Two 5 MSPS ADCs are used to digitize the piezo driver signal. Piezo sensor and modulator signals are generated using two 16 bit 125 MSPS DACs.

To control all circutis in the module a low cost FPGA is used. It communicates with all other devices through I2C and SPI buses and buffers the data between the FPGA Processing Module and the data converters used for piezo and modulator signals.

The block diagram of the Data Conversion Module is presented in Fig. 4.

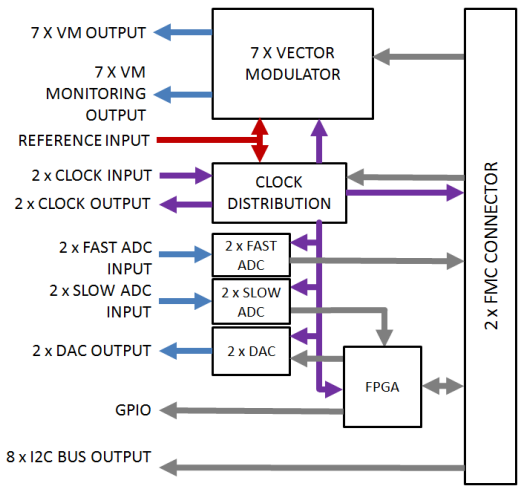

Figure 4: The Block Diagram of the Data Converters Module

LO Generation Module

The LO Generation Module is responsible for the generation of the LO and clock signals used across the device. The planned clock frequency is 117.4 MHz. Two possible IF frequencies are considered: 23.48 and 29.35 MHz.

This module utilizes the same direct analog generation scheme as the one used in the LO RTM designed by PEG. It is described further in [4].

Reference Generation Module

The Reference Generation Module distributes the reference signal. It can operate in two modes, either external signal can be distributed or the reference signal can be generated locally by an integrated PLL.

The performance of the PLL circuit, which is based on Texas Instruments LMX2592 chip, was measured using an evaluation board. The phase noise spectrum of the output reference signal is presented in Fig. 5. The jitter integrated in the 10 Hz to 1 MHz band equals 264 fs. This phase noise level should be sufficient for the functional tests of the LLRF control systems.

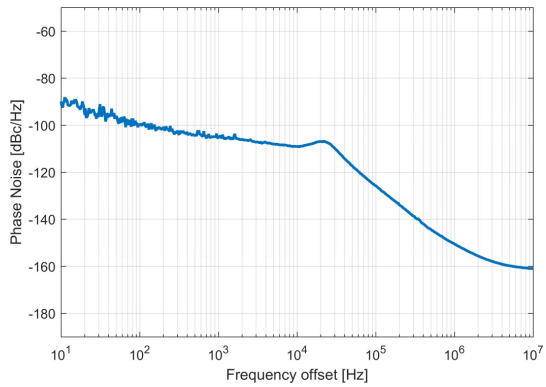

Figure 5: The expected phase noise spectrum of the signal generated by the Reference Generation Module.

FIRMWARE

The main part of the firmware is the simulation model. The input signals comes from the ADCs on the Data Conversion Module. The data processing is performed on the data in the vector format, so the first stage is the digital IQ demodulation. Depending on the IF frequency IQ or non-IQ sampling schemes can be used. The non-IQ scheme is preferred, because of the reduced effect of the higher order harmonics [5]. However, due to more complex calculations it adds additional latency to the signal processing path.

The first modeled element is the amplifier. It generates the amplifier's forward and reflected signals. It requires additional power supply modulator signal, which is generated inside the firmware, based on the user predefined sample table. This signal is also send to the DAC, that generates the analog output signal.

The next element is the cavity model. It is fed with the amplifier forward, beam current and detuning calculation signals. Based on those signals, cavity probe, forward and reflected signals are calculated. Basing on the information from the cavity and a piezo models the detuning value is calculated and the piezo sensor signal is produced.

The beam signal is generated as a custom waveform, so different currents can be simulated. The phase of the beam is related to the phase of the reference signal, so it remains constant with the changes of the RF drive signal.

To synchronize the Cavity Simulator with LLRF control system a synchronization signal is required. External signal can be used or it can be generated locally from the reference signal. It is fed to the blocks that generate the modulator and beam signals.

For the purpose of testing the Cavity Simulator, a simple LLRF controller, arbitrary waveform generators and data acquisition system are provided. This tools can be used to

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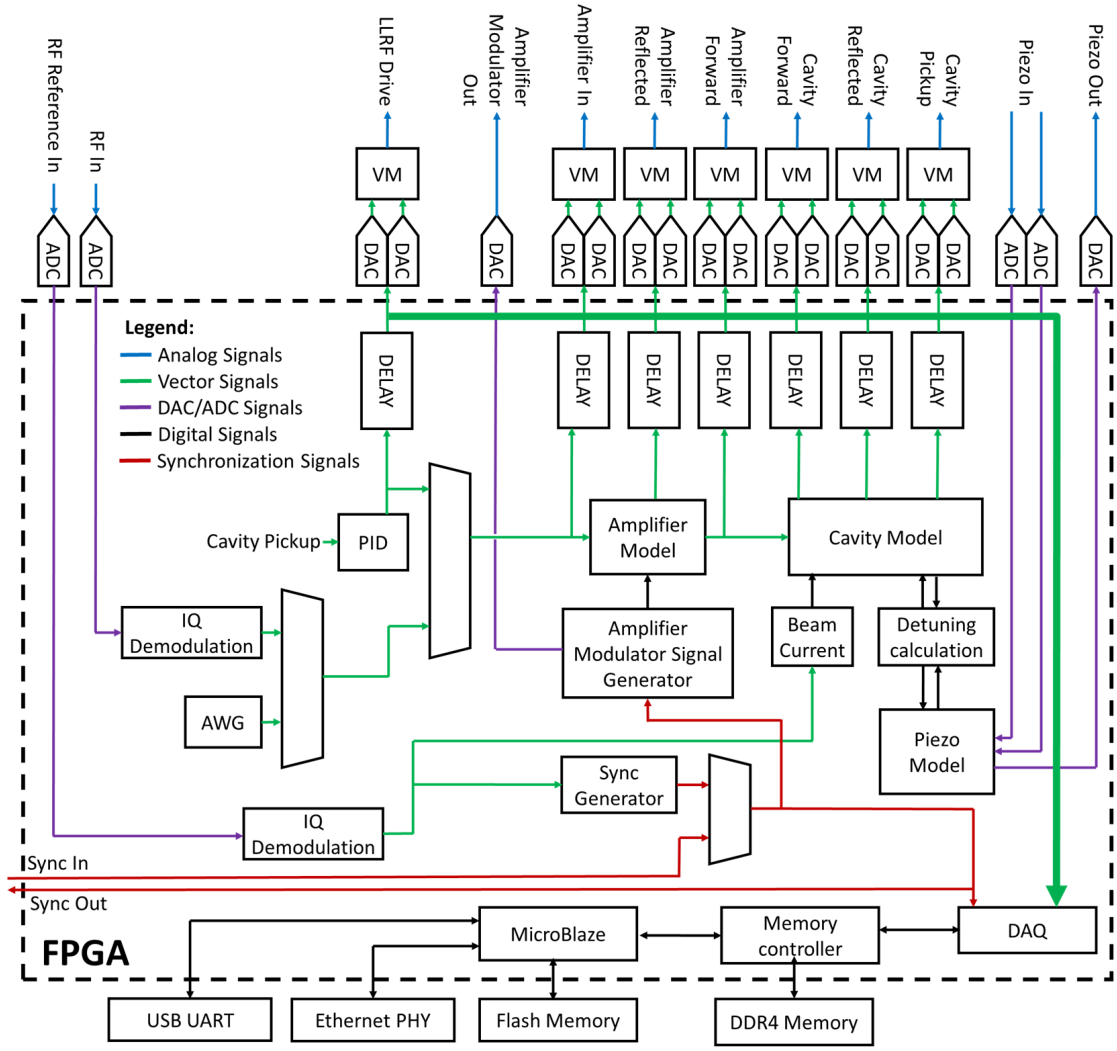

Figure 6: The block diagram of the Cavity Simulator firmware.

verify the proper operation of the device and will simplify the development.

To control the device Xilinx MicroBlaze softcore processor is used. It is responsible for the interpretation of the control commands sent to the device, setting the model parameters and transmission of acquired data.

A simplified block diagram of the Cavity Simulator firmware is presented in Fig. 6.

SUMMARY

In this paper the concept of the Cavity Simulator design was presented. The overview of the hardware, together with the description of the most critical components and the planned firmware were shown.

The device is currently in the hardware development stage. It is planned to finnish this part of the project by the end of 2017.

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