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THE INTERLOCK SYSTEM OF FELiChEM*

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Abstract

FELiChEM is an infrared free-electron laser user facility under construction at NSRL. The design of the interlock system of FELiChEM is based on EPICS. The interlock system is made up of the hardware interlock system and the software interlock system. The hardware interlock system is constructed with PROFINET and redundancy technology. The software interlock system is designed with an independent configuration file to improve the flexibility. The test results of the prototype system are also described in this paper.

INTRODUCTION

Tunable Infrared Laser for Fundamental of Energy Chemistry (FELiChEM) is the significant scientific instrument which is approved by the National Natural Science Foundation of China in 2013 [1]. FELiChEM contains one state-of-the-art infrared free electron lasers, one 60MeV linac and three research stations: photo-detection, photo-ionization, and photo-excitation setups.

EPICS is a set of software tools for building distributed control systems to operate devices such as Particle Accelerators and Large Experiments. For accelerator, the interlock system takes the charge of machine protection and the personal protection. As we adopted EPICS to establish the control system in FELiChEM, we also design the interlock system based on EPICS. This system comprises of the hardware interlock system and the software interlock system. The hardware interlock system has two parts: Machine Protection System (MPS) and Personal Protection System (PPS). We adopt redundancy technology and PROFINET to improve the reliability in the hardware interlock system. In the design of the software interlock system, we use an independent configuration file to improve the flexibility.

HARDWARE INTERLOCK SYSTEM

In the hardware interlock system of FELiChEM, the requirement of response time is about 100ms. We use PROFINET for field communication. PROFINET is an industrial internet standard. Depending on the PROFINET definition, it has PROFINET IO controller layer and IO device layer. For the hardware interlock system, PLC is the controller for dealing with interlock logic. Meanwhile, the distributed IO stations are the IO devices to get field signal and achieve interlock action. IOC is used to integrate the hardware interlock system into EPICS environment.

As shown in Figure 1, the IOC layer, PROFINET IO controller layer and PROFINET IO device layer form the three-layer interlock system architecture. Each layer is separate and can be configured in redundant mode. Furthermore, the link media between IO controller layer and IO device layer can also adopt redundant technology.

IOC layer includes master IOC and slave IOC which are running on the VMware virtual machines (VM). The two VMs use Fault Tolerance (FT) mechanism to achieve redundant function. VMware FT achieves zero downtime and zero data loss by creating exactly the same VM from the master VM. The master VM and the slave VM use heartbeat mechanism for monitoring mutual status. So when the master VM shutdown, the slave VM can take it works over as a redundant function implementation [2].

The PROFINET IO controller layer uses a pair of redundant Phoenix RFC 460R PLCs. The master PLC and the slave PLC synchronize data via fiber. They can switch roles with each other. IOC communicates with master PLC by Ethernet, and the corresponding driver is developed via TCP/IP protocol [3]. PROFINET supports three types of protocol: TCP/IP, Real-Time (RT) and Isochronous Real-Time (IRT). In FELiChEM interlock system, we use RT protocol between the controller layer and the device layer.

We also set up redundant network link media topology based on Rapid Spanning Tree Protocol (RSTP) to improve the reliability. RSTP can provide network path redundancy.

PROFINET IO device layer has several IO stations, and each station has several IO modules. IO device layer divides into MPS and PPS. MPS part includes 8 sub-systems: electron gun, vacuum, power, modulator, microwave, cooling water, undulator and resonant cavity. PPS includes access control system, check button, emergency stop button and dose measurement alarms. In the hareware interlock systelm of FELiChEM, we haven't use redundancy configuration in IO device layer.

TEST OF PROTOTYPE HARDWARE INTERLOCK SYSTEM

Response time and redundant switch-over time are the key parameters in the hardware interlock system. We establish a prototype system for measuring these parameters.

In the prototype system, the PROFINET IO devices layer has two IO stations for simulating MPS and PPS separately. Each station has one 16-channels DI module and one 16-channels DO module. Figure 2 is the operator interface developed with Control System Studio(CSS).

We use two Phoenix SMCS 8TX industrial switches for setting up the PROFINET network, and it can support RSTP protocol.

Test of Response Time

The response time refers to the time difference between IO station receiving input DI signal and setting interlock DO

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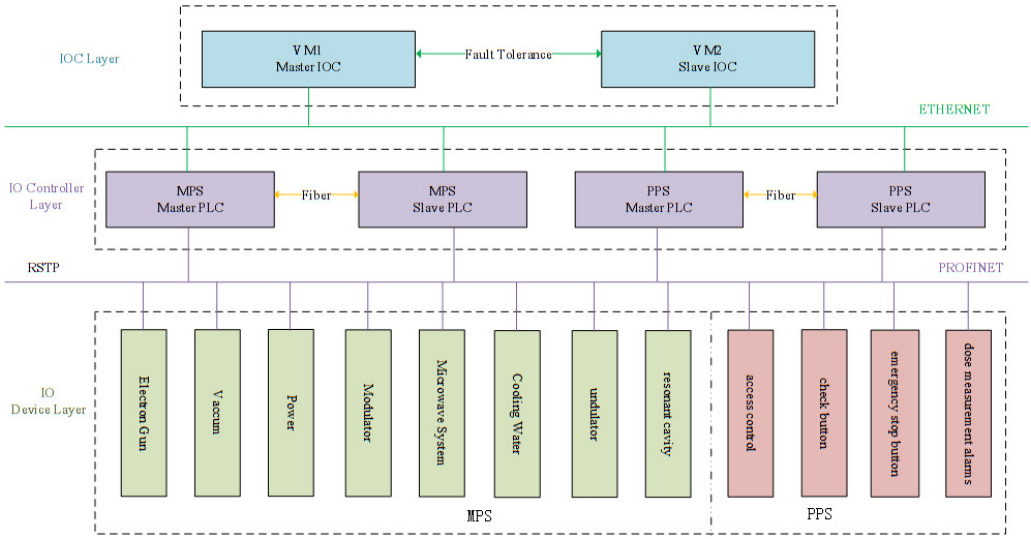

Figure 1: Architecture of the Hardware Interlock System.

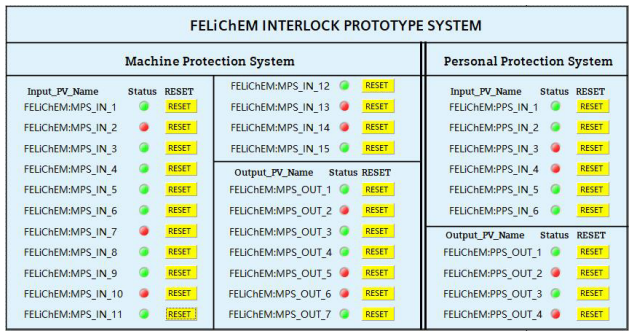

Figure 2: The Operator Interface of Prototype System.

signal out. We use the oscilloscope to measure DI and DO signals for getting the response time. As shown in Figure 3, the test result is about 6ms.

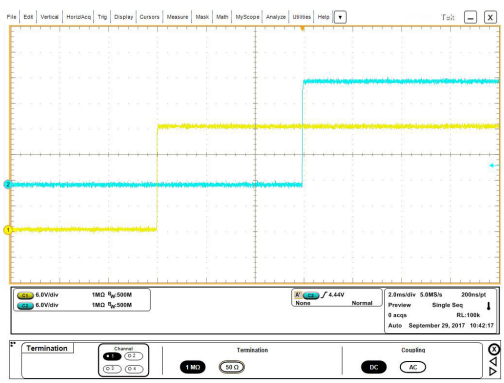

Figure 3: The Response Time Test Result by Oscilloscope.

Test of Switch-Over Time

The switch-over time refers to the PLC switch-over time. When PLCs communicate with IO stations, they use the flag in frames to distinguish the master PLC and slave PLC. So the PLC roles switch can be interpreted identified from the captured frames by Wireshark. The average test result is 6.229ms.

According to the test results, the response time and the PLC switch-over time are all much shorter than requirement in FELiChEM hardware interlock system.

SOFTWARE INTERLOCK SYSTEM

Compared to hardware interlock system, software interlock system is more flexible and configurable [4]. Thus we also design the software interlock system as a necessary supplement in low response time condition.

In software interlock system, we use the independent configuration file to define the interlock logic. We develop interlock program by using Python to read the Process Variables (PVs) in EPICS database, then it explain the configuration file and executes corresponding interlock logic. Configuration file stores different interlock logic by JavaScript Object Notation (JSON). Be similar to Extensible Markup Language (XML), JSON is a kind of more lightweight language [5].

Figure 4 displays the test JSON configuration file. In each interlock unit, it defines a monitor list and an action list. Input PVs is contained in Monitor list. "*compare_operator*" and "*design_value*" is used to set up the relevant parameter. In action list, we use "*set_point*" and "*delay_time*" to set specific interlock actions.

```
{
  "interlock_unit":{
    "monitor_list":[
       { "pv_name":"PV_IN_1","compare_operator":">=","design_value":4},
       { "pv_name":"PV_IN_2","compare_operator":"==","design_value":3}
    ],
    "action_list" : [
       { "action" : "set", "pv_name" : "PV_OUT_1","set_point" : 0 },
       { "action" : "delay", "delay_time" : 5},
       { "action" : "set", "pv_name" : "PV_OUT_2", "set_point" : 0.5 }
    ]
  }
}
```

Figure 4: JSON File of Software Interlock System.

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Figure 5 is the flow chart of software interlock system. After program start, it will process interlock logic in monitor list according to the JSON file. If all the process results are true, the program will read action list and process interlock action.

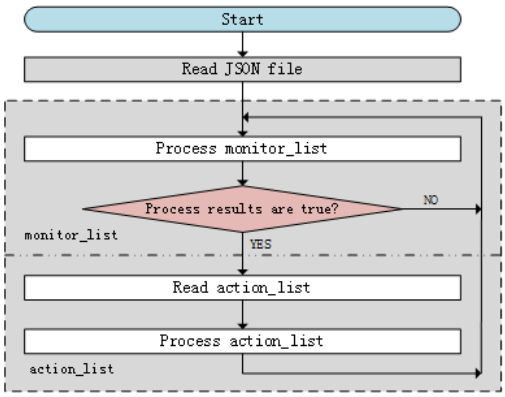

Figure 5: Flow chart of Software Interlock System.

Figure 6 is the result of the example. When *PV_IN*_1 is greater than or equal to *4* and *PV_IN_2* is equal to *3*, program executes interlock action as the setting of action list. First it sets *PV_OUT_1* to *0*, then after 5 seconds *PV_OUT_1* is set to *0.5*.

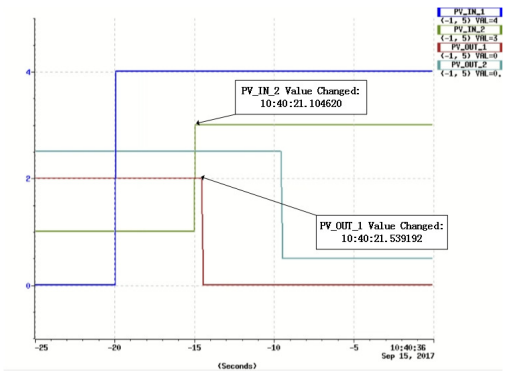

Figure 6: Execution Result of Soft Interlock System.

By the "camonitor" command, we test the response time of software interlock system. The jump time has also been marked in Figure 6. The test result is 434.572ms. Comparing the response time (6ms) of hardware interlock system, software interlock system is obviously slower.

CONCLUSION

We describe the design of FELiChEM interlock system under the EPICS framework. We design the hardware interlock system based on PROFINET, including the IOC layer, PROFINET IO controller layer and PROFINET IO device layer. Based on the prototype system, the response time is 6ms, the switch-over time of PLC is 6.229ms. All the results meet the design requirement. As a necessary supplement, we design the software interlock system to increase flexibility which separates interlock program and configuration files.

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