Design and Implementation of the Fast Protection System for CSNS

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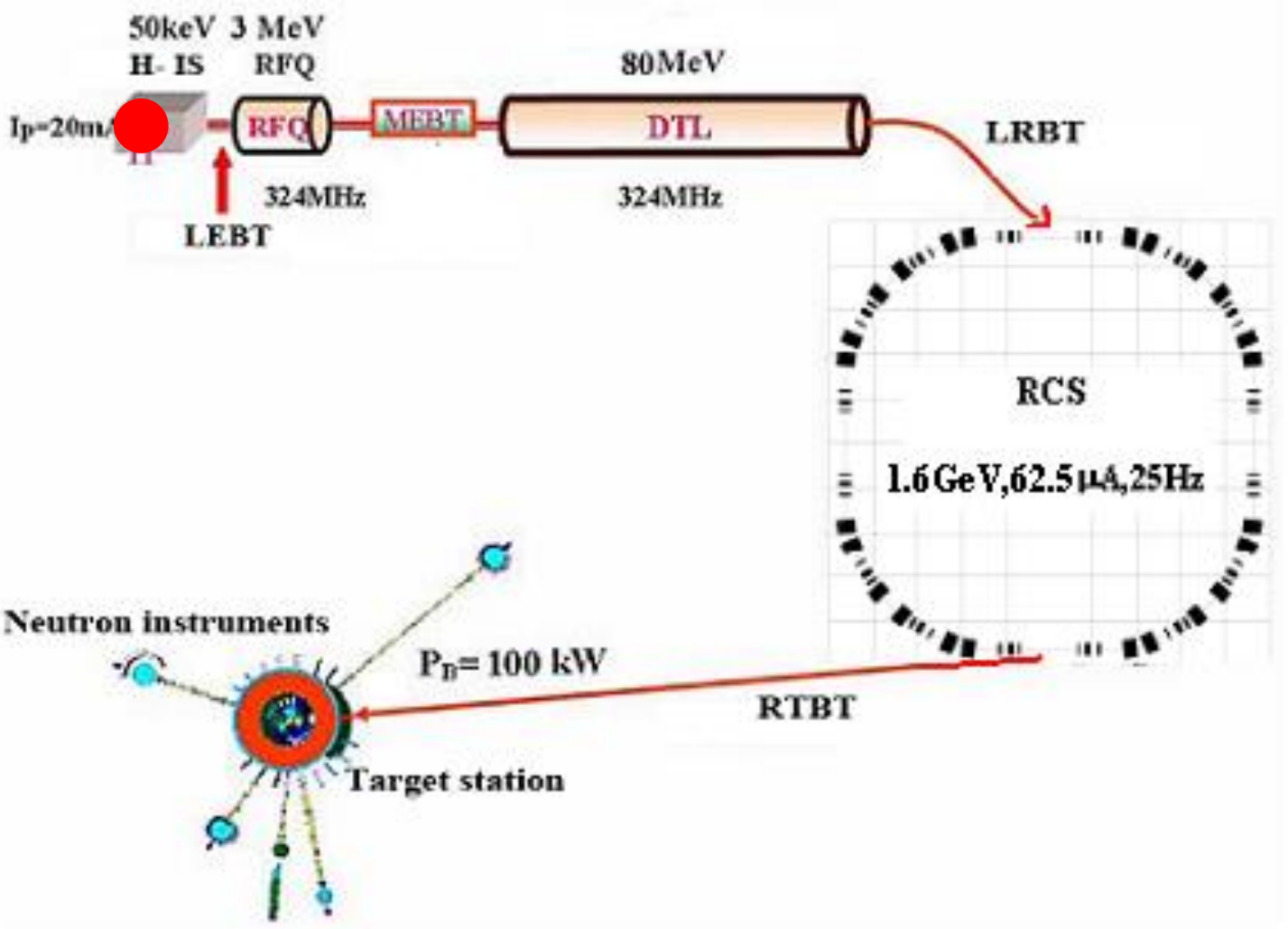
Outline

- Brief introduction to CSNS (China Spallation Neutron Source)
- Fundamental safety requirements
- Basic design considerations and rules
- Overall design
- Design and implementation of FPS(Fast Protection System)

Outline

- Next to do
- Summary

Brief introduction to CSNS



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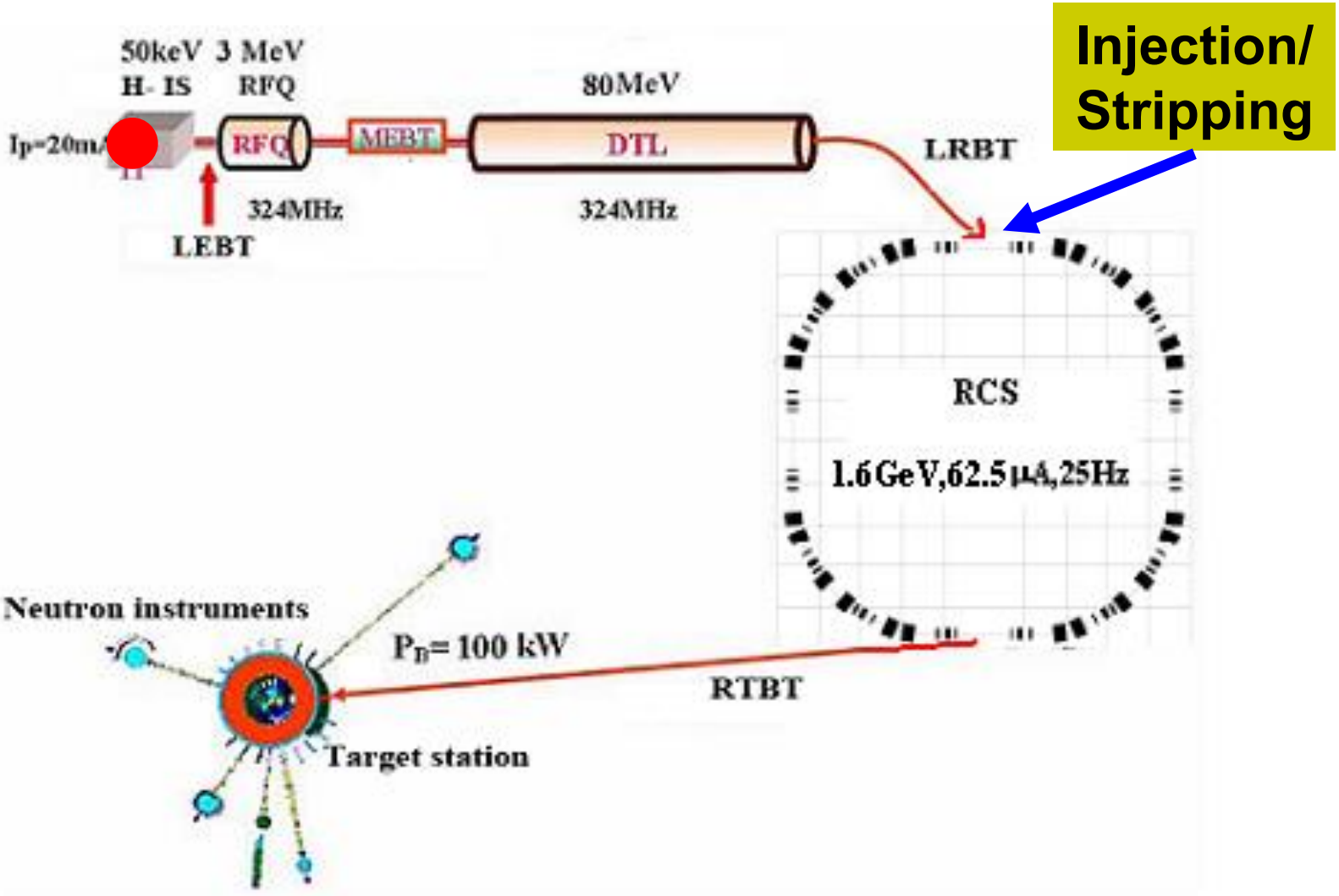

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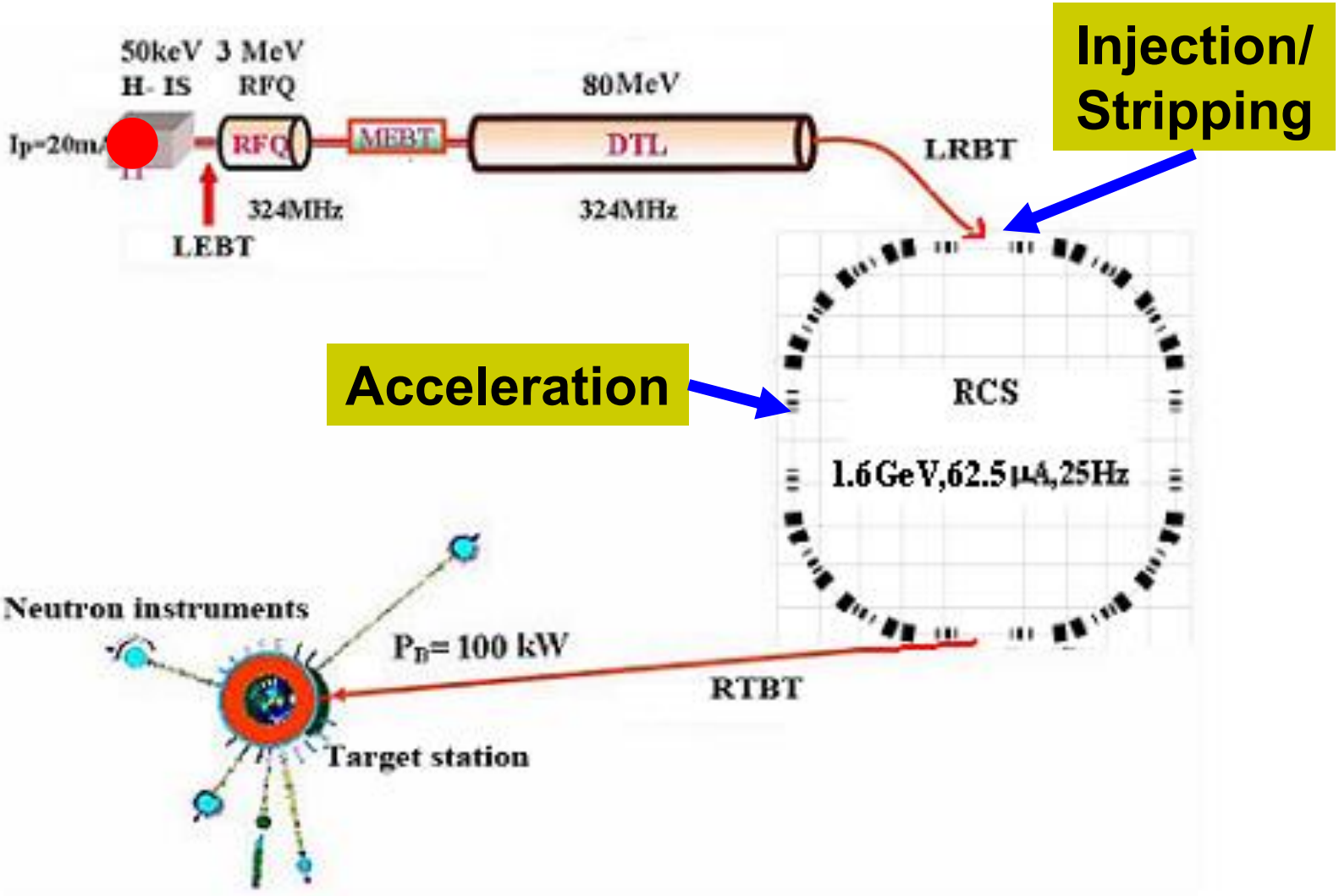

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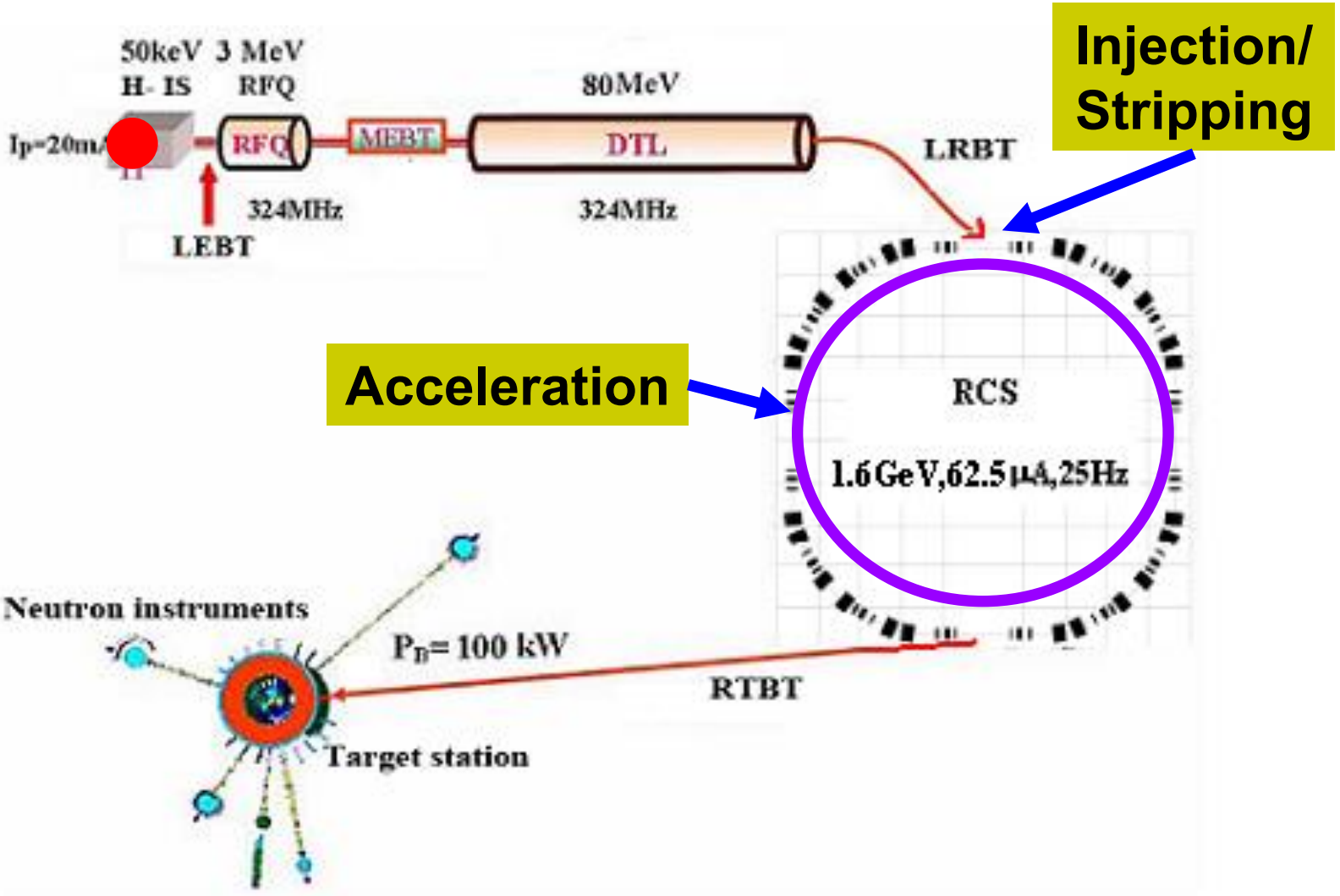

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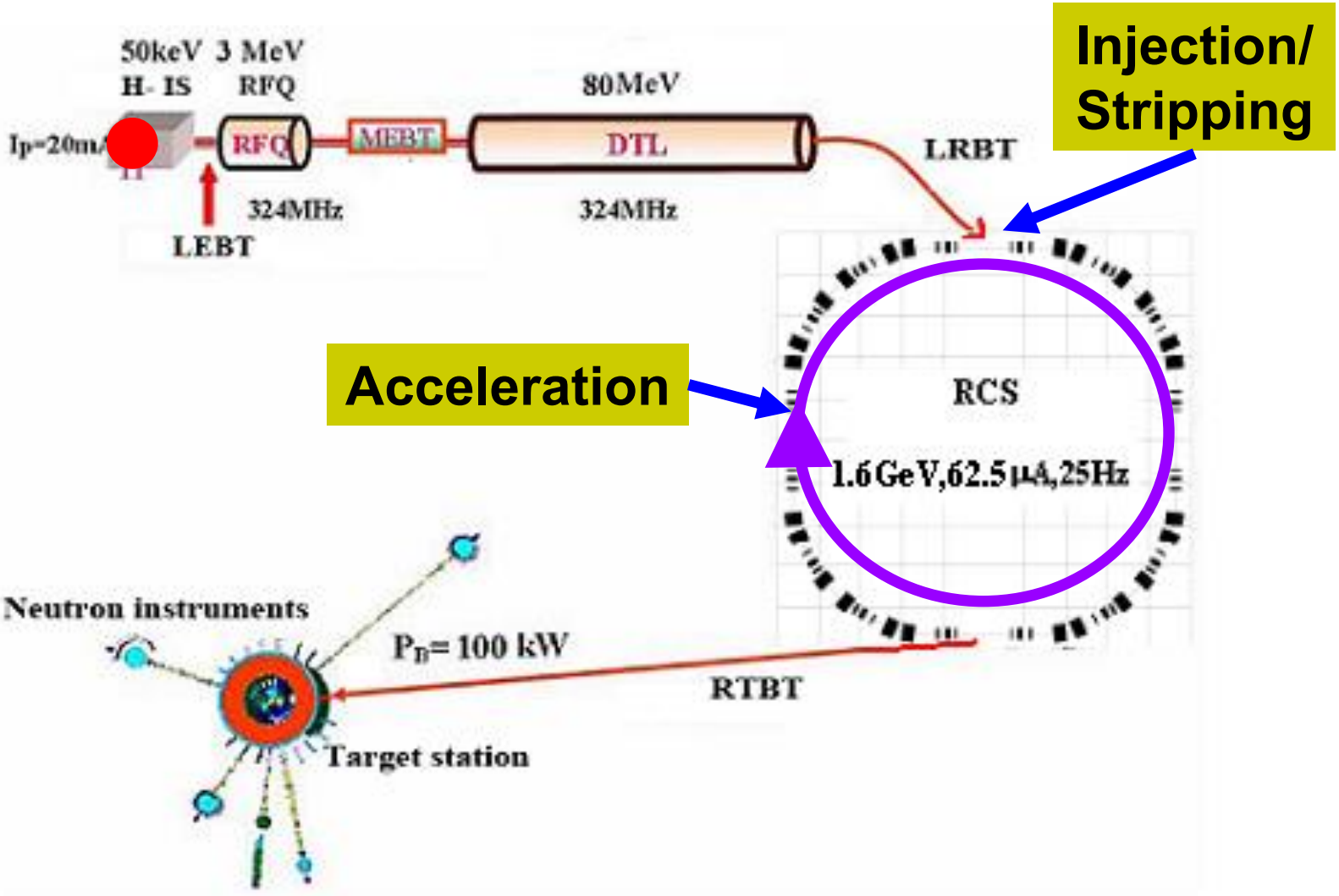

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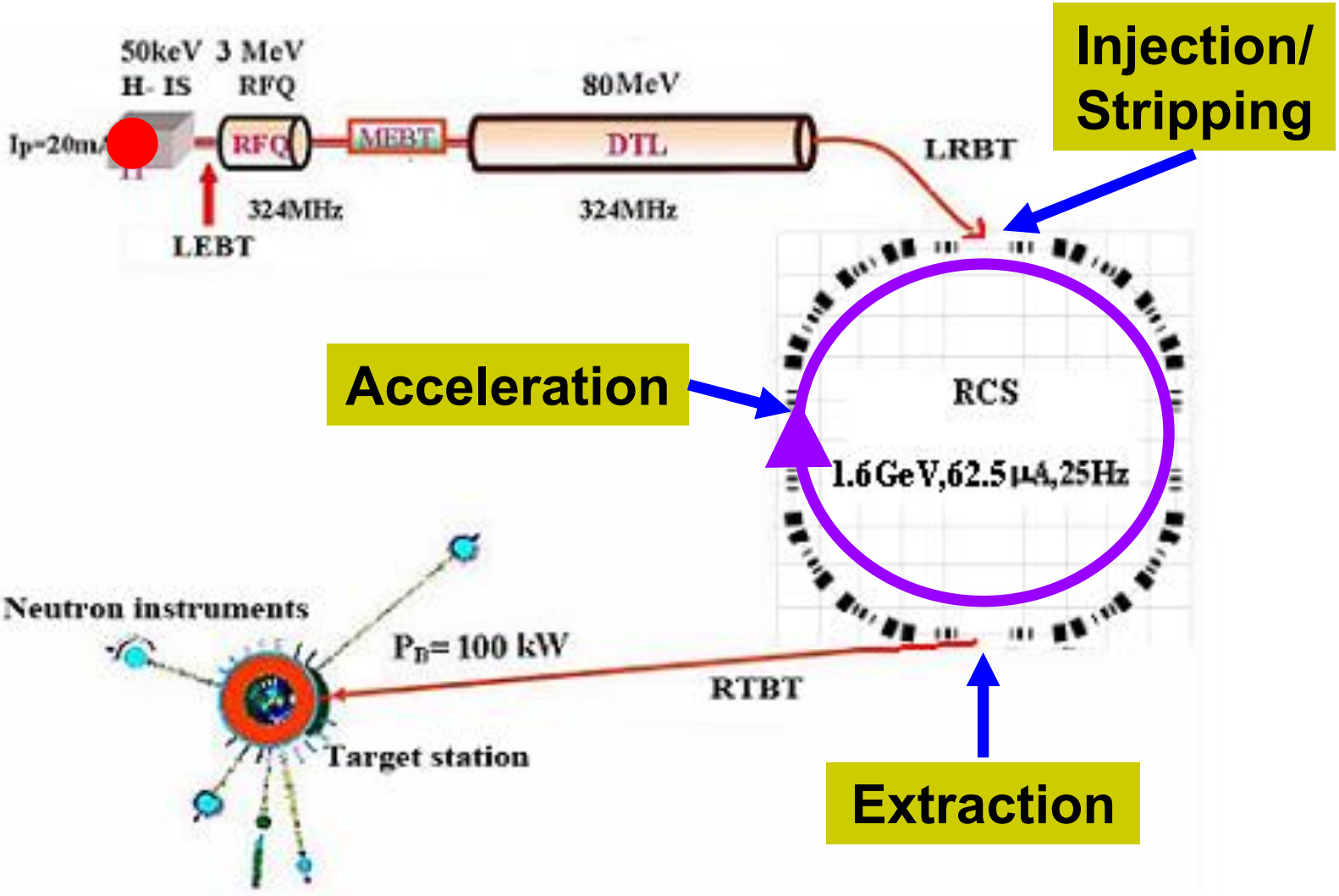

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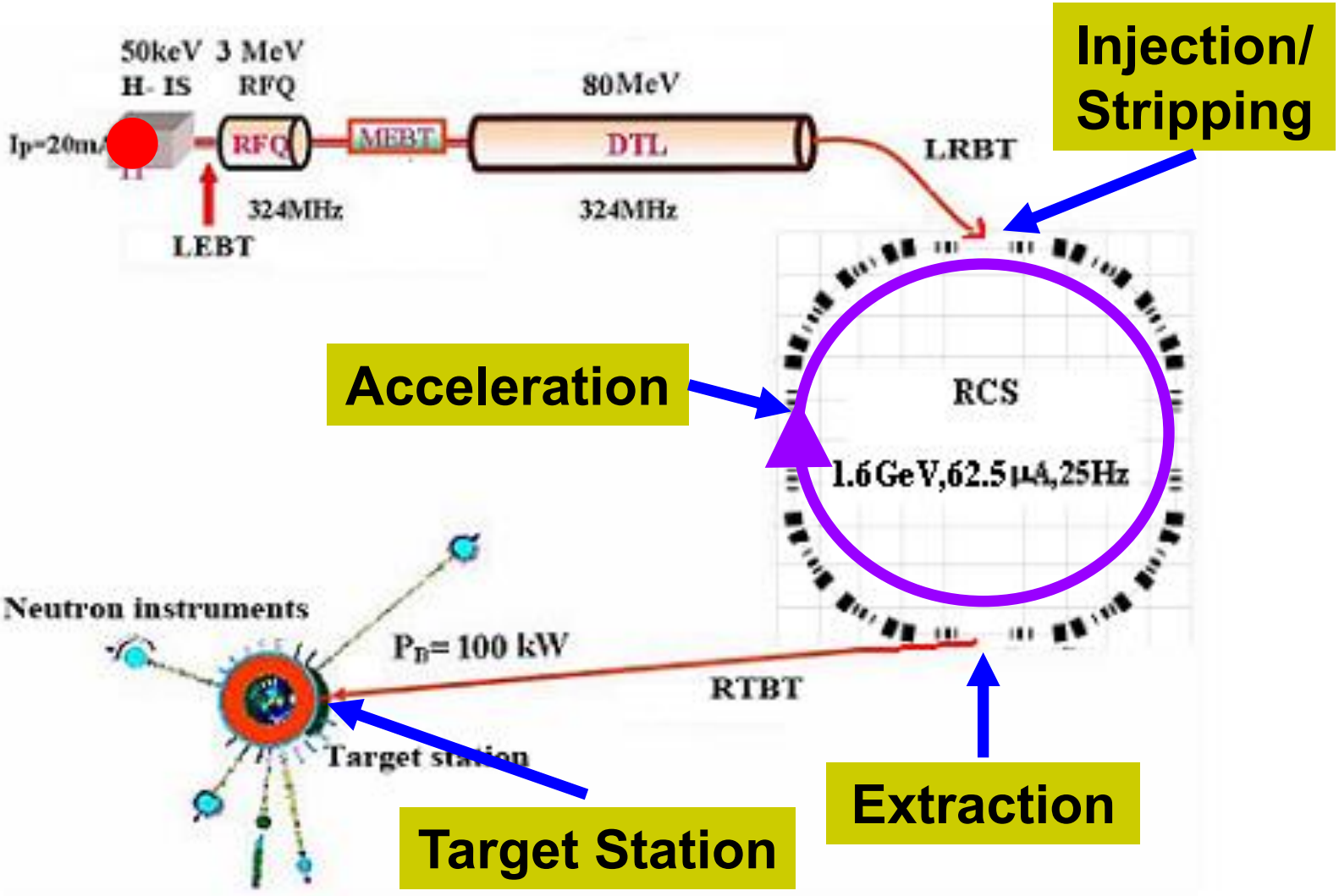

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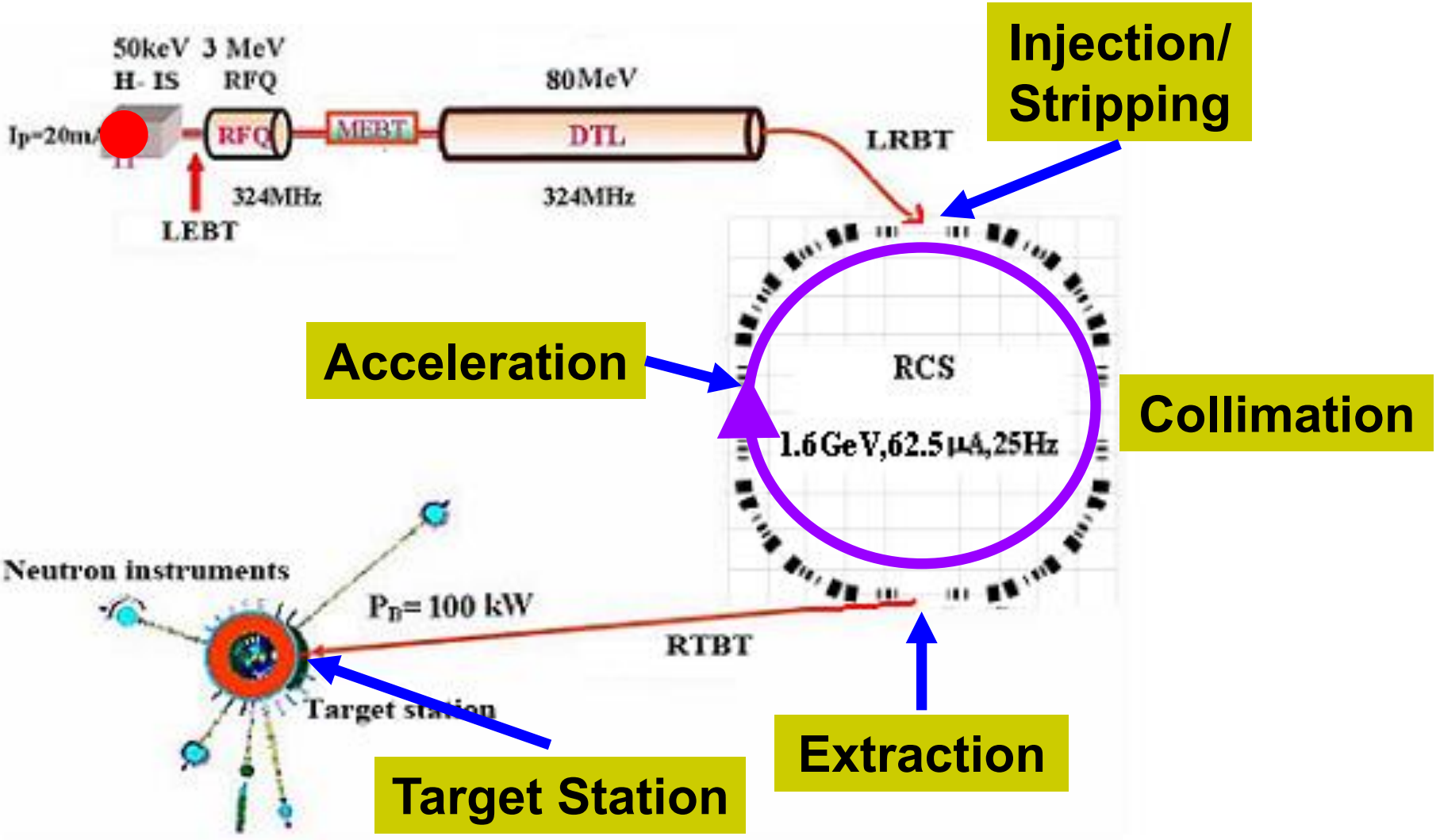
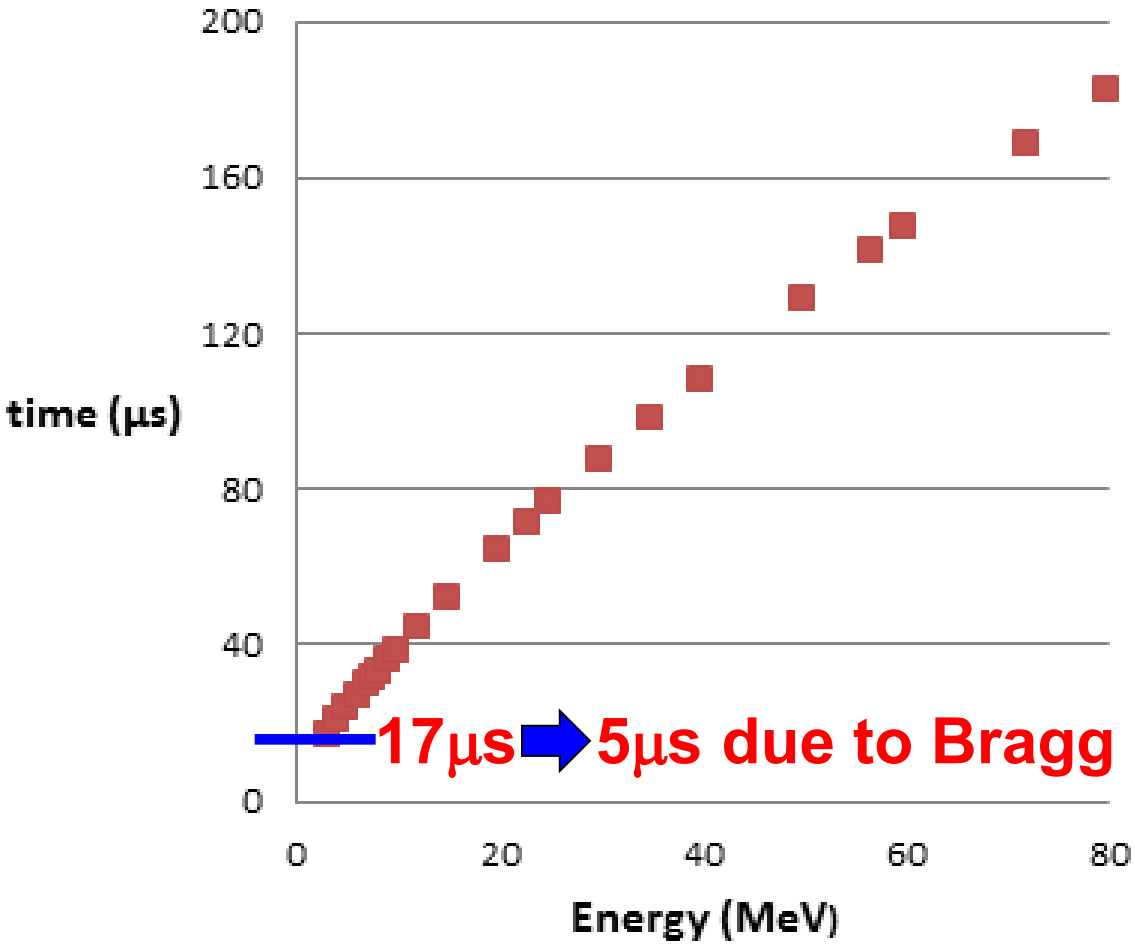


Fundamental safety requirements

- To prevent permanent damage to materials due to a heat deposition exceeding their thermal stress limit of accelerator components along the beam line, especially for copper in DTL (Drift Tube LINAC).

Fundamental safety requirements

Time to reach thermal stress limit on surface



1. Un-chopped beam, 15mA
2. Beam size : 0.2cm * 0.2cm RMS
3. Hitting the components directly

17μs ➡ 5μs due to Bragg Peak ➡ 10μs if chopped

Critical most cases

Basic design considerations and rules

- Reliable and mature industrial and commercial products should be used when available.
- All interfaces should be fail-safe or online real-time checked to make sure the reliability.
- Interlock logic should be as simple as possible and developed with reliable tools.
- Considerations : reliability, maintainability, stability, scalability and flexibility.

Overall design

Inputs classification

- Failure of components along the beam line below 50keV (before RFQ) will not bring severe damage due to the lower beam energy and the loss of H- in RFQ. These signals are delivered to MPS, a protection system of ms response time.

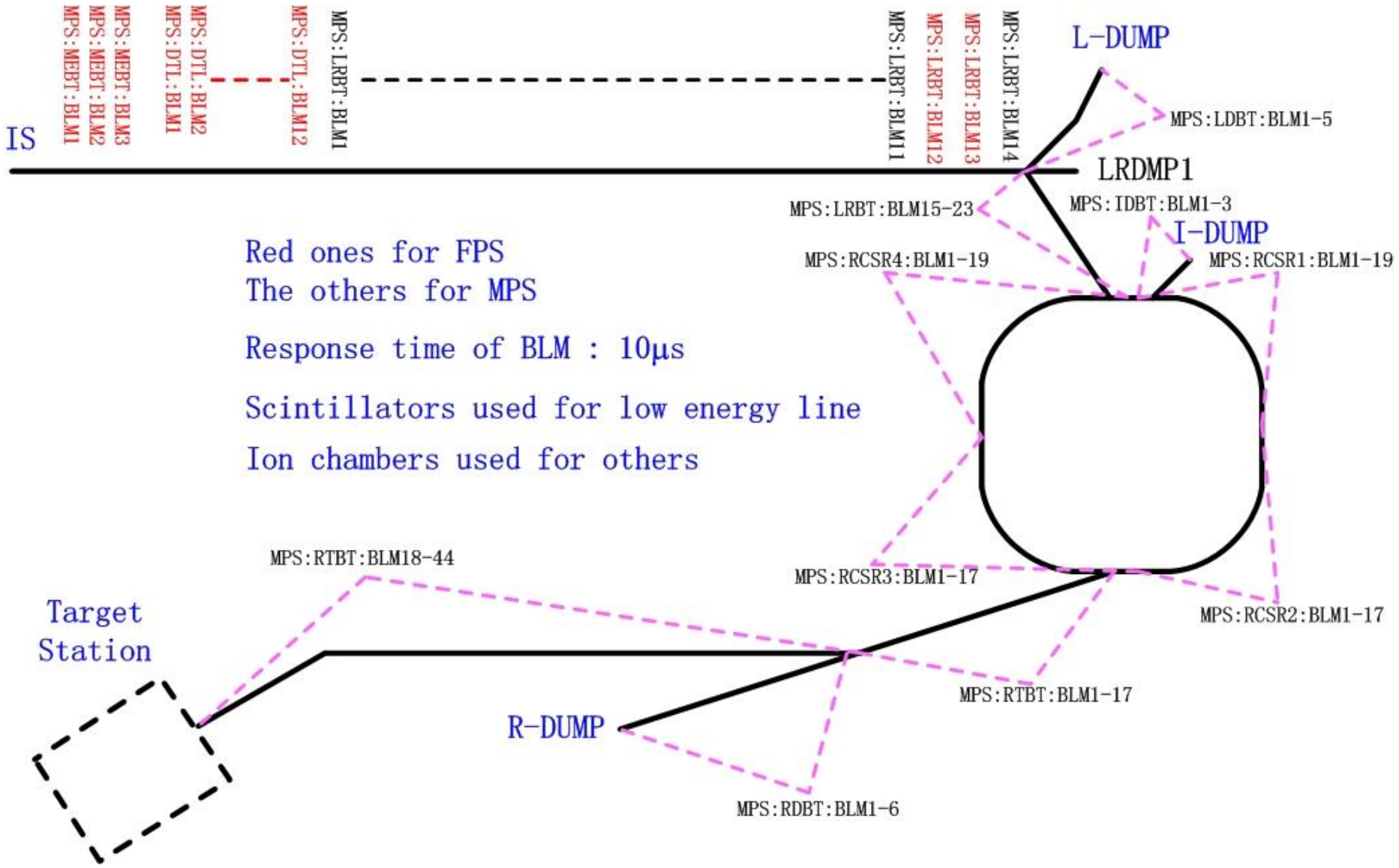
Overall design

Inputs classification

- Failure of components from RFQ to the end of DTL will possibly bring great damage, especially to the copper of the drift tubes since their small diameter. These signals are delivered to FPS. BLM (Beam Loss Monitor) signals in this region are also delivered to FPS. Two BLM signals on the LRBT are also delivered to FPS to protect the de-buncher.

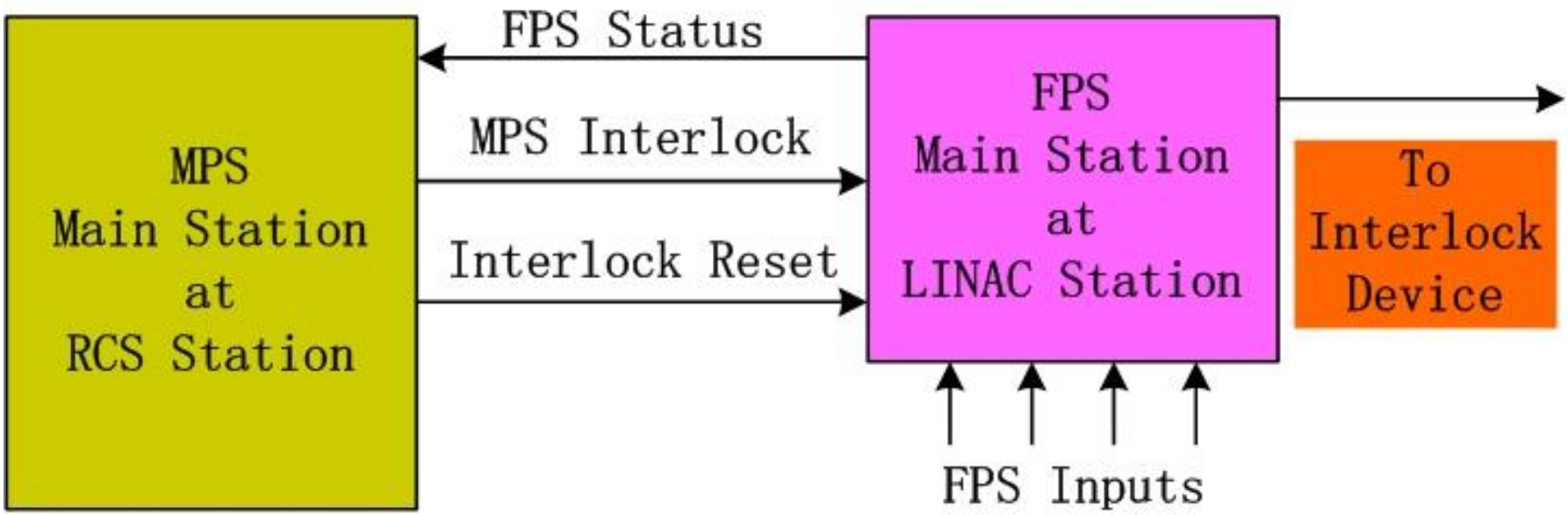
Overall design

Distribution of BLMs


MPS:MEBT:BLM1
MPS:MEBT:BLM2
MPS:MEBT:BLM3
MPS:DTL:BLM1
MPS:DTL:BLM2
MPS:DTL:BLM12
MPS:LRBT:BLM1
MPS:LRBT:BLM11
MPS:LRBT:BLM12
MPS:LRBT:BLM13
MPS:LRBT:BLM14
IS
L-DUMP
MPS:LDBT:BLM1-5
LRDMP1
MPS:LRBT:BLM15-23
MPS:IDBT:BLM1-3
I-DUMP
MPS:RCSR4:BLM1-19
MPS:RCSR1:BLM1-19
Red ones for FPS
The others for MPS
Response time of BLM : 10μs
Scintillators used for low energy line
Ion chambers used for others
MPS:RTBT:BLM18-44
MPS:RCSR3:BLM1-17
MPS:RCSR2:BLM1-17
Target Station
MPS:RTBT:BLM1-17
R-DUMP
MPS:RDBT:BLM1-6

Overall design

System architecture



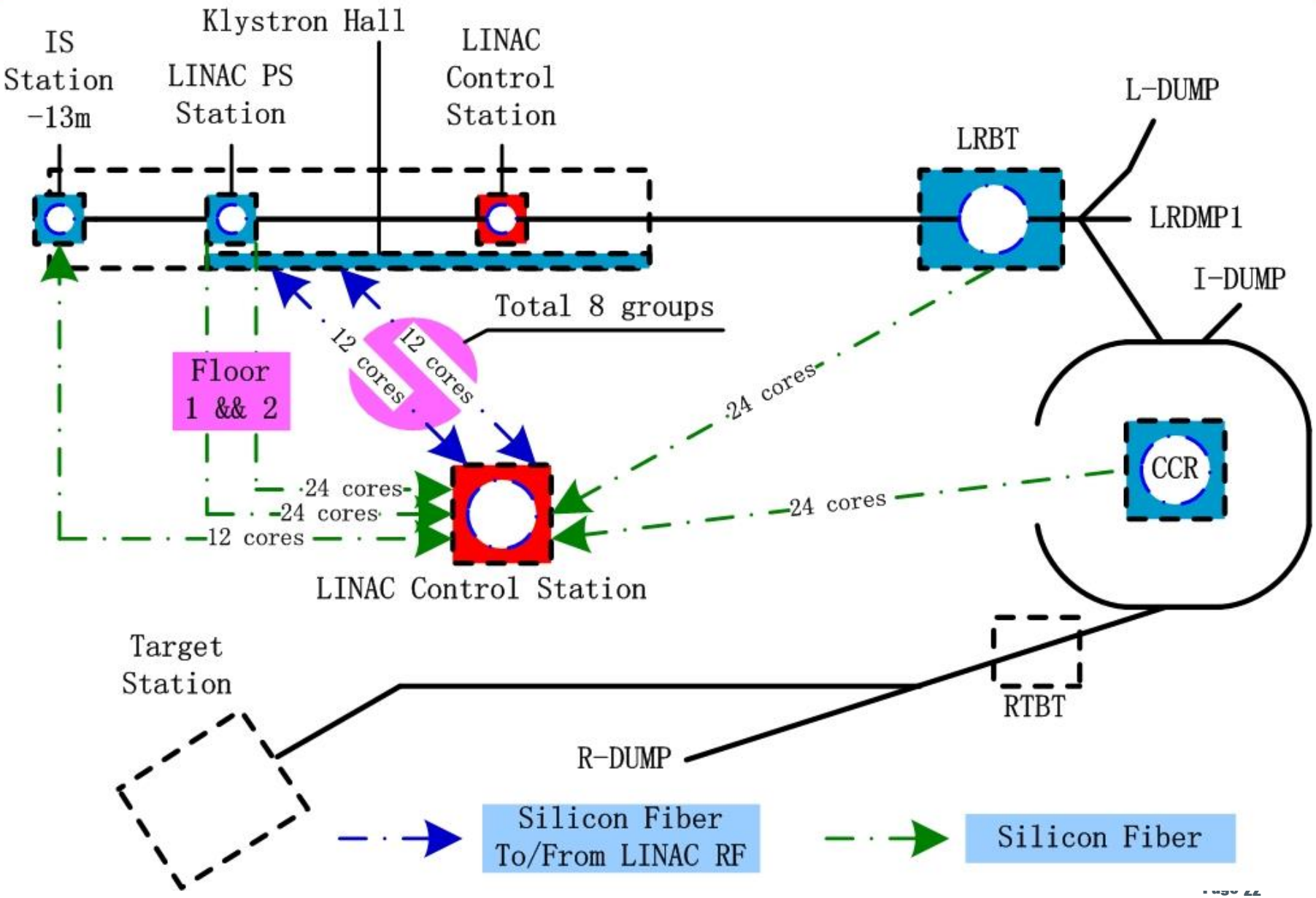
Overall design

Technique selection

- For FPS, a response time of around 5μs, low level signal and FPGA (Field Programmable Gate Array) should be used to fulfill the critical requirement, and to provide good flexibility.

Overall design

Structure and distribution of FPS


IS
Station
-13m
Klystron Hall
LINAC PS
Station
LINAC
Control
Station
L-DUMP
LRBT
LRDMP1
I-DUMP
Total 8 groups
12 cores
12 cores
Floor
1 && 2
24 cores
24 cores
24 cores
24 cores
12 cores
CCR
LINAC Control Station
Target
Station
RTBT
R-DUMP
Silicon Fiber
To/From LINAC RF
Silicon Fiber

Overall design

How to stop the beam and recover

- Sending out interlock signals to stop the RFQ radio frequency power, to stop the beam gate signals to all the LINAC radio frequency powers, to stop the timing signal to the ion source extraction power supply, to turn down the high voltage of the ion source power supply from 17kV to 10kV at the same time.

Overall design

How to stop the beam and recover

- To recover the RFQ radio frequency power to maintain RFQ resonance after either the timing signal of the ion source extraction power supply stopped or the high voltage of it turned down.
- To recover the timing signal of the ion source extraction power supply after its high voltage turned down.

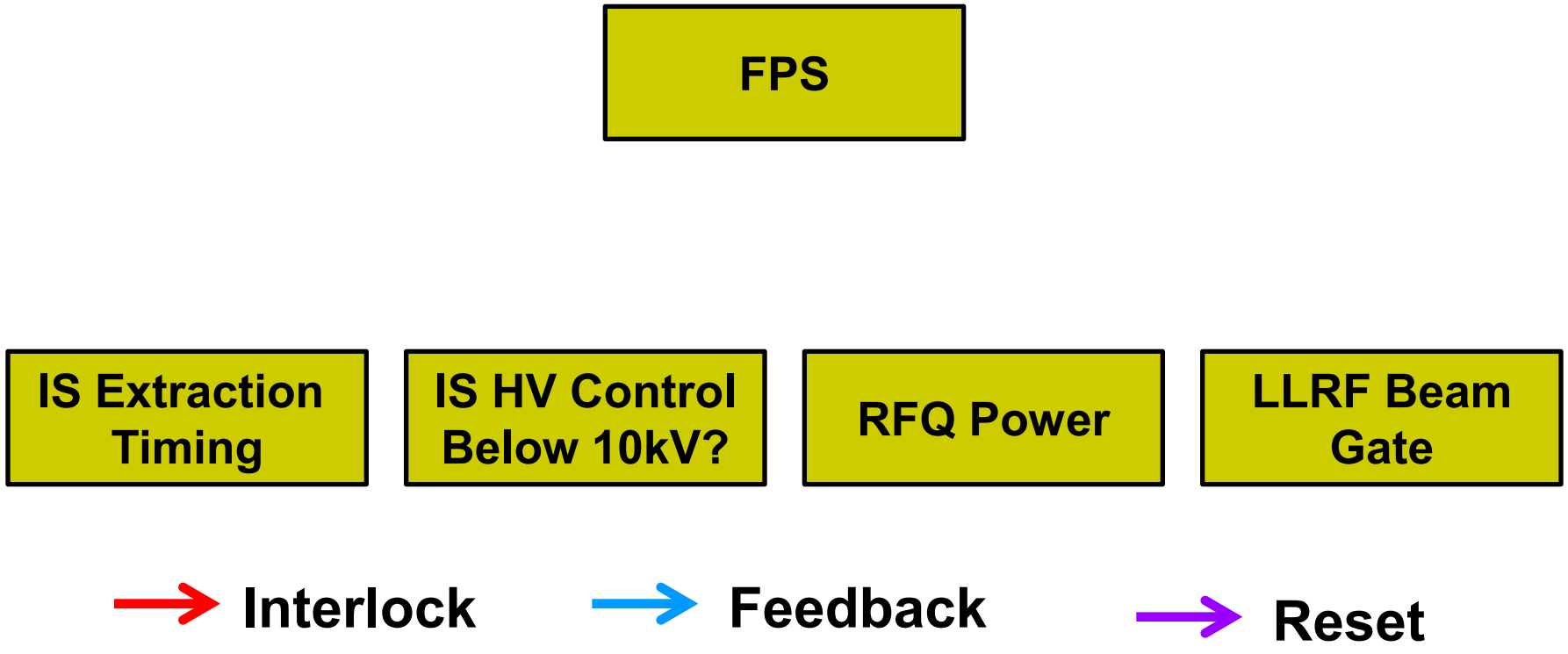
Overall design

How to stop the beam and recover

- The accelerator can recover from the interlock state after hand reset from the MPS with the faults cleared. Otherwise, beam is not permitted.

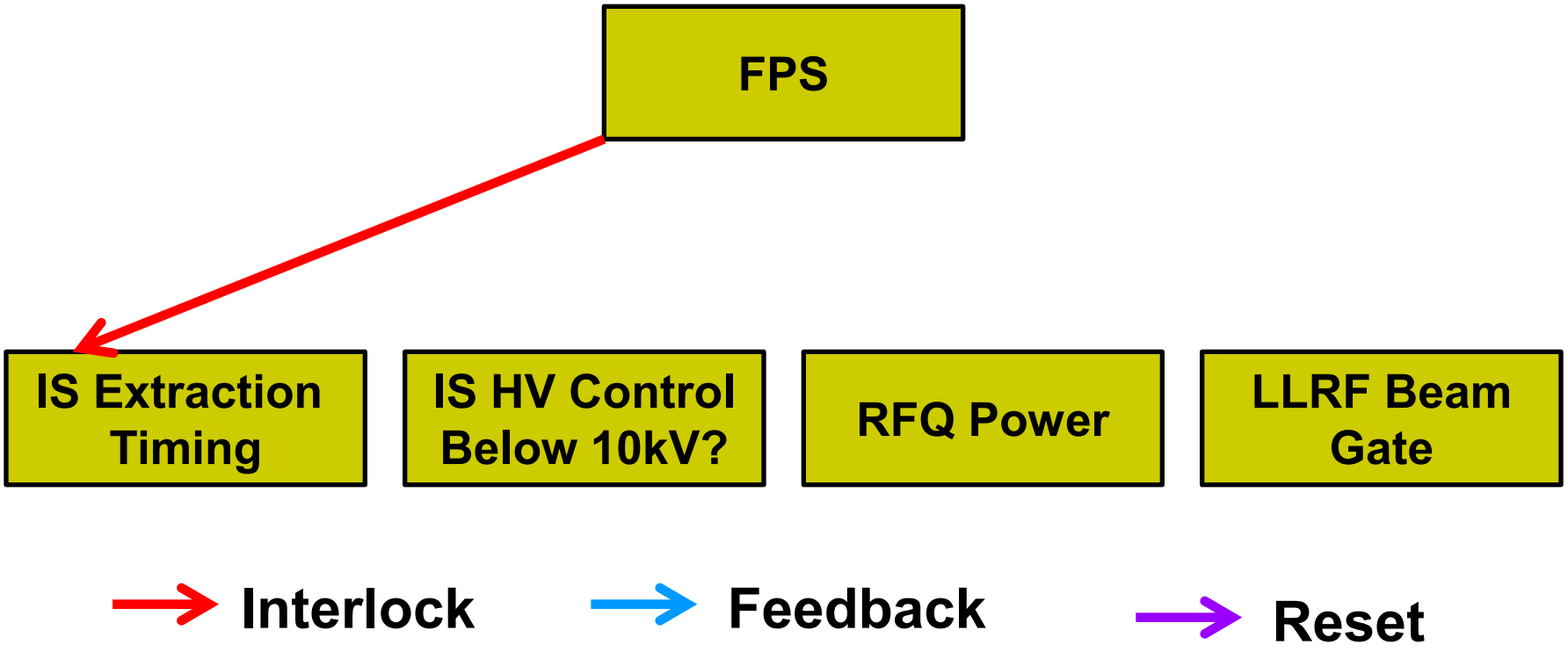
Overall design

How to stop the beam and recover



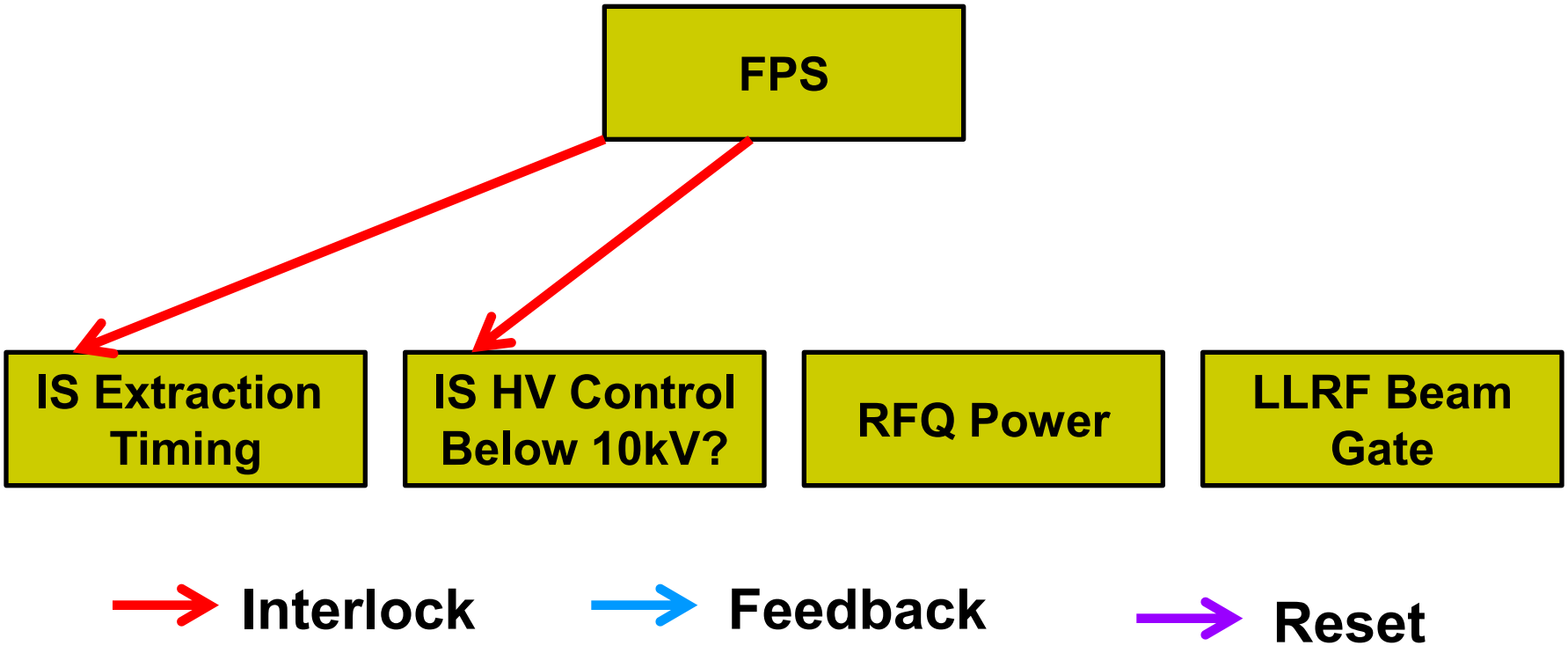
Overall design

How to stop the beam and recover



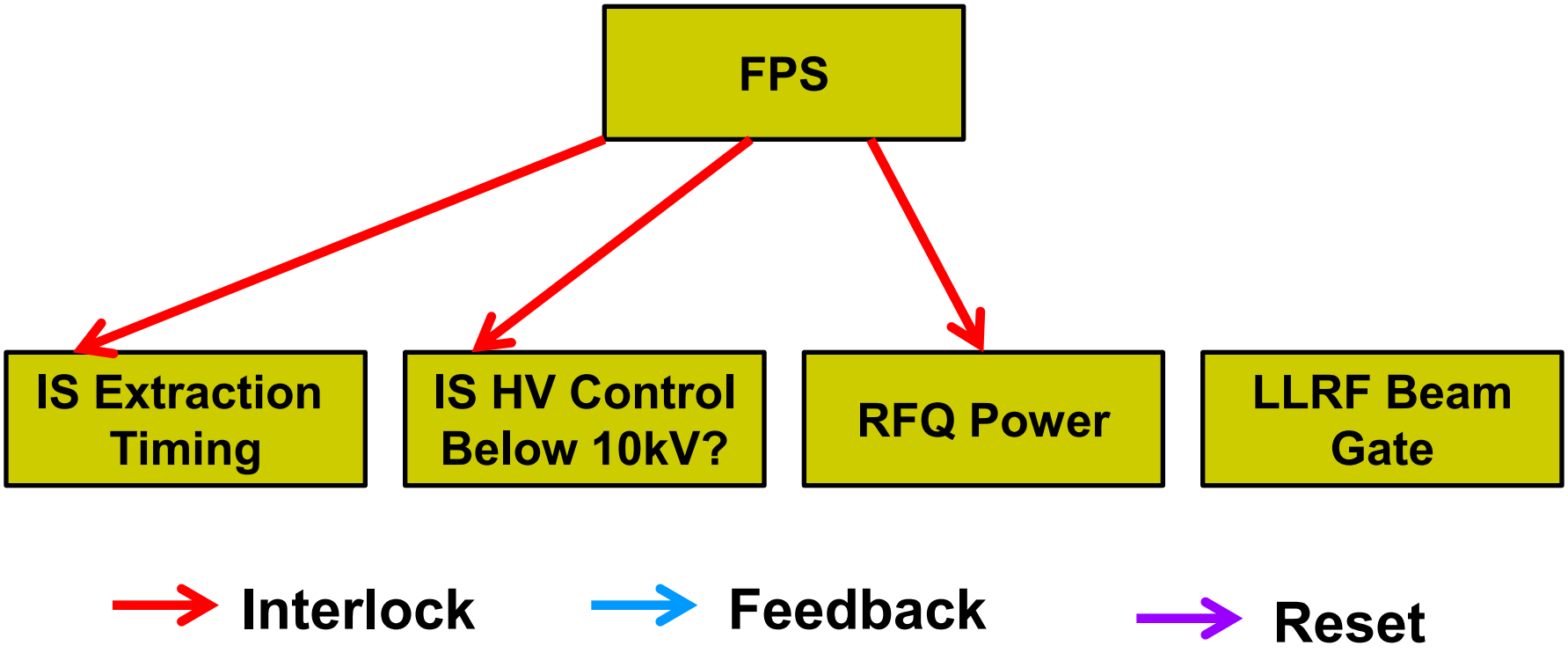
Overall design

How to stop the beam and recover



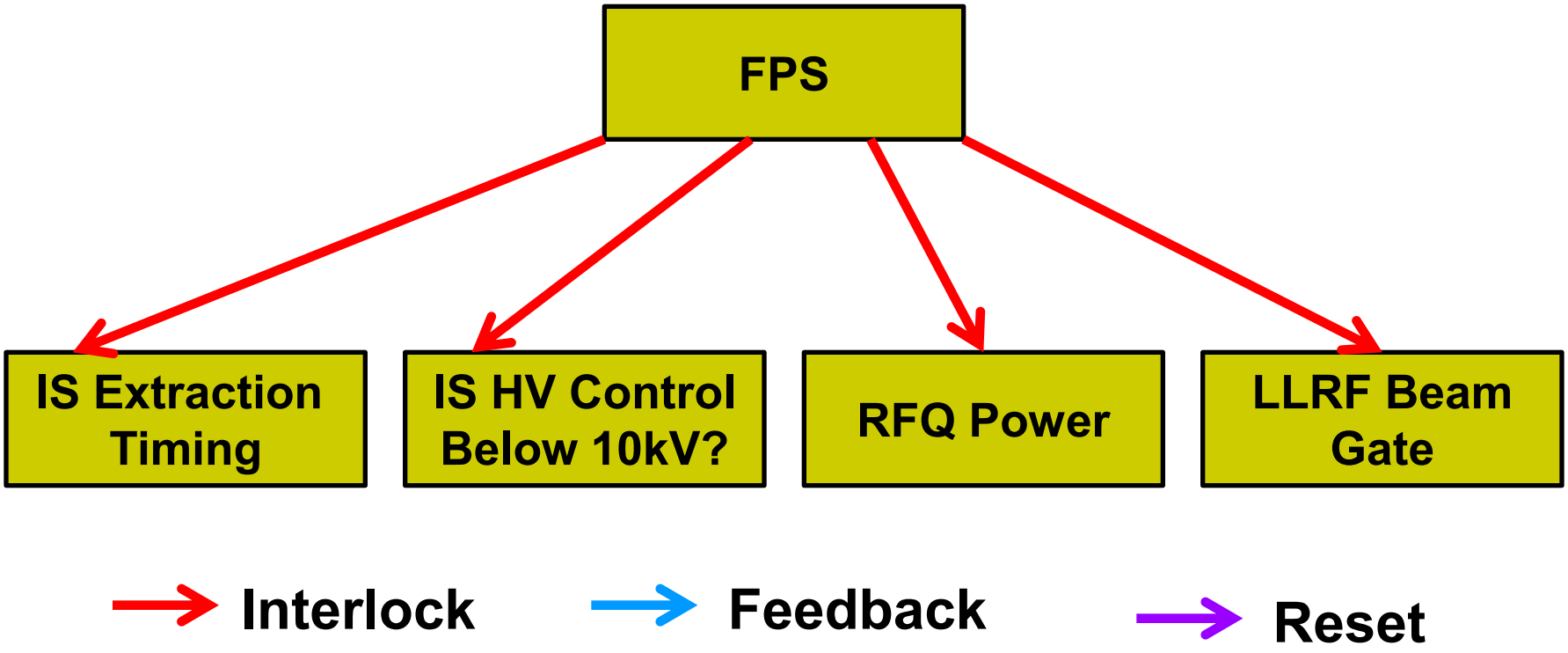
Overall design

How to stop the beam and recover



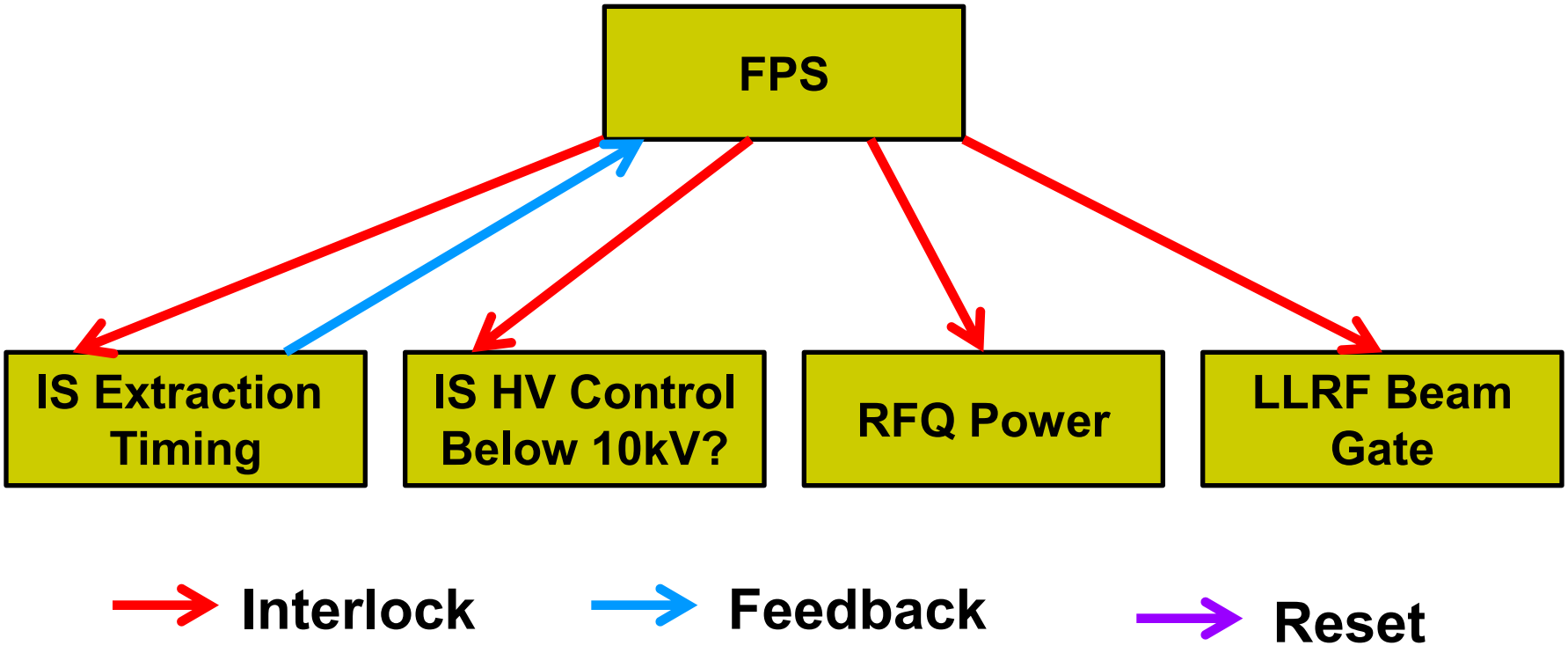
Overall design

How to stop the beam and recover



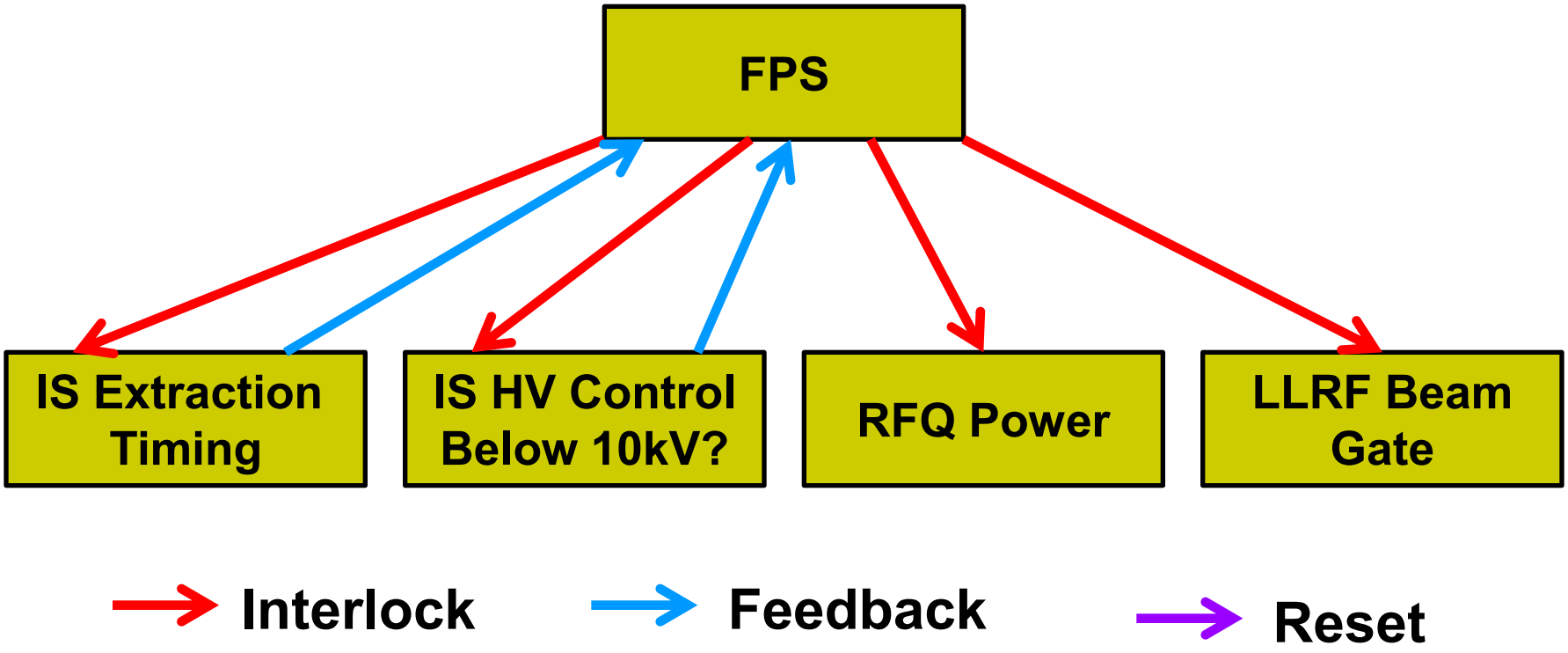
Overall design

How to stop the beam and recover



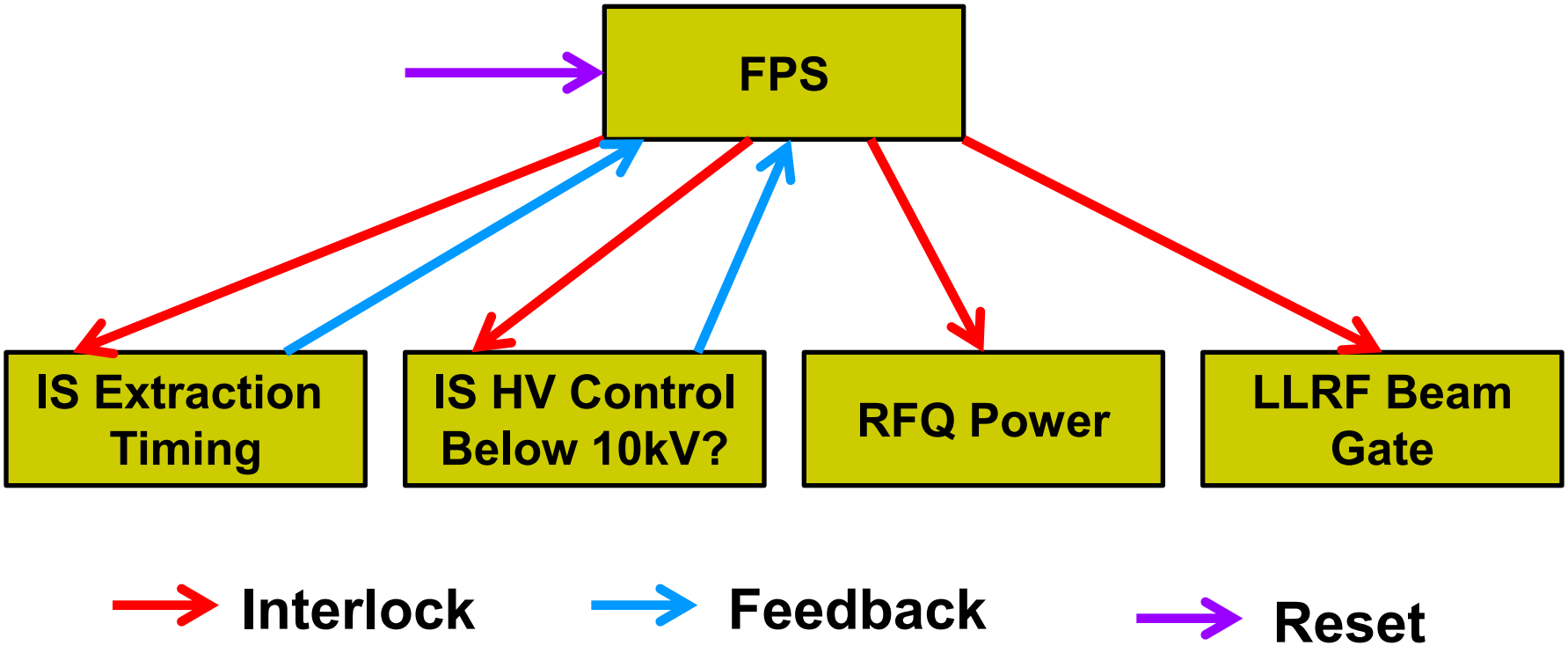
Overall design

How to stop the beam and recover



Overall design

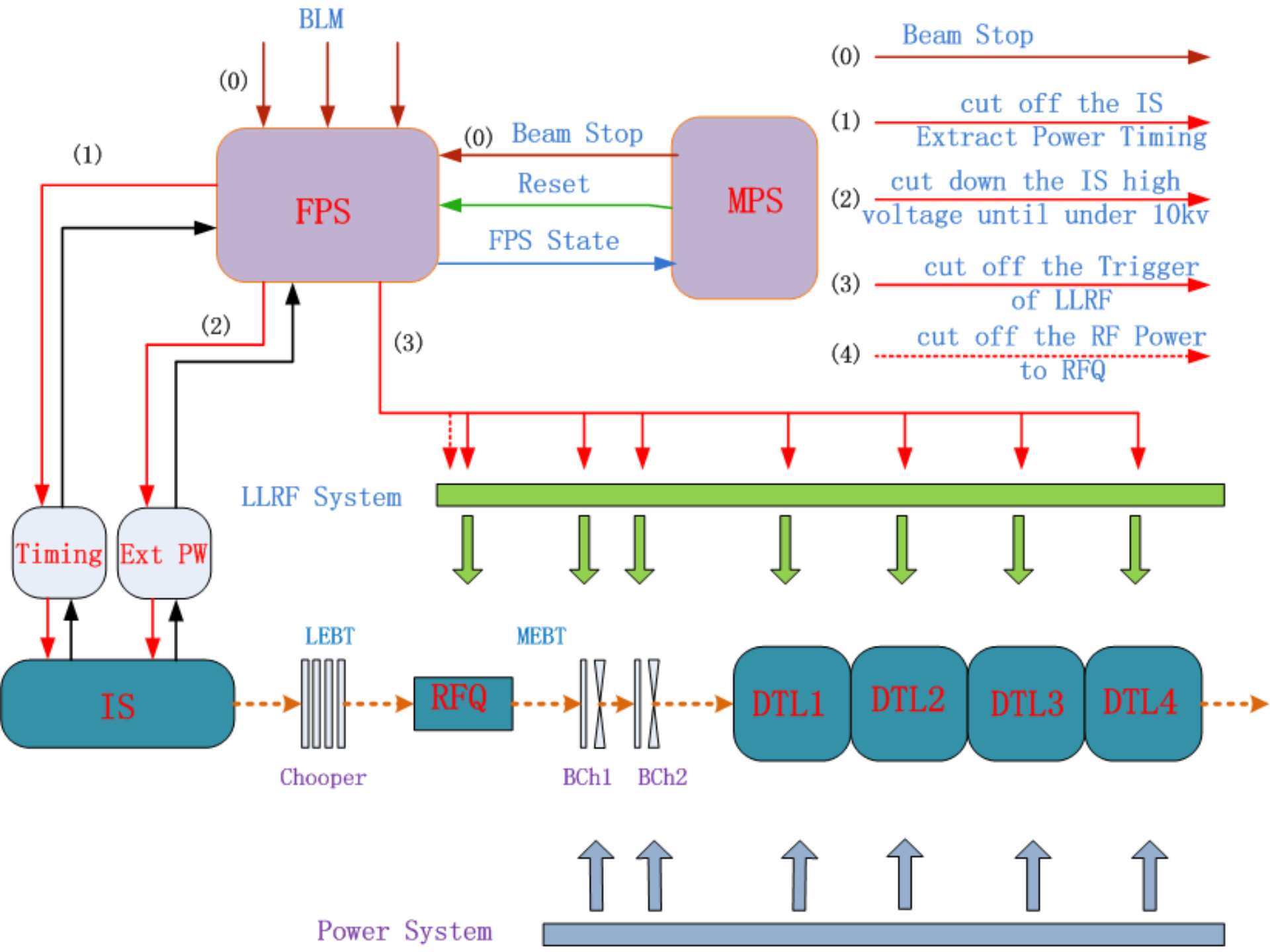
How to stop the beam and recover



Overall design

How to stop the beam and recover

- Figure.


BLM
(0)
(1)
FPS
(0) Beam Stop
Reset
FPS State
MPS
(2)
(3)
(0) Beam Stop
(1) cut off the IS Extract Power Timing
(2) cut down the IS high voltage until under 10kv
(3) cut off the Trigger of LLRF
(4) cut off the RF Power to RFQ
LLRF System
Timing
Ext PW
IS
LEBT
Chooper
RFQ
MEBT
BCh1
BCh2
DTL1
DTL2
DTL3
DTL4
Power System

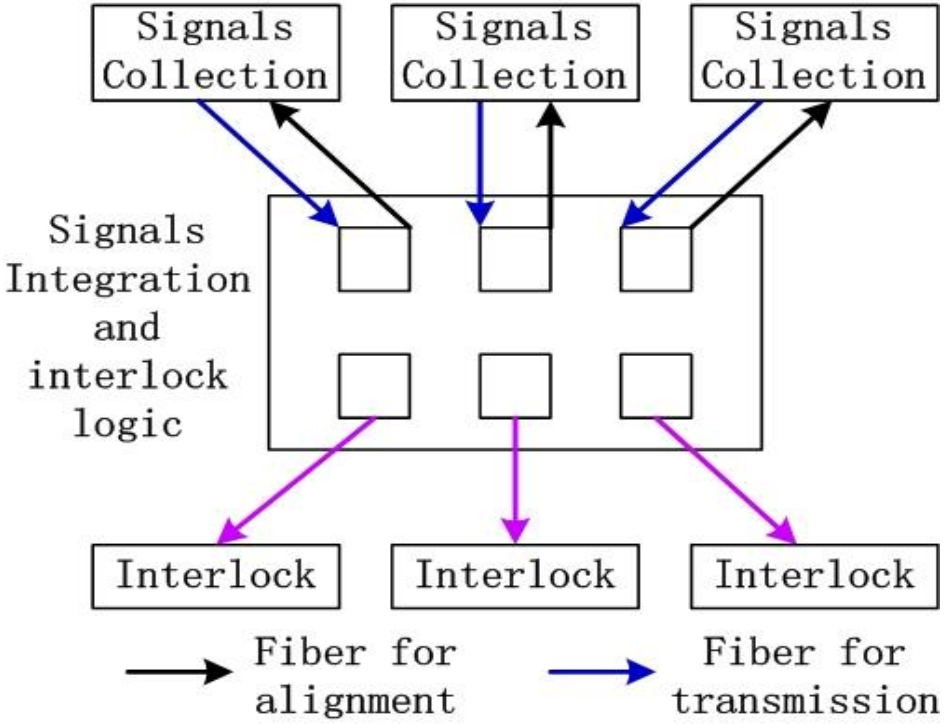
Design and implementation of FPS

- FPGA chip XC6SLX100T-3FGG900 from Xilinx is chosen as the main component for the FPS. Total 8 GTPs (Gigabit Transceiver Port, RocketIO), maximum 480 user IOs, ~100k logic cells …
- Central station : 6U VME 64x crate with 21 slots. Some user IOs for specific applications.

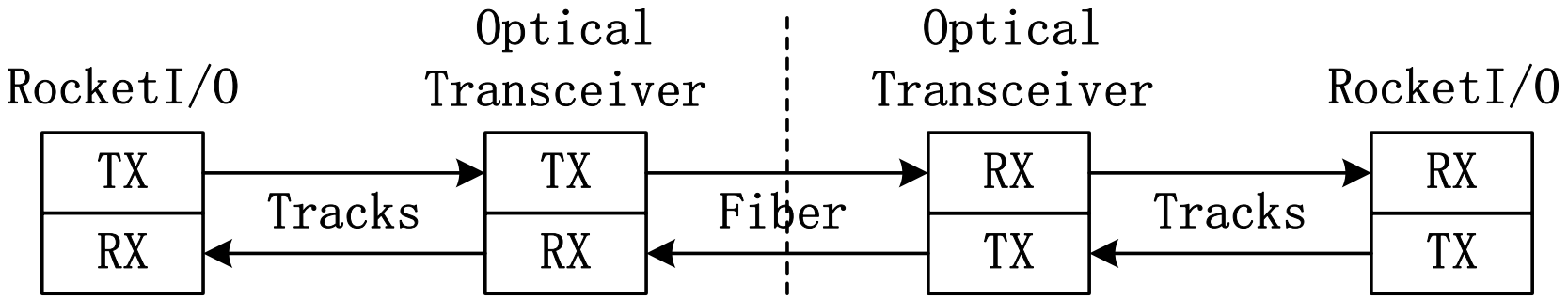
Design and implementation of FPS

- Signals collection in front end near interlock sources, with single core fibers for ground isolation. Signals to central stations through high speed serial links (GTP + opt. transceivers + opt. fibers) to reduce the number of fiber cores, to ease system installation, maintenance and upgrade.

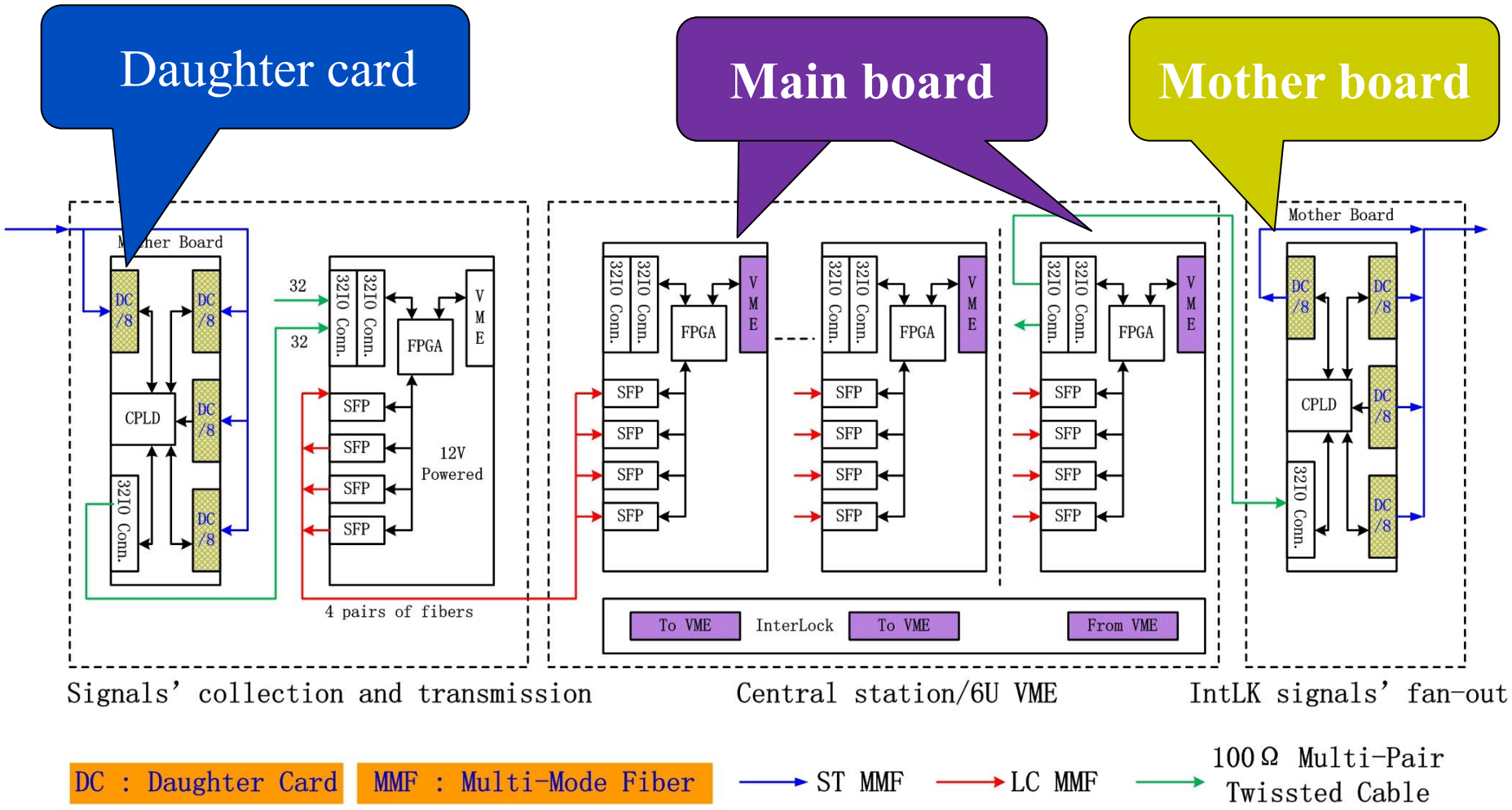
Design and implementation of FPS



- **Fiber and High Speed Serial Transmission based connection**
- **Auto-Synchronization**
- **1 pair fibers carrying 16 signals**
- **Central integration and treatment in 6U VME crate**

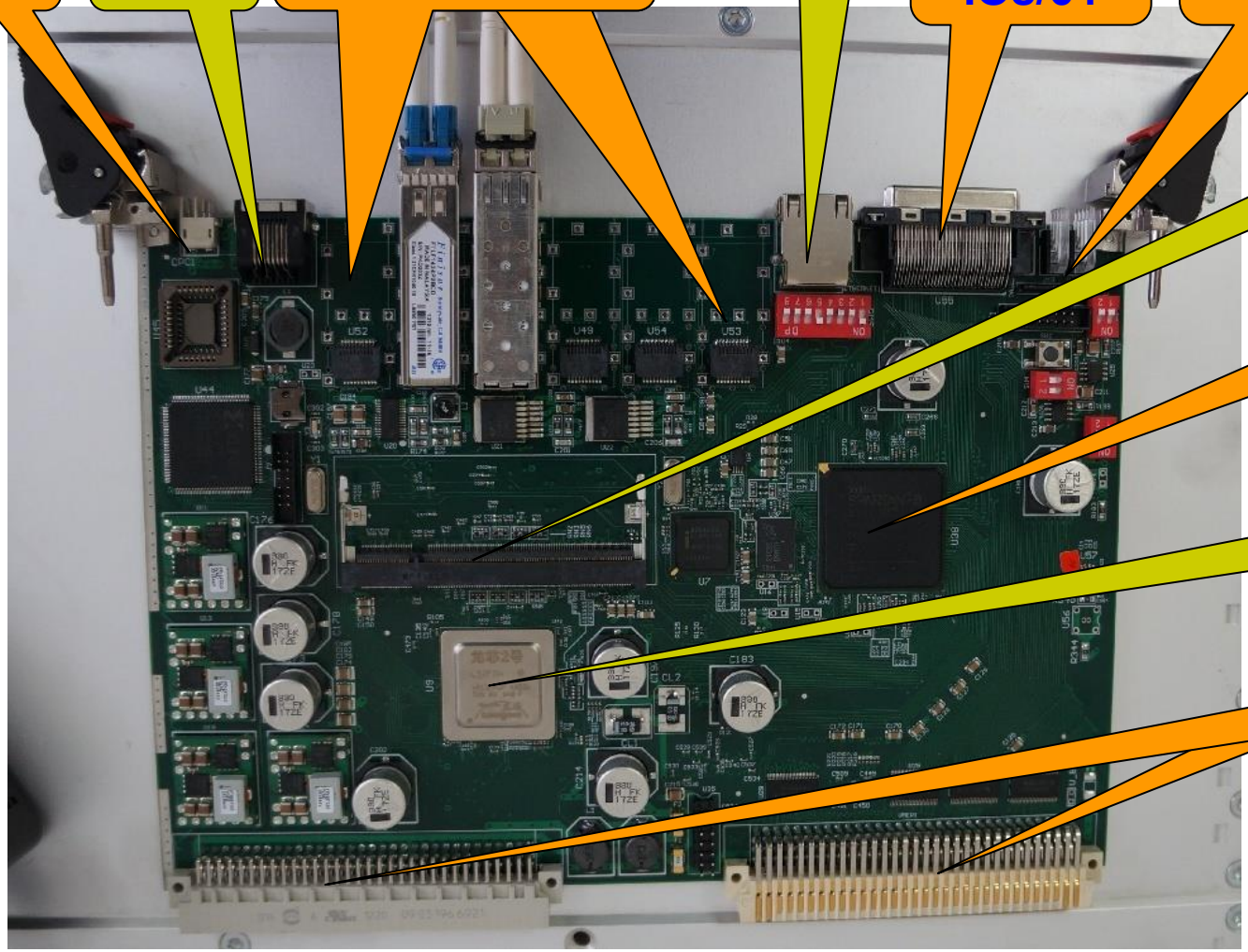


Design and implementation of FPS



Design and implementation of FPS

Photo of FPS main board



+12V

UART

Opt. transceivers/ RocketI/Os/6

Gb net

Extended IOs/64

Lamp indicators/8

DDR2 SODIMM

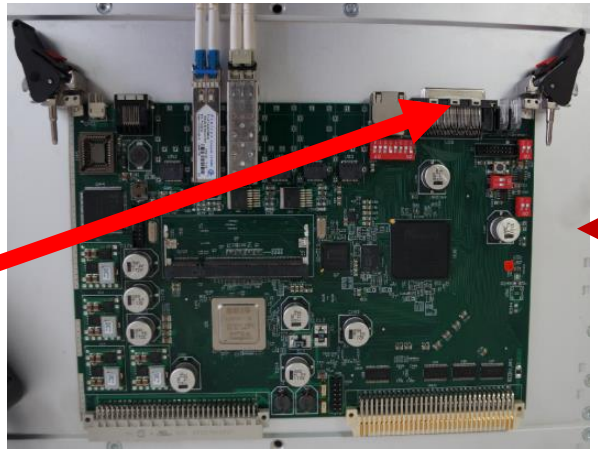
FPGA/XC6SLX 100T-3FGG900

CPU/ Loongson 2F

VME P1/P2

PWR : VME +5V or ext. +12V

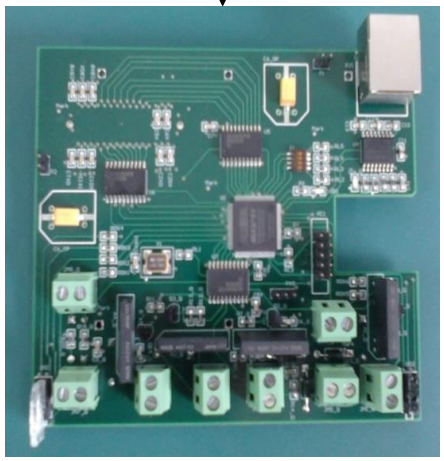
Design and implementation of FPS

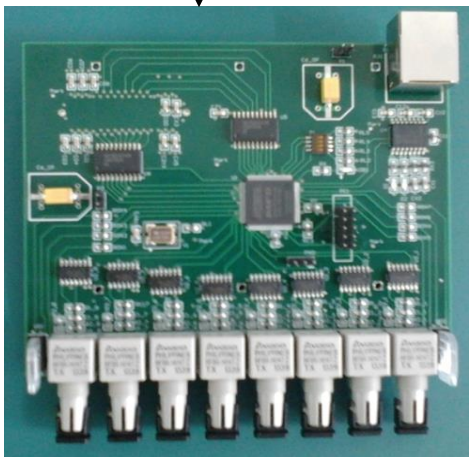


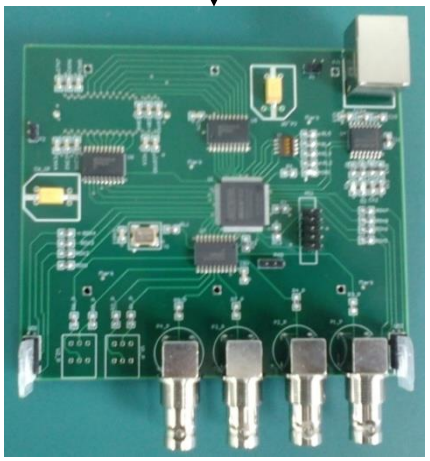
OP adaptor

Mother Board

Main Board







Design and implementation of FPS

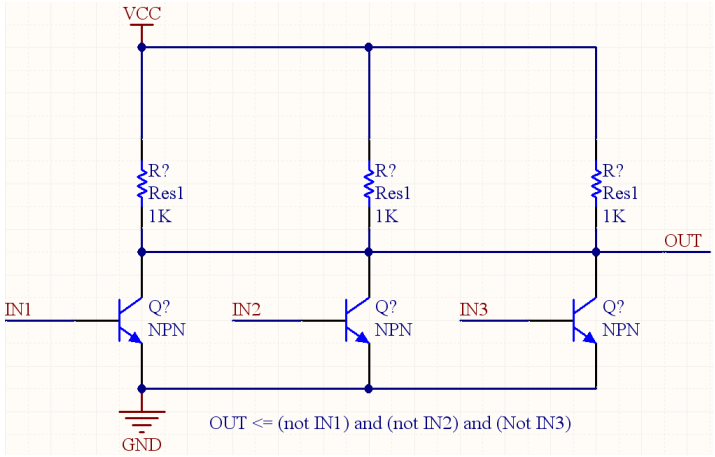
FPS Central Station : Field photo

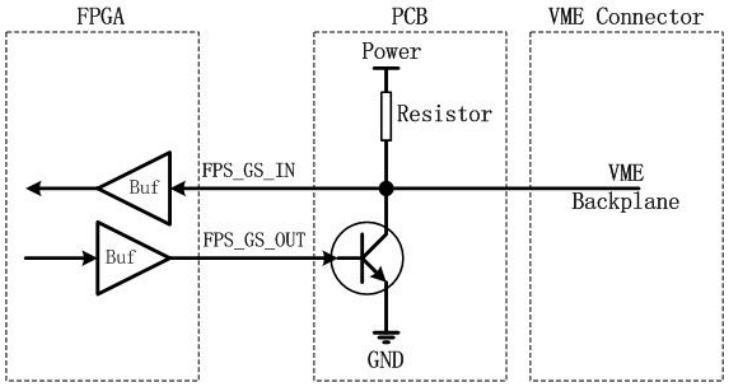
Design and implementation of FPS

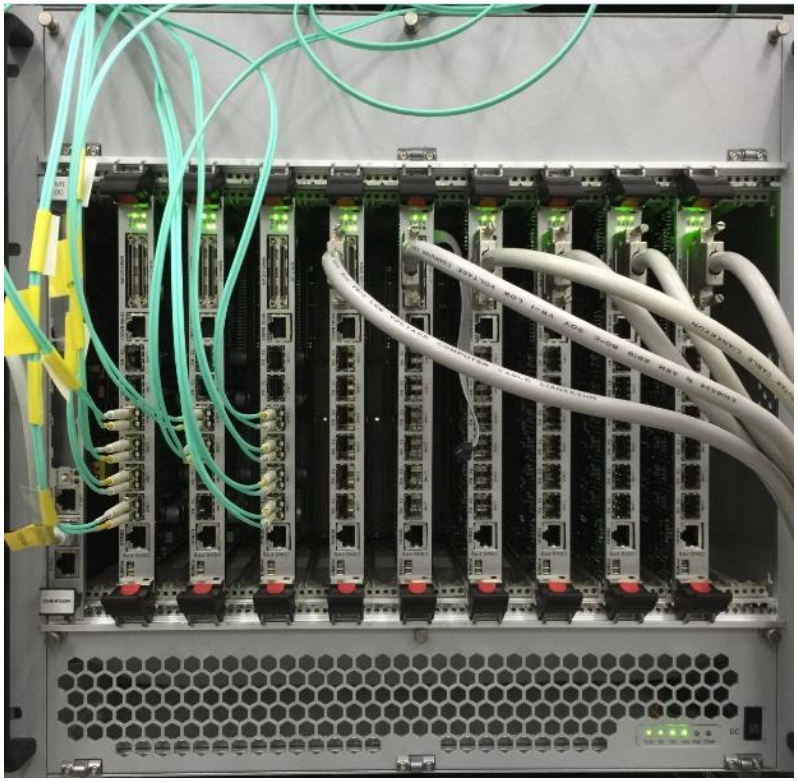
Cabinet front

Cabinet rear

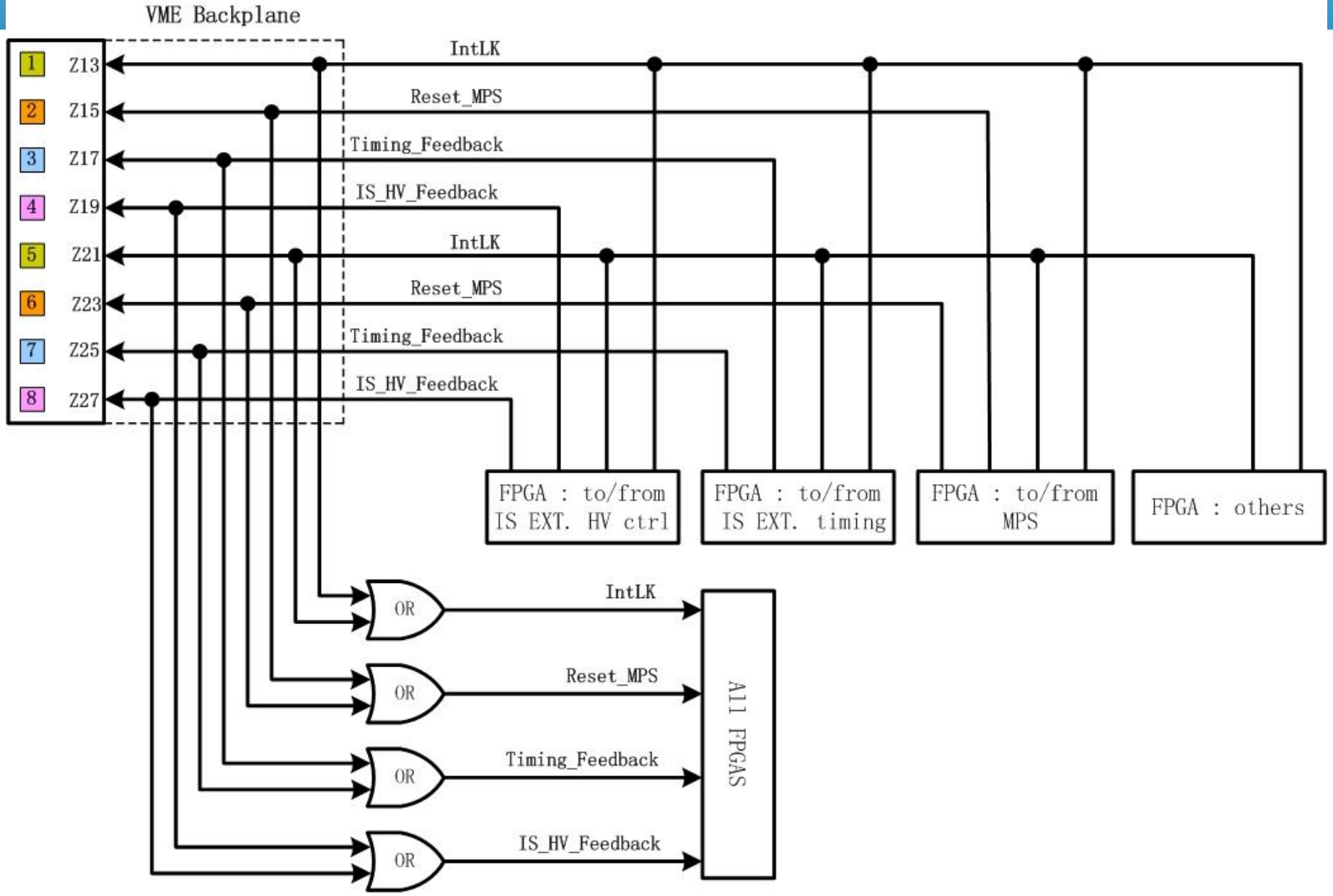
Design and implementation of FPS







Interlock output of each main board will transmit to the backplane, then all boards in crate receive it.


VME Backplane
1 Z13
2 Z15
3 Z17
4 Z19
5 Z21
6 Z23
7 Z25
8 Z27
IntLK
Reset_MPS
Timing_Feedback
IS_HV_Feedback
IntLK
Reset_MPS
Timing_Feedback
IS_HV_Feedback
FPGA : to/from IS EXT. HV ctrl
FPGA : to/from IS EXT. timing
FPGA : to/from MPS
FPGA : others
OR
OR
OR
OR
IntLK
Reset_MPS
Timing_Feedback
IS_HV_Feedback
All FPGAS

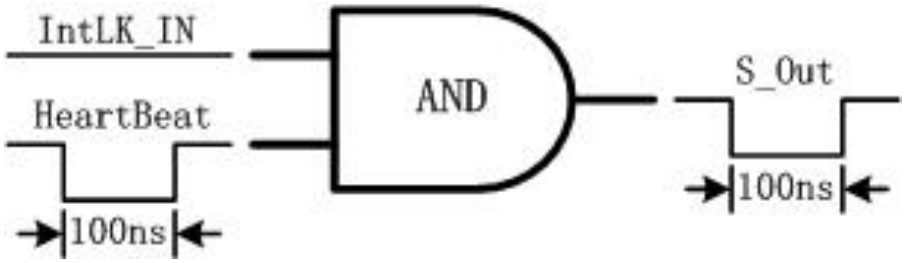
Design and implementation of FPS

Safety issues

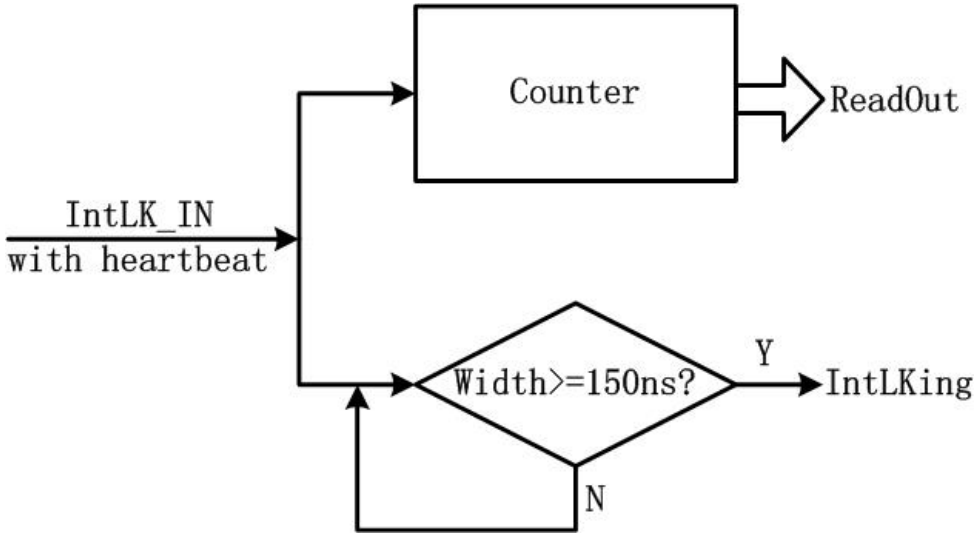
- Interface fail-safe definition : Avago optical transmitter 1414 and receiver 2412 are used for interlock inputs. Normal conditions are defined as the 1414 gives light out, interlock occurs when no light.
- Periodic heart-beat function are designed to make sure the safety of the signal route from the front end collection to the main station.

Design and implementation of FPS

Safety issues



Heart-beat signal generation in the CPLD on the daughter card of front end



Heart-beat signal check and counting in the FPGA on the main board at central station

Design and implementation of FPS

Safety issues

- Continuous readout and comparison of the interlock registers, the channel-mask registers and the heart-beat counters in the FPGA on the main boards at central station to make sure the proper work of the whole system, alarms will be given out when any error.
- Alarm when the VME crate power off.

Design and implementation of FPS

Safety issues

- Interlock signals to the RFQ RF, the IS extraction timing, the IS extraction HV control go through independent routes from the central station. Any of which fails will not affect the others' functions.

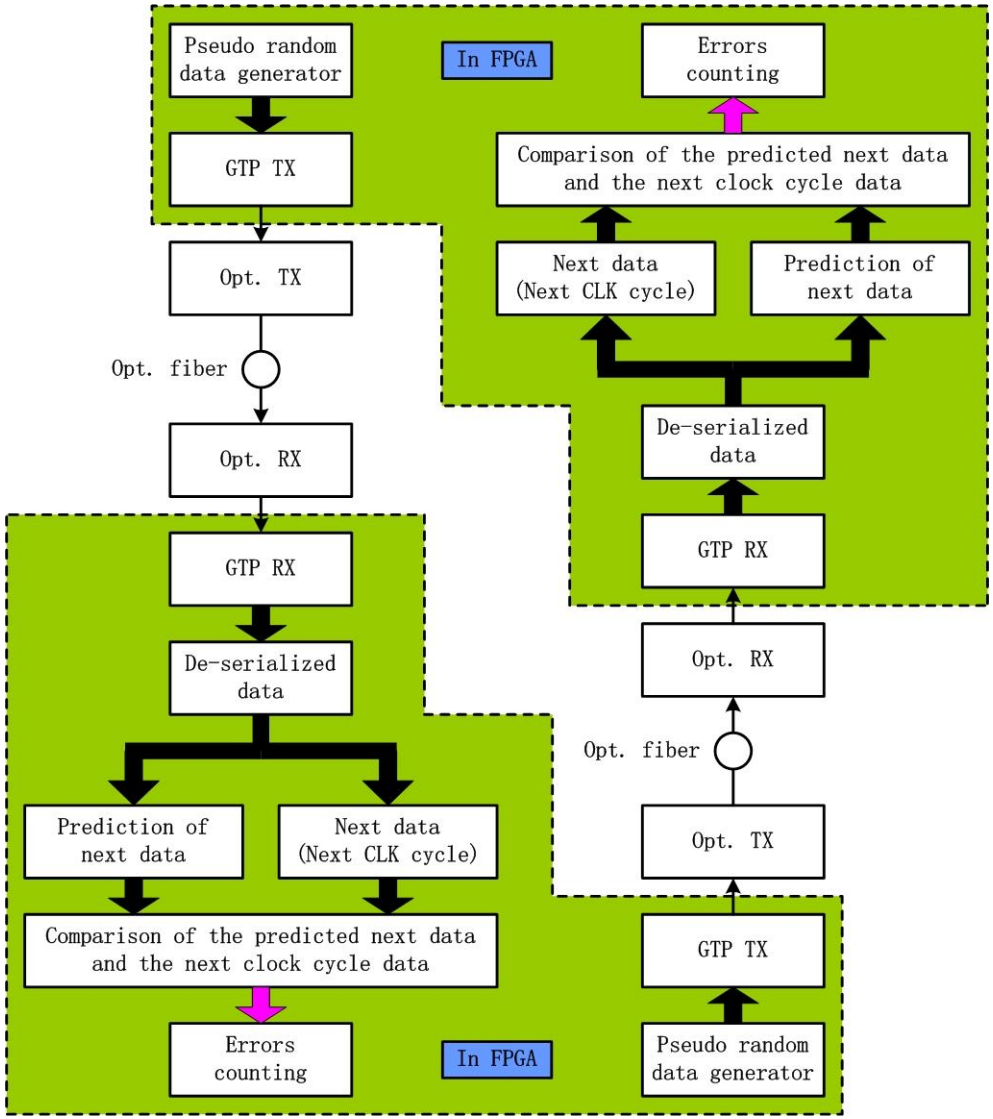
Design and implementation of FPS

Logic development and test

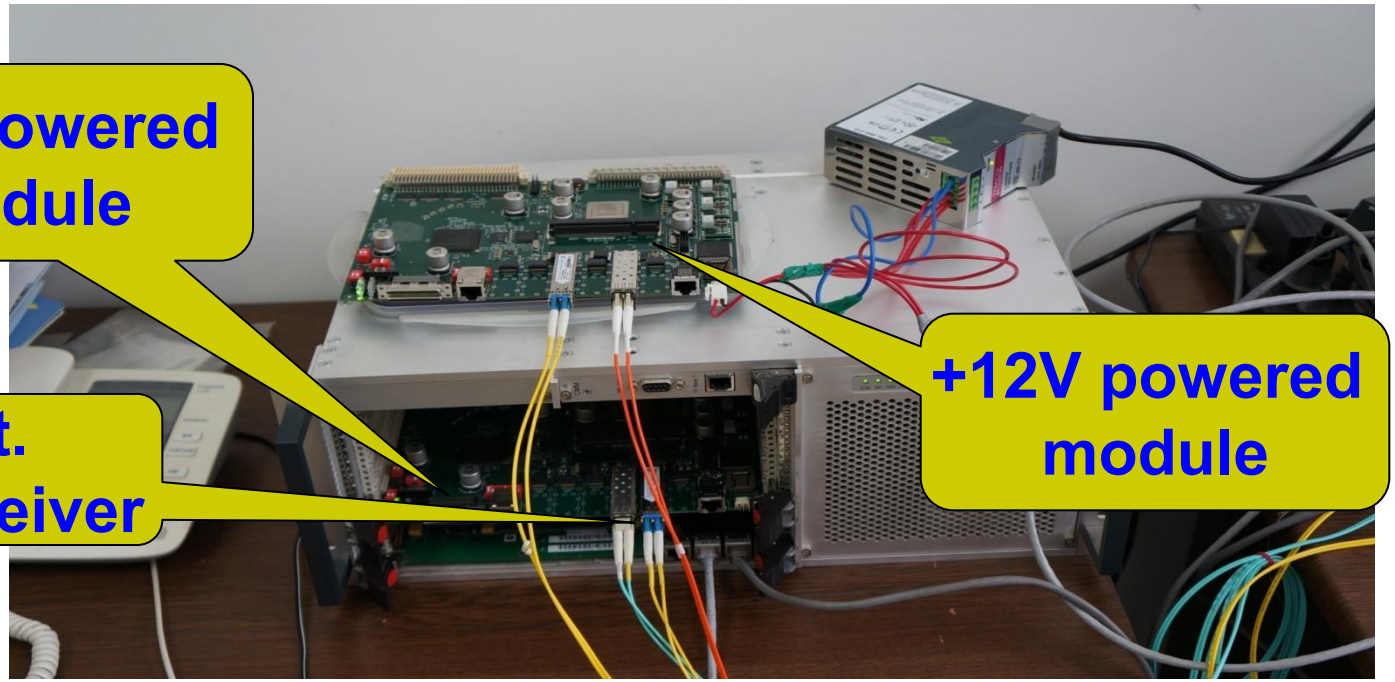
- Auto-synchronization function of the high speed path and bit error rate.
- When both fibers of the same high speed transceiver pair are plugged in, serial data are automatically de-serialized to parallel data.
- Bit error rate test is done with pseudo random data generated in the FPGA logic.

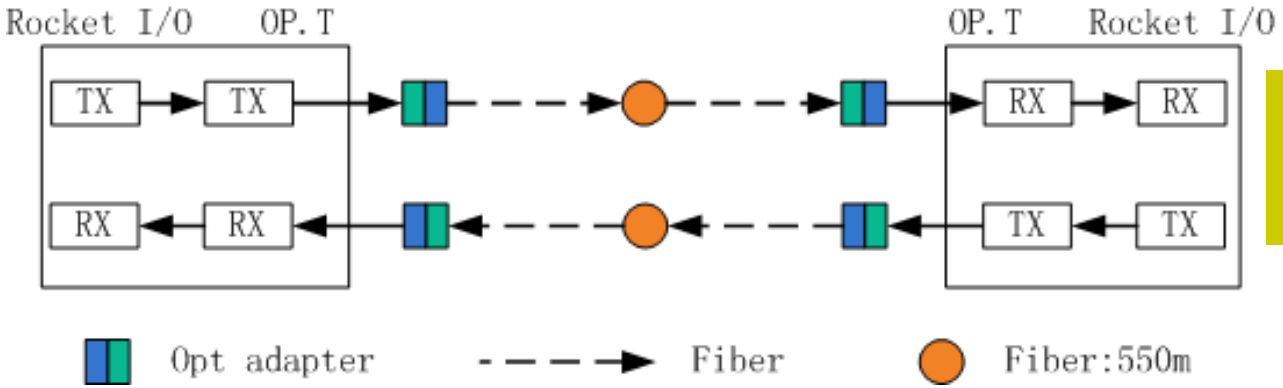
Design and implementation of FPS

Illustration of Bit Error Rate test



Design and implementation of FPS



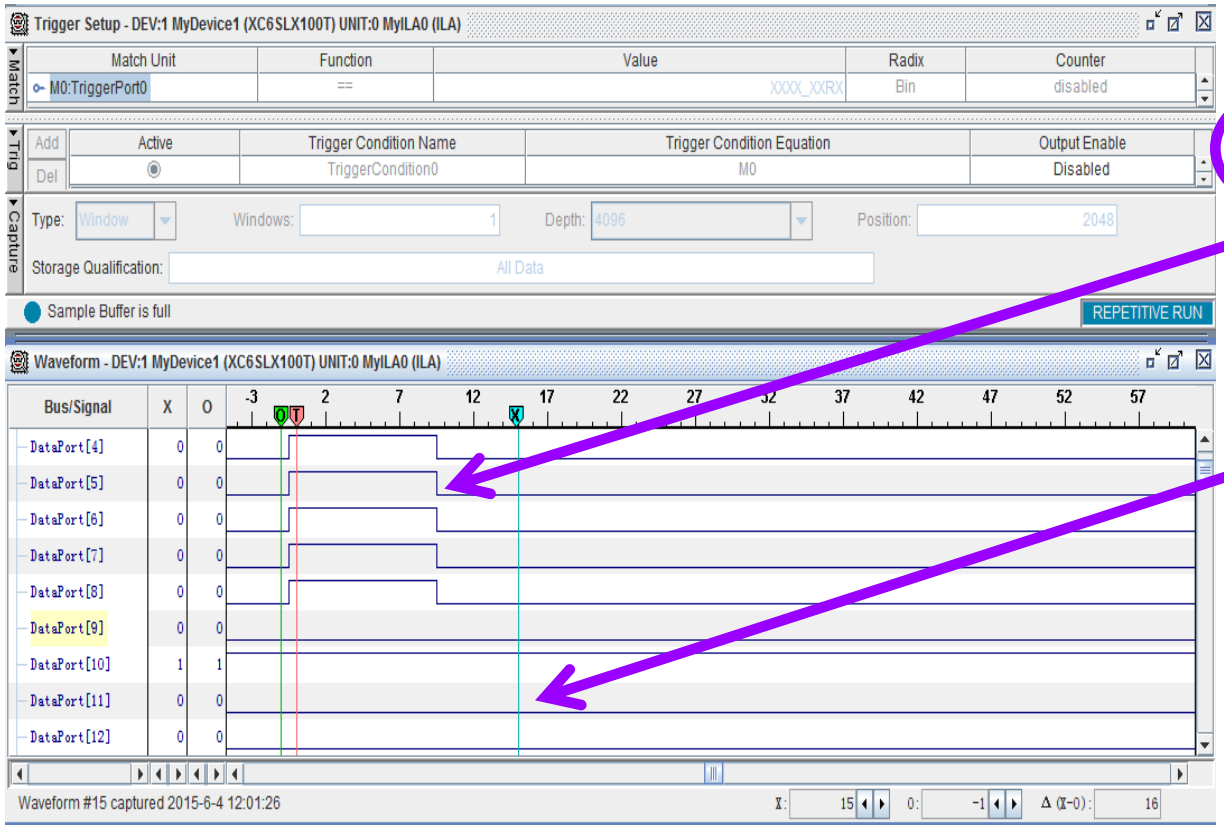


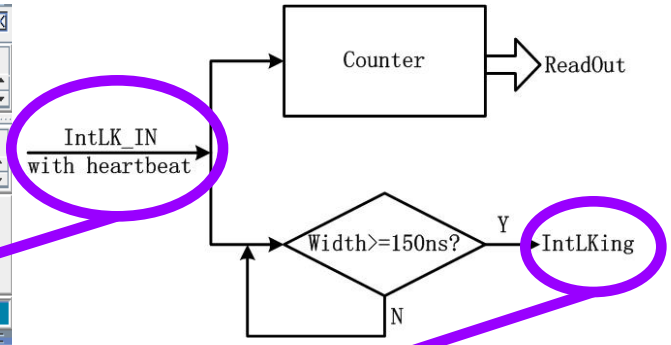
No errors in 27 hours

Design and implementation of FPS

Logic development and test

- **Heart-beat function.**





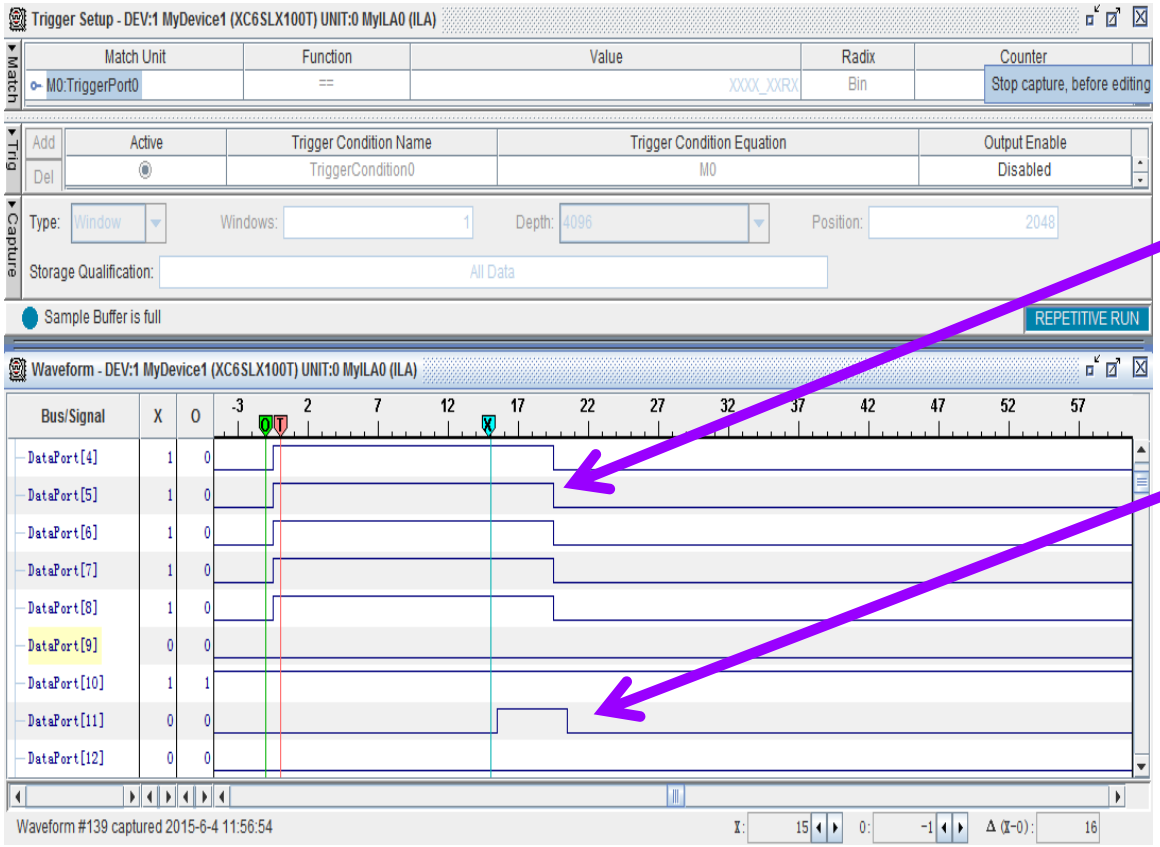
Signal width : 100ns

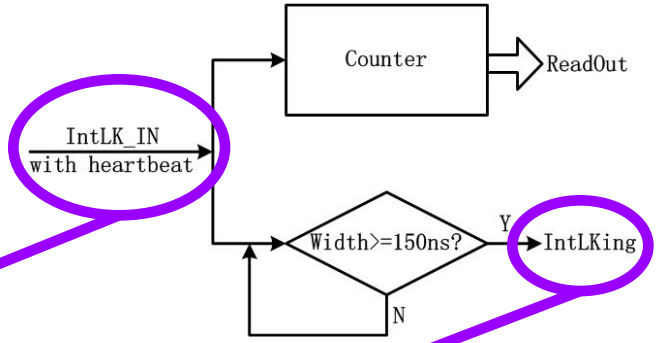
ChipScope Sampling clock : 100MHz

Design and implementation of FPS

Logic development and test

- **Heart-beat function.**





Signal width : 200ns

ChipScope Sampling clock : 100MHz

Design and implementation of FPS

Logic development and test

- Interlock function. Till now, signals connected are MEBT and DTL power supplies, MPS related, IS extraction timing and IS extraction HV control.
- Function test of RFQ RF power interface has been done electrically, but not connected.

Design and implementation of FPS

Logic development and test

- Till now, all signals connected have been tested one by one with ChipScope monitoring in the FPGA, including the feedback signals from the IS extraction timing and the IS extraction HV control.
- Interlock signal to the RFQ RF power is cancelled when either of the feedback signals is OK.

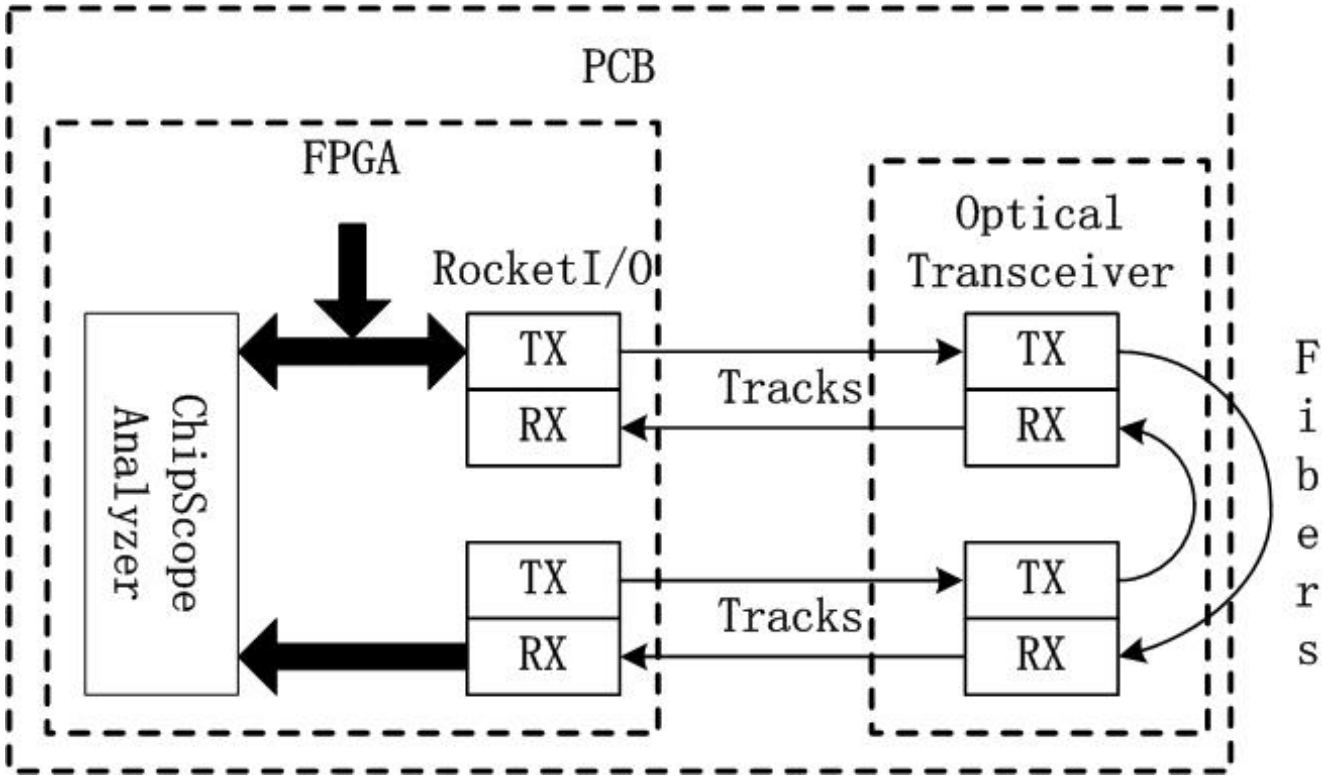
Design and implementation of FPS

Time consumption

- Time consumption includes delays in the fibers/cables and delays in the boards.
- Main delay is due to the length of optical fibers.

Design and implementation of FPS

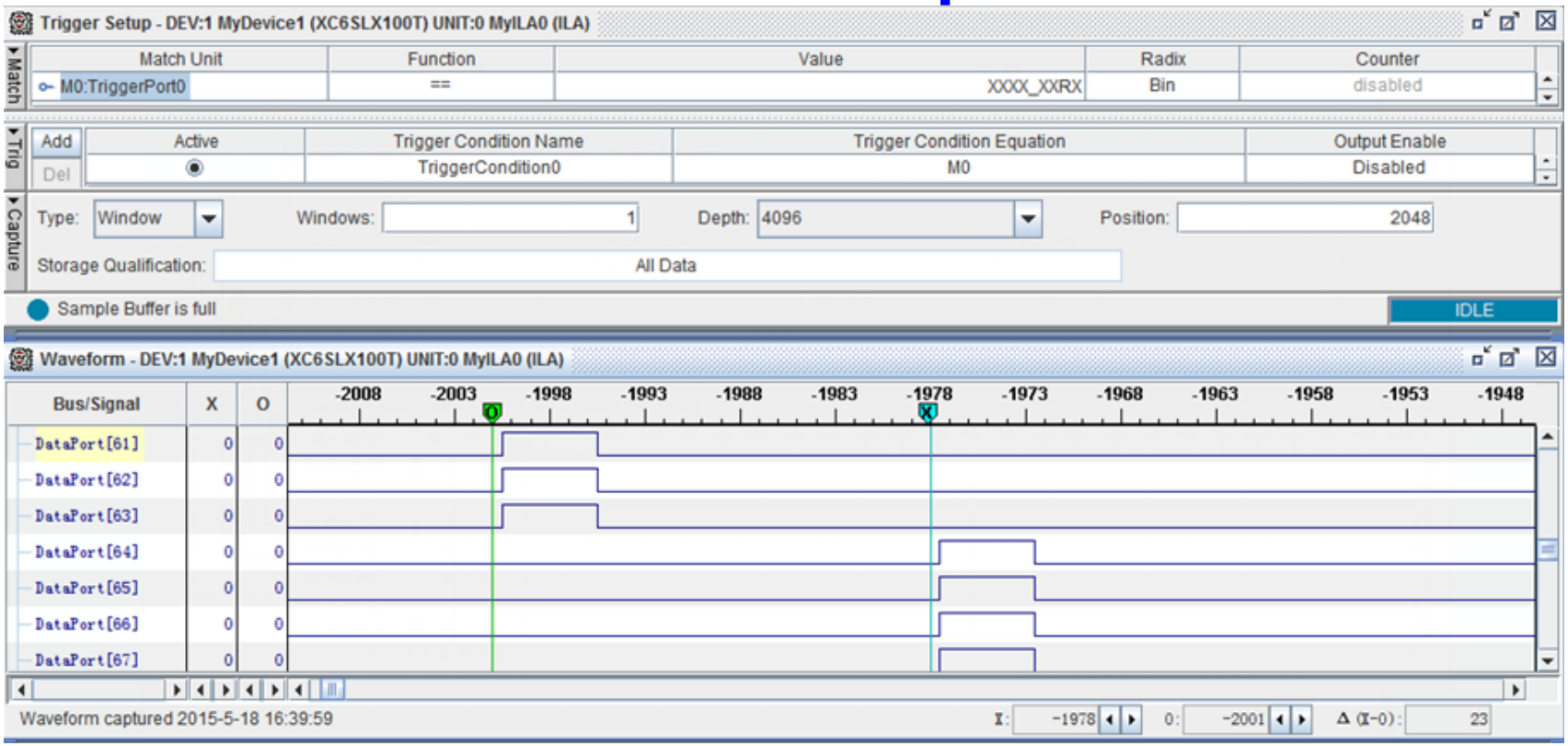
Time consumption



Delay Measurement of High Speed Serial Links : Diagram

Design and implementation of FPS

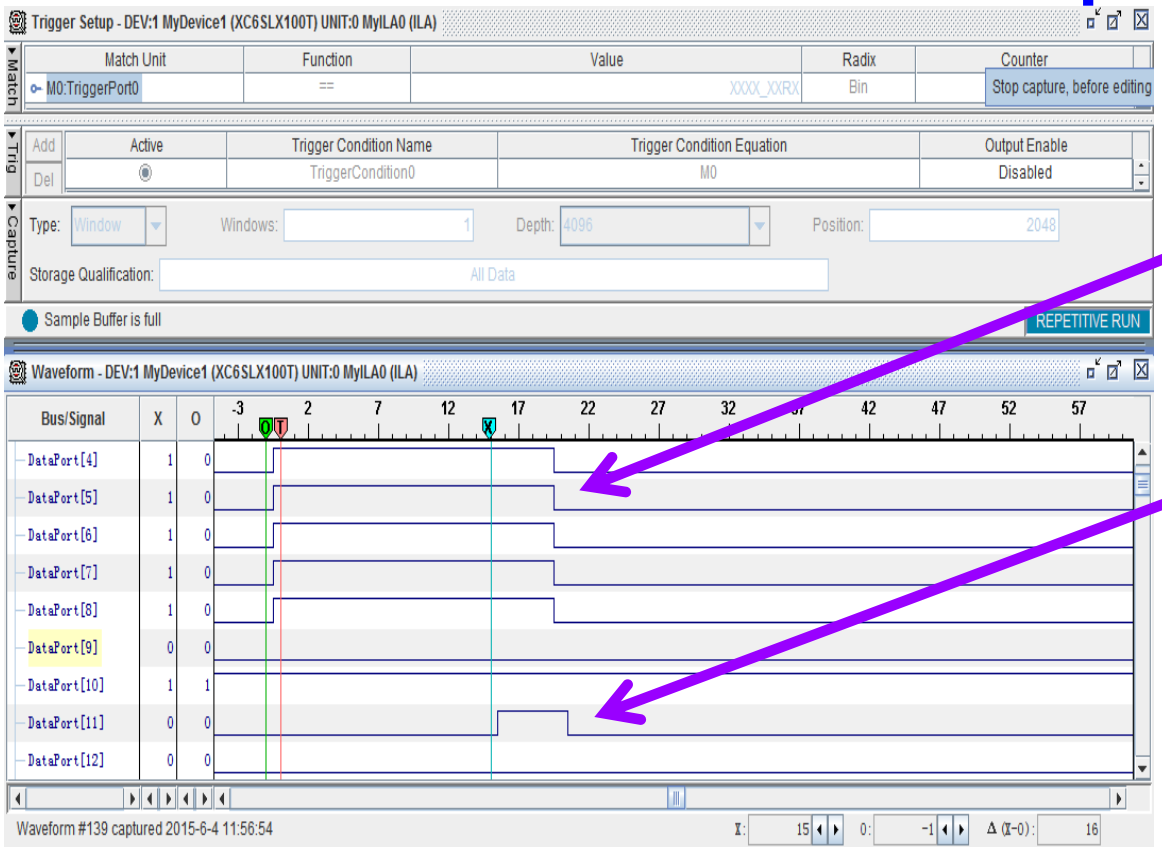
Time consumption

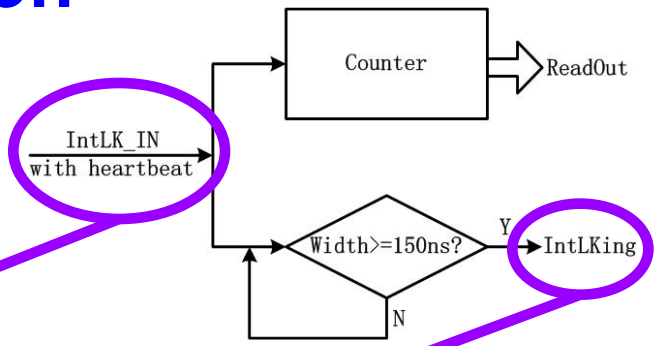


Delay Measurement of High Speed Serial Links : ~230ns
(23 clock cycles, clock period : 10ns)

Design and implementation of FPS

Time consumption





Signal width : 200ns

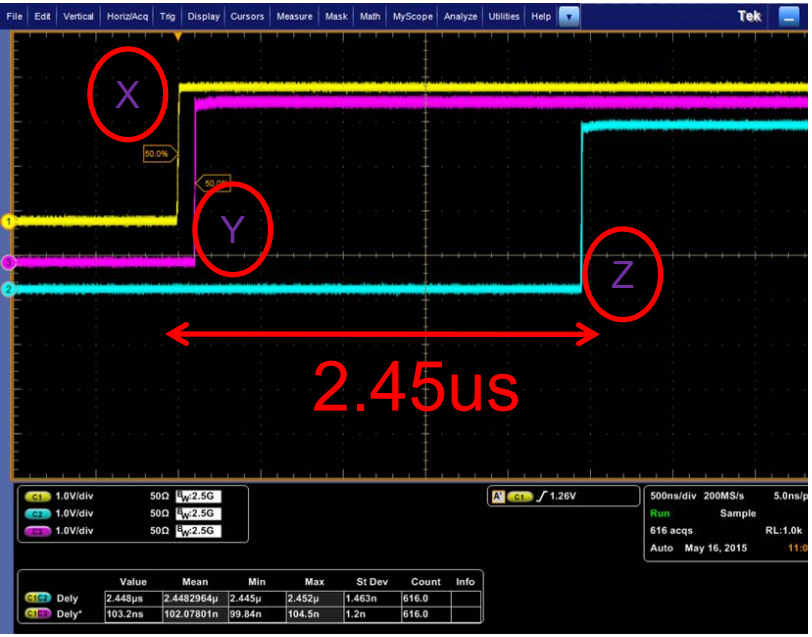
ChipScope Sampling clock : 100MHz

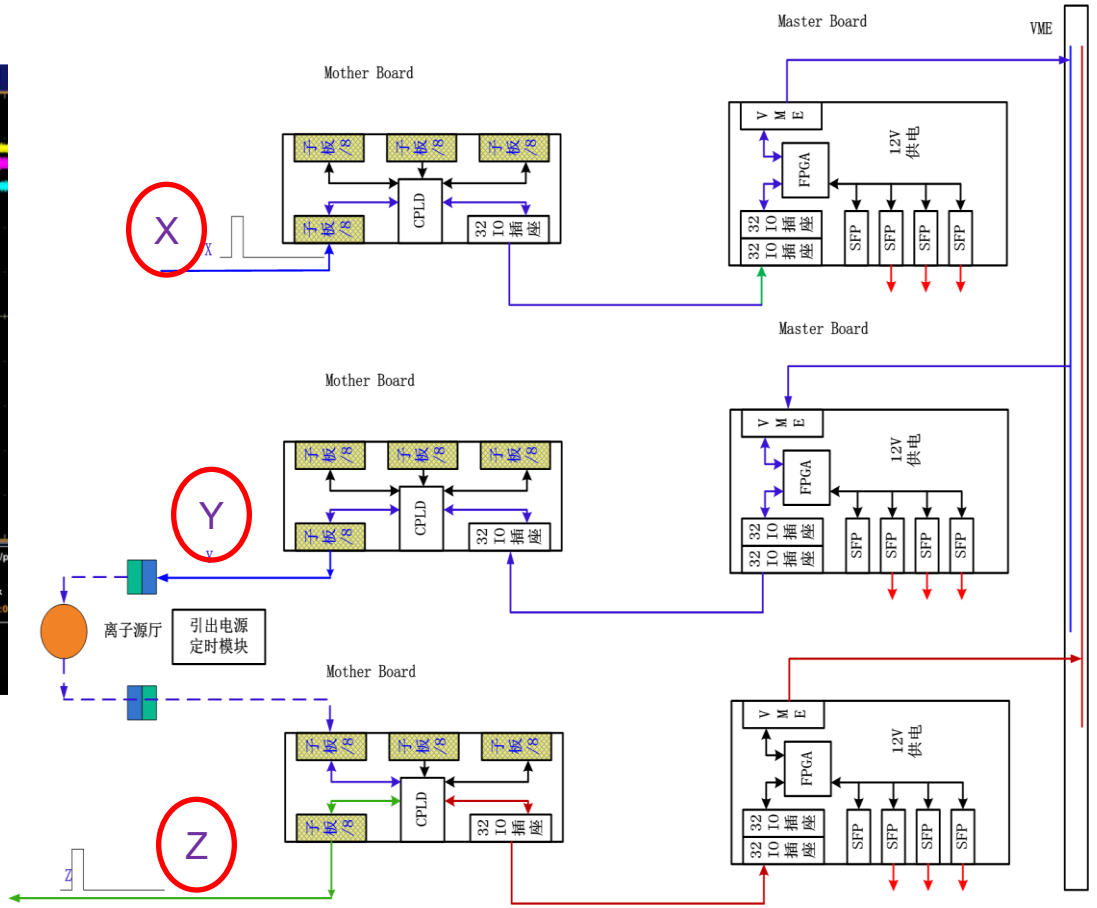
Delay Measurement of main logic with heart-beat: ~180ns

(150ns width check + 1clk register + backplane delay + IO delay)

Design and implementation of FPS

Time consumption

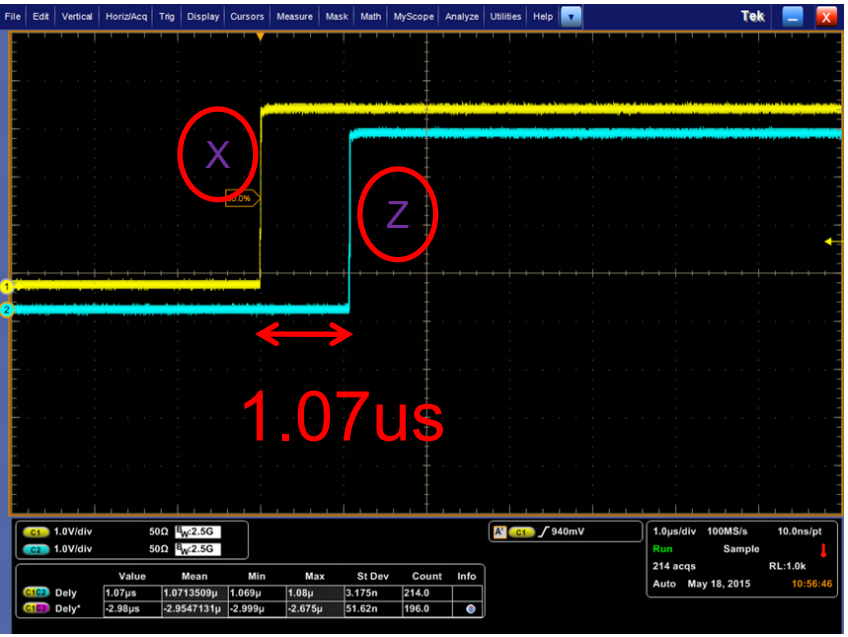


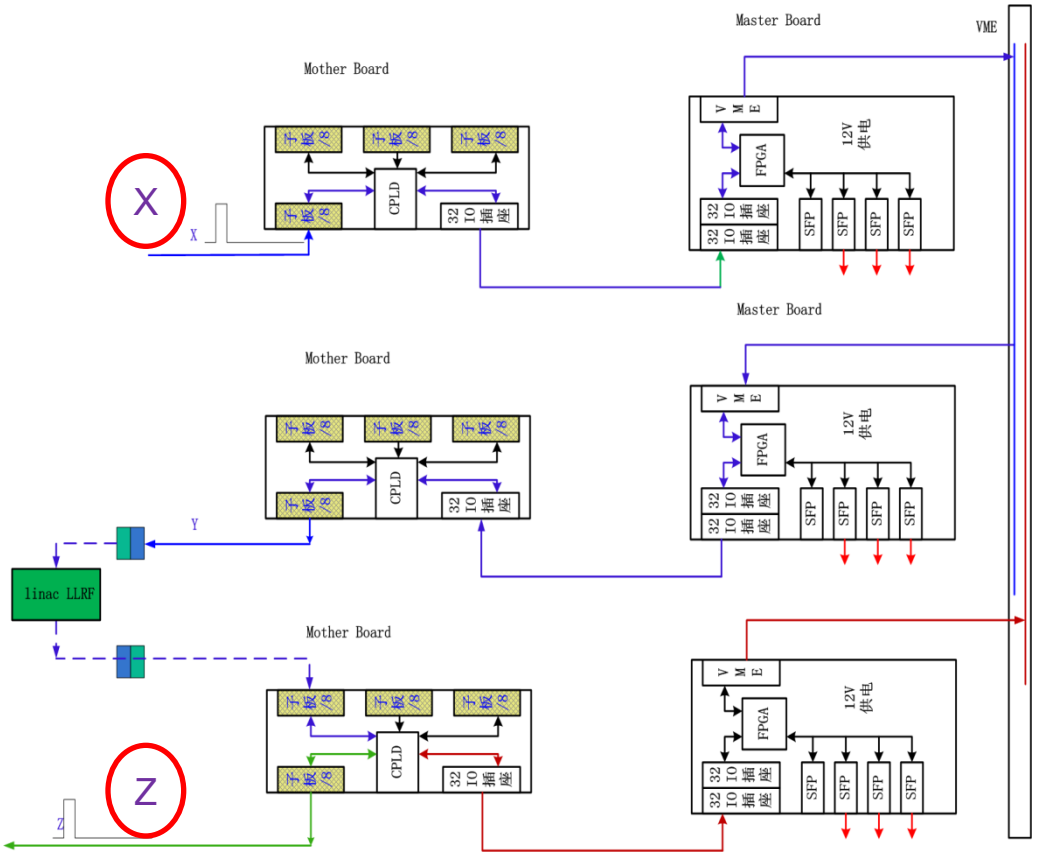


From Interlock to IS extraction timing stop :
~1.3μs (Mainly fiber delay)

Design and implementation of FPS

Time consumption

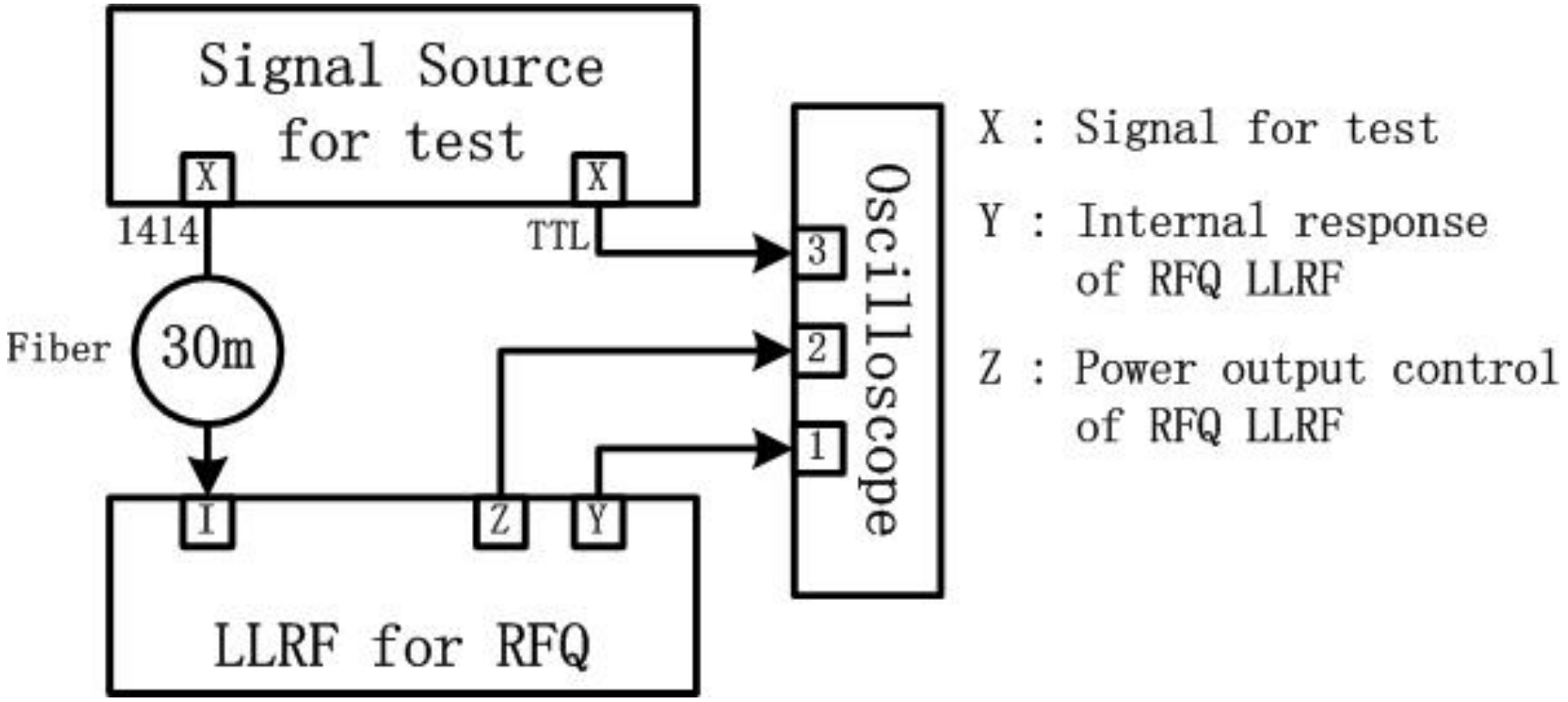




From Interlock to RFQ
RF interlock input :
~0.6μs (Mainly fiber delay)

Design and implementation of FPS

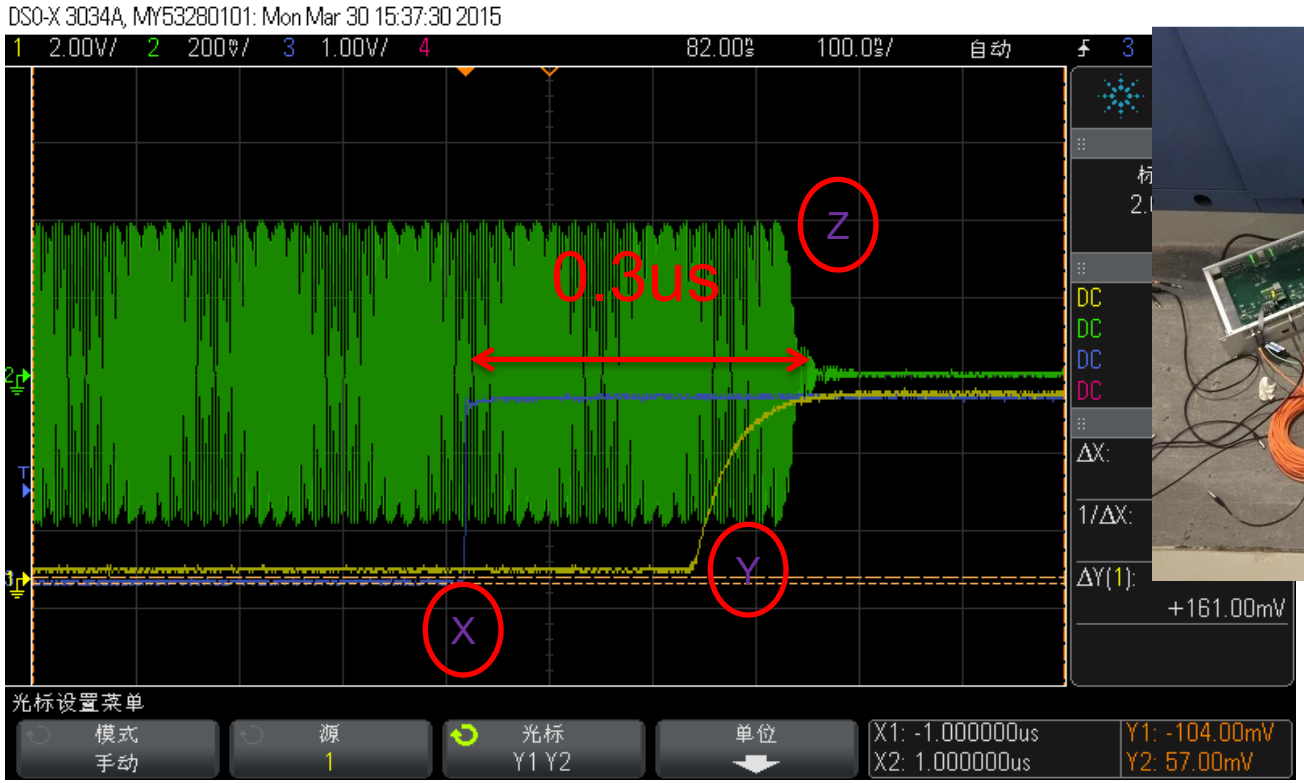
Time consumption

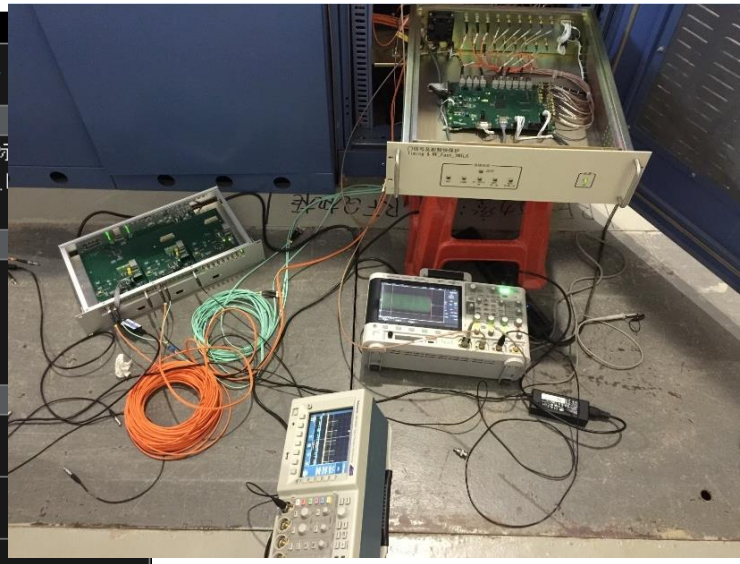


Response time of RFQ LLRF from interlock to stop power : Diagram

Design and implementation of FPS

Time consumption





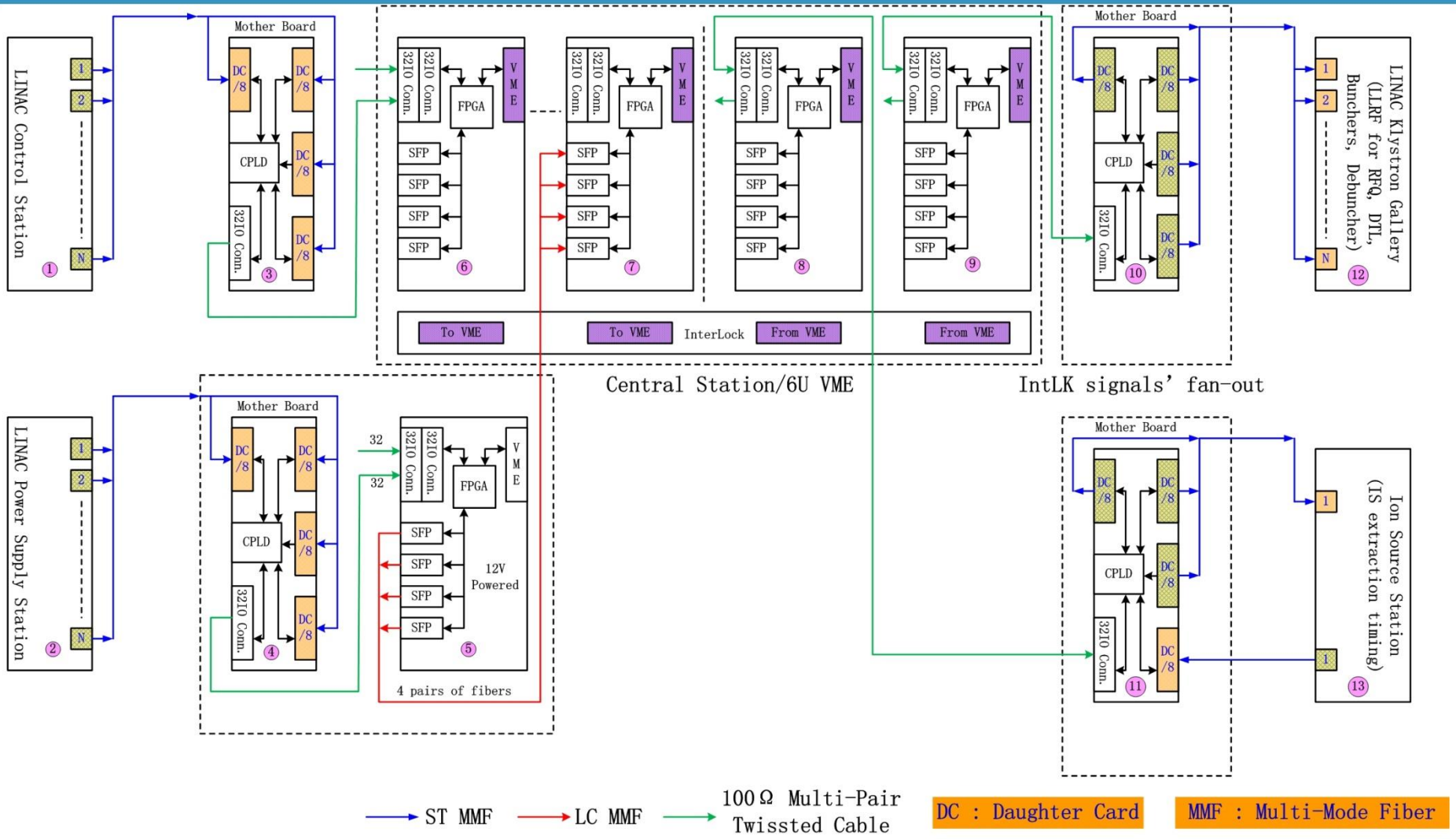
Response time of RFQ LLRF from interlock to stop power : ~150ns (300ns – (delay of 30m fiber))

Design and implementation of FPS

Time consumption

- **Maximum time consumption :**

Critical paths : from ② to ⑫ and to ⑬



Critical paths : from ② to ⑫ and to ⑬

Design and implementation of FPS

Time consumption

- **Critical paths :**

②=>④ : 20m fiber : delay 100ns;

④=>⑤ : Board/1.5m cable : delay ~50ns;

⑤=>⑦ : 90m fiber/high speed serial link : delay : 450ns + 230ns = 680ns;

⑦=>⑧ : Hear beat check/IO/Backplane : delay : ~180ns;

Design and implementation of FPS

Time consumption

- **Critical paths :**

⑦=>⑨ : Almost same as ⑦=>⑧ : ~180ns;

⑧=>⑪ : Almost same as ④=>⑤ : ~50ns;

⑨=>⑩ : Almost same as ⑧=>⑪ : ~50ns;

⑪=>⑬ : ~1.3μs (~220m fiber/board);

Design and implementation of FPS

Time consumption

- **Critical paths :**

⑩=>⑫ : 600ns + 150ns = 750ns (~100m fiber …)

②=> ⑫ (Interlock to RFQ power), total 1.8μs.

②=> ⑬ (Interlock to IS extraction timing), total 2.4μs.

Design and implementation of FPS

Time consumption

- **Critical paths :**

  Response time of power supplies to FPS is [2.8, 3.4]μs.

  So, total response time (Interlock source, FPS, actuator) is [4.6, 5.2] μs.

Design and implementation of FPS

Time consumption

- **Beam Loss Monitors :**

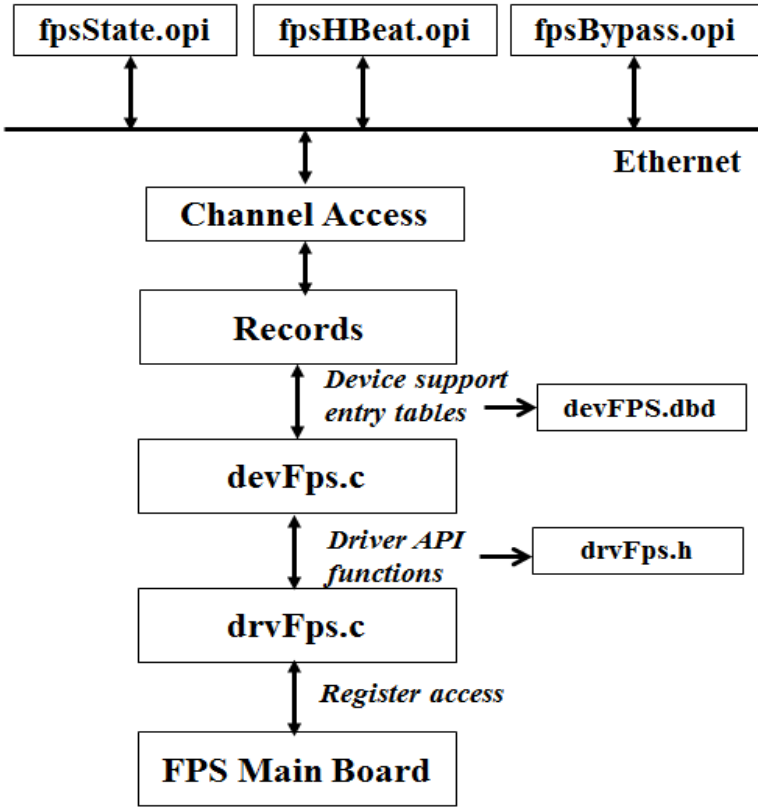
  Response time of Beam Loss Monitors are below 10μs.

  So, total response time (Interlock source, FPS, actuator) is 11.8μs.

Design and implementation of FPS

Software development

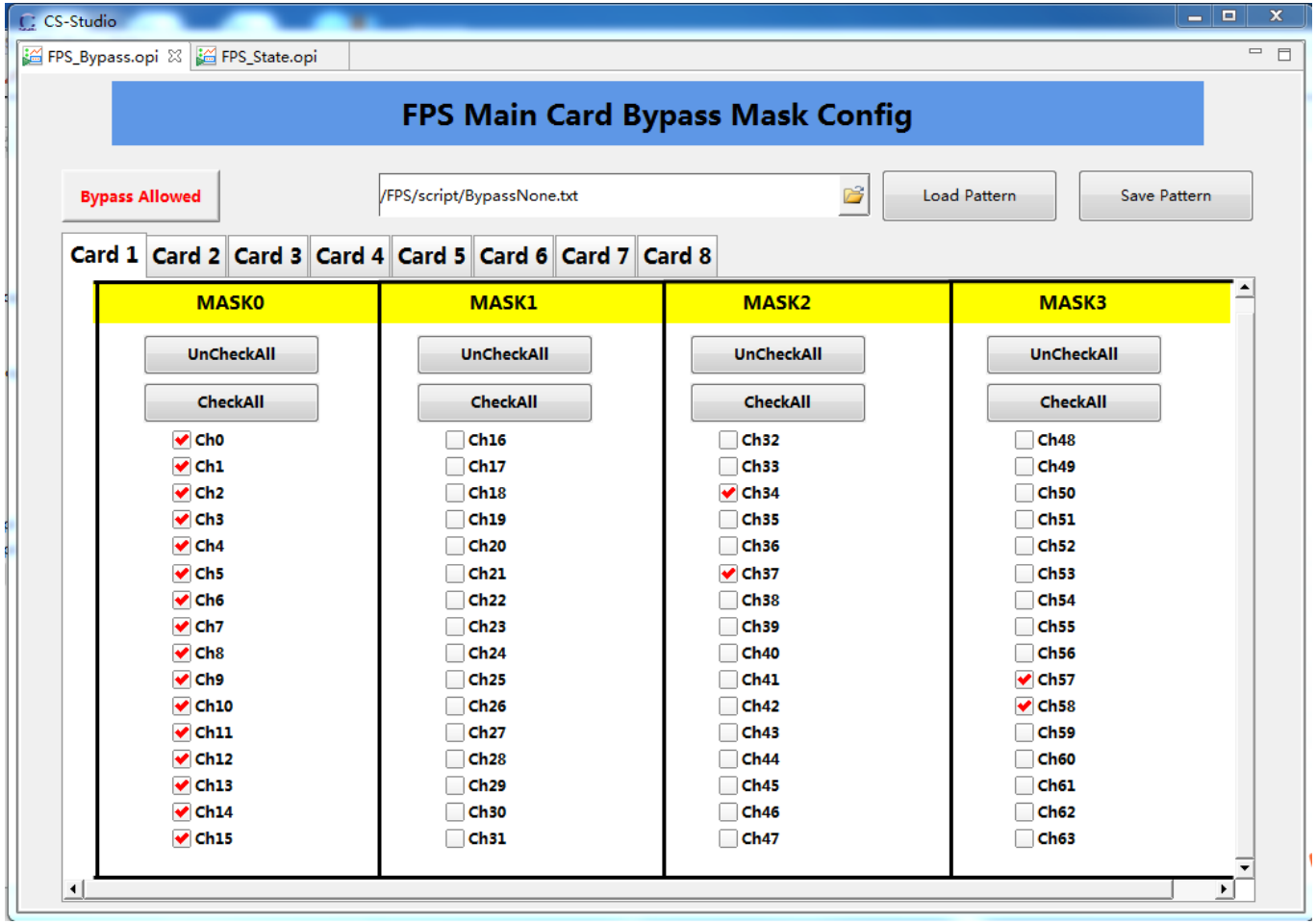
- IOC : VME 5100/VxWorks
- Periodic readout and comparison.
- Stronger controller may be used later.



FPS EPICS software diagram

Design and implementation of FPS

Software development

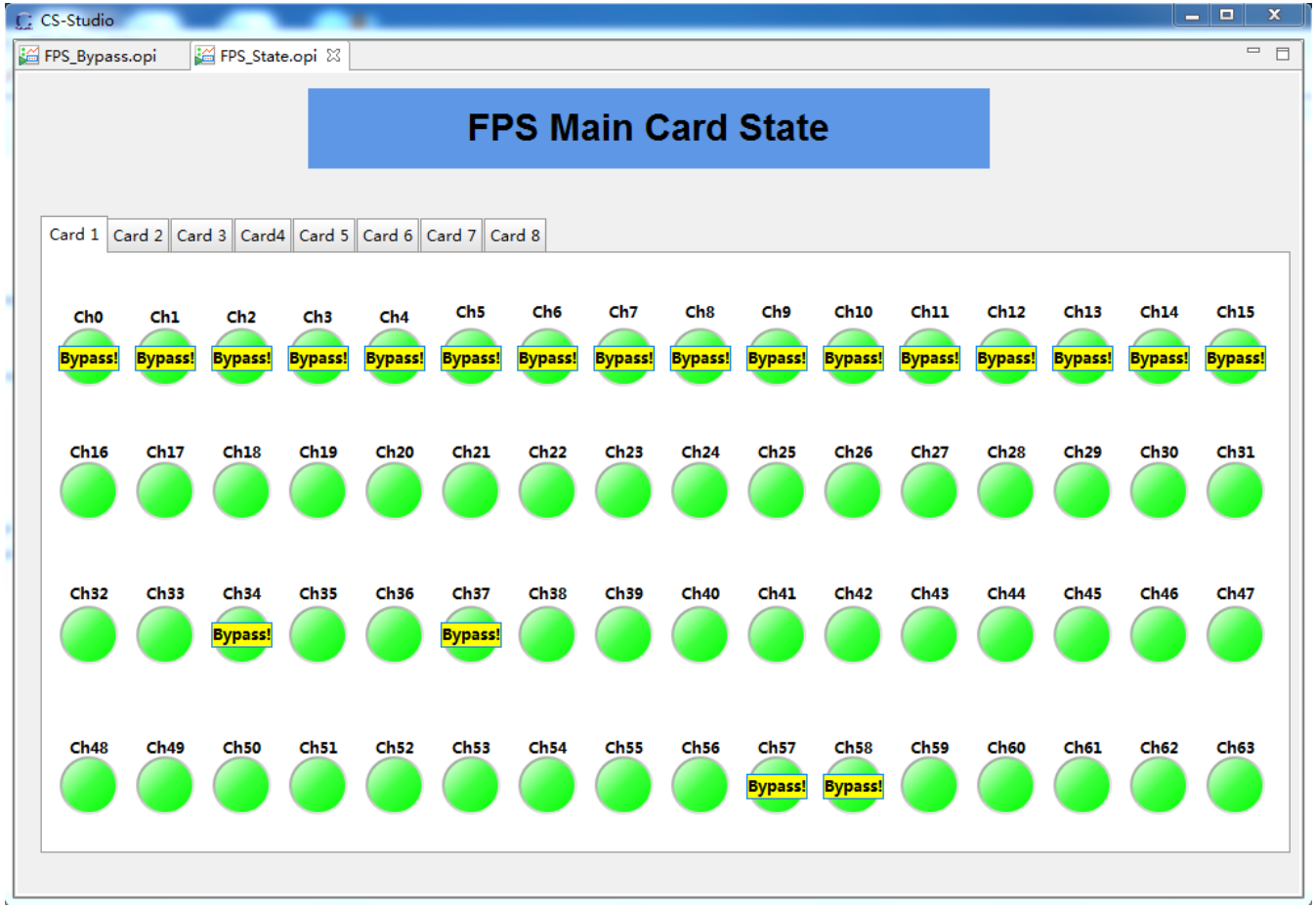


Design and implementation of FPS

Software development

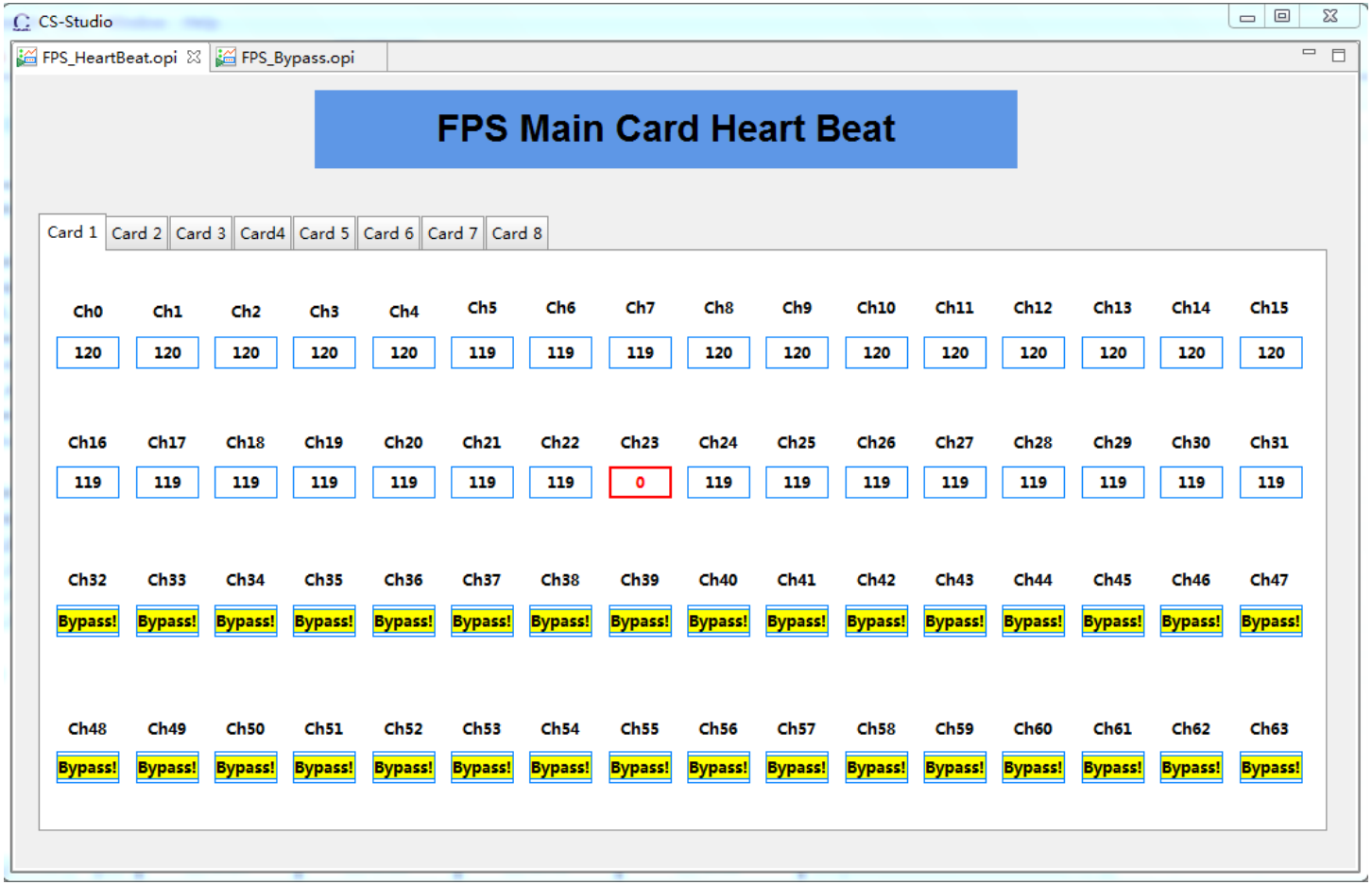
Design and implementation of FPS

Software development



Design and implementation of FPS

Software development



Next to do

- Whole function test for FPS in field will be done around October, 2015 during the installation of DTL1.
- Whole system of FPS will be settled and put into use around November, 2015.

Summary

- Machine protection requirements and design of the fast protection system are introduced.
- Till now, the system can fulfill the requirements after preliminary tests.
- Backup connections for FPS will be routed to the RCS building for possible fast protection connections in the future.

Summary

- Part of the protection system has been settled, further test and implementation will start soon.

All suggestions are welcome!

Thanks a lot!