Design and Implementation of the Fast Protection System for CSNS

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Outline

- Brief introduction to CSNS (China Spallation Neutron Source)
- Fundamental safety requirements
- Basic design considerations and rules
- Overall design
- Design and implementation of FPS (Fast Protection System)
Outline

● **Next to do**

● **Summary**
Brief introduction to CSNS
Brief introduction to CSNS

Injection/Stripping

Neutron instruments

$P_D = 100 \text{ kW}$

Target station

$1.6 \text{ GeV}, 62.5 \mu\text{A}, 25\text{Hz}$

RCS
Brief introduction to CSNS

Injection/Stripping

Acceleration

Neutron instruments

Target station

P_B = 100 kW
Brief introduction to CSNS

Injection/Stripping

Acceleration

Neutron instruments

$P_T = 100 \text{ kW}$

Target station

$1.6 \text{ GeV}, 62.5 \mu \text{A}, 25\text{Hz}$
Brief introduction to CSNS

Injection/Stripping

Acceleration

Neutron instruments

$P_B = 100 \text{ kW}$

Target station

1.6 GeV, 62.5 $\mu$A, 25 Hz
Brief introduction to CSNS

Innovation/Stripping

Acceleration

RCS

1.6 GeV, 62.5 μA, 25 Hz

Extraction

Neutron instruments

P₀ = 100 kW

Target station
Brief introduction to CSNS

Injection/Stripping

Acceleration

Extraction

Target Station

Target station

Neutron instruments

P_T = 100 kW

RCS

1.6 GeV, 62.5 μA, 25 Hz

DTL

MEBT

RFQ

H-IS

RFQ

LEBT

LRBT

324 MHz

324 MHz

50 keV 3 MeV

I_p = 20 mA
Brief introduction to CSNS

Injection/Stripping

Acceleration

Collimation

Extraction

Target Station

Neutron instruments

P_b = 100 kW

Target station

RCS

1.6 GeV, 62.5 μA, 25 Hz
Fundamental safety requirements

- To prevent permanent damage to materials due to a heat deposition exceeding their thermal stress limit of accelerator components along the beam line, especially for copper in DTL (Drift Tube LINAC).
Fundamental safety requirements

1. Un-chopped beam, 15mA
2. Beam size: 0.2cm * 0.2cm RMS
3. Hitting the components directly

17µs $\Rightarrow$ 5µs due to Bragg Peak $\Rightarrow$ 10µs if chopped

Critical most cases
Basic design considerations and rules

- Reliable and mature industrial and commercial products should be used when available.
- All interfaces should be fail-safe or online real-time checked to make sure the reliability.
- Interlock logic should be as simple as possible and developed with reliable tools.
- Considerations: reliability, maintainability, stability, scalability and flexibility.
Overall design

Inputs classification

- Failure of components along the beam line below 50keV (before RFQ) will not bring severe damage due to the lower beam energy and the loss of H- in RFQ. These signals are delivered to MPS, a protection system of ms response time.
Overall design

Inputs classification

Failure of components from RFQ to the end of DTL will possibly bring great damage, especially to the copper of the drift tubes since their small diameter. These signals are delivered to FPS. BLM (Beam Loss Monitor) signals in this region are also delivered to FPS. Two BLM signals on the LRBT are also delivered to FPS to protect the de-buncher.
Overall design

Distribution of BLMs
Overall design

Distribution of BLMs

Red ones for FPS
The others for MPS

Response time of BLM: 10μs

Scintillators used for low energy line
Ion chambers used for others

Target Station

R-DUMP

L-DUMP

LRDMP1
Overall design

System architecture
Overall design

Technique selection

For FPS, a response time of around $5\mu$s, low level signal and FPGA (Field Programmable Gate Array) should be used to fulfill the critical requirement, and to provide good flexibility.
Overall design

Structure and distribution of FPS
Overall design

How to stop the beam and recover

- Sending out interlock signals to stop the RFQ radio frequency power, to stop the beam gate signals to all the LINAC radio frequency powers, to stop the timing signal to the ion source extraction power supply, to turn down the high voltage of the ion source power supply from 17kV to 10kV at the same time.
Overall design

How to stop the beam and recover

- To recover the RFQ radio frequency power to maintain RFQ resonance after either the timing signal of the ion source extraction power supply stopped or the high voltage of it turned down.

- To recover the timing signal of the ion source extraction power supply after its high voltage turned down.
Overall design

How to stop the beam and recover

- The accelerator can recover from the interlock state after hand reset from the MPS with the faults cleared. Otherwise, beam is not permitted.
Overall design

How to stop the beam and recover

- FPS
- Interlock
- Feedback
- Reset
Overall design

How to stop the beam and recover

IS Extraction Timing
IS HV Control Below 10kV?
RFQ Power
LLRF Beam Gate

Interlock  Feedback  Reset
Overall design

How to stop the beam and recover

- IS Extraction Timing
- IS HV Control Below 10kV?
- RFQ Power
- LLRF Beam Gate

Interlock  ➔  Feedback  ➔  Reset
Overall design

How to stop the beam and recover

- IS Extraction Timing
- IS HV Control Below 10kV?
- RFQ Power
- LLRF Beam Gate

- Interlock
- Feedback
- Reset
Overall design

How to stop the beam and recover

- IS Extraction Timing
- IS HV Control Below 10kV?
- RFQ Power
- LLRF Beam Gate

- Interlock
- Feedback
- Reset
Overall design

How to stop the beam and recover

- IS Extraction Timing
- IS HV Control Below 10kV?
- RFQ Power
- LLRF Beam Gate

Interlock → Feedback → Reset
Overall design

How to stop the beam and recover

- IS Extraction Timing
- IS HV Control Below 10kV?
- RFQ Power
- LLRF Beam Gate

Arrows indicate:
- Interlock
- Feedback
- Reset
Overall design

How to stop the beam and recover

- IS Extraction Timing
- IS HV Control Below 10kV?
- RFQ Power
- LLRF Beam Gate

- Interlock
- Feedback
- Reset
Overall design

How to stop the beam and recover

• Figure.
Design and implementation of FPS

- FPGA chip XC6SLX100T-3FGG900 from Xilinx is chosen as the main component for the FPS. Total 8 GTPs (Gigabit Transceiver Port, RocketIO), maximum 480 user IOs, ~100k logic cells …

- Central station: 6U VME 64x crate with 21 slots. Some user IOs for specific applications.
Design and implementation of FPS

- Signals collection in front end near interlock sources, with single core fibers for ground isolation. Signals to central stations through high speed serial links (GTP + opt. transceivers + opt. fibers) to reduce the number of fiber cores, to ease system installation, maintenance and upgrade.
Design and implementation of FPS

Fiber and High Speed Serial Transmission based connection

Auto-Synchronziation

1 pair fibers carrying 16 signals

Central integration and treatment in 6U VME crate
Design and implementation of FPS

Daughter card

Main board

Mother board

Signals’ collection and transmission
Central station/6U VME
IntLK signals’ fan-out

DC: Daughter Card  MMF: Multi-Mode Fiber

ST MMF  LC MMF

100Ω Multi-Pair Twisted Cable
Design and implementation of FPS

- +12V
- UART
- Opt. transceivers/Rocketl/Os/6
- Gb net
- Extended IOs/64
- Lamp indicators/8
- DDR2 SODIMM
- FPGA/XC6SLX 100T-3FGG900
- CPU/Loongson 2F
- VME P1/P2
- PWR: VME +5V or ext. +12V
Design and implementation of FPS

Mother Board

Main Board

OP adaptor
Design and implementation of FPS

- Opt. adaptor
- Opt. transceiver
- Main Board
  - VME
- IS Mother Board
- MPS Mother Board
- Timing Mother Board
- LLRF Mother Board
- LLRF Mother Board
- BLM Mother Board
- FPS Central Station
- Field photo
- OPI
Design and implementation of FPS

- Mother Module
- Main board
- Orderliness
- Multimode fiber

Opt. adaptor
Opt. transceiver

Cabinet front
Cabinet rear
Design and implementation of FPS

Interlock output of each main board will transmit to the backplane, then all boards in crate receive it.
Design and implementation of FPS
Signals to/from the backplane with redundant components and routes
(Two and-or gates 74F38 are used, each for 4 signals to backplane)
Design and implementation of FPS

Safety issues

- Interface fail-safe definition: Avago optical transmitter 1414 and receiver 2412 are used for interlock inputs. Normal conditions are defined as the 1414 gives light out, interlock occurs when no light.

- Periodic heart-beat function are designed to make sure the safety of the signal route from the front end collection to the main station.
Design and implementation of FPS

Safety issues

Heart-beat signal generation in the CPLD on the daughter card of front end

Heart-beat signal check and counting in the FPGA on the main board at central station
Design and implementation of FPS

Safety issues

- Continuous readout and comparison of the interlock registers, the channel-mask registers and the heart-beat counters in the FPGA on the main boards at central station to make sure the proper work of the whole system, alarms will be given out when any error.

- Alarm when the VME crate power off.
Design and implementation of FPS

Safety issues

- Interlock signals to the RFQ RF, the IS extraction timing, the IS extraction HV control go through independent routes from the central station. Any of which fails will not affect the others’ functions.
Design and implementation of FPS

Logic development and test

- Auto-synchronization function of the high speed path and bit error rate.

- When both fibers of the same high speed transceiver pair are plugged in, serial data are automatically de-serialized to parallel data.

- Bit error rate test is done with pseudo random data generated in the FPGA logic.
Design and implementation of FPS

Bit Error Rate test
Design and implementation of FPS

- VME powered module
- Opt. transceiver
- +12V powered module

No errors in 27 hours
Design and implementation of FPS

Logic development and test

● Heart-beat function.

Signal width: 100ns
ChipScope Sampling clock: 100MHz

Counter

ReadOut

IntLK_IN

with heartbeat

Width >= 150ns?

IntLKING
Design and implementation of FPS

Logic development and test

Heart-beat function.

ChipScope Sampling clock: 100MHz

Signal width: 200ns
Design and implementation of FPS

Logic development and test

- Interlock function. Till now, signals connected are MEBT and DTL power supplies, MPS related, IS extraction timing and IS extraction HV control.

- Function test of RFQ RF power interface has been done electrically, but not connected.
Design and implementation of FPS

Logic development and test

● Till now, all signals connected have been tested one by one with ChipScope monitoring in the FPGA, including the feedback signals from the IS extraction timing and the IS extraction HV control.

● Interlock signal to the RFQ RF power is cancelled when either of the feedback signals is OK.
Design and implementation of FPS

Time consumption

- Time consumption includes delays in the fibers/cables and delays in the boards.
- Main delay is due to the length of optical fibers.
Design and implementation of FPS

Time consumption

Delay Measurement of High Speed Serial Links: Diagram
Design and implementation of FPS

Time consumption

Delay Measurement of High Speed Serial Links: \(~230\text{ns}\)
(23 clock cycles, clock period: 10\text{ns})
Design and implementation of FPS

Time consumption

Delay Measurement of main logic with heart-beat: \( \sim 180\text{ns} \)

\((150\text{ns width check} + 1\text{clk register} + \text{backplane delay} + \text{IO delay})\)
Design and implementation of FPS
Time consumption

From Interlock to IS extraction timing stop:
~1.3 µs (Mainly fiber delay)
Design and implementation of FPS

Time consumption

From Interlock to RFQ
RF interlock input: 
~0.6μs (Mainly fiber delay)
Design and implementation of FPS

Time consumption

Response time of RFQ LLRF from interlock to stop power:

Diagram
Design and implementation of FPS

Time consumption

Response time of RFQ LLRF from interlock to stop power: ~150ns (300ns – (delay of 30m fiber))
Design and implementation of FPS

Time consumption

- Maximum time consumption:

Critical paths: from ② to (12) and to (13)
Critical paths: from ② to (12) and to (13)
Design and implementation of FPS

Time consumption

- Critical paths:
  
  ②=>④ : 20m fiber : delay 100ns;
  
  ④=>⑤ : Board/1.5m cable : delay ~50ns;
  
  ⑤=>⑦ : 90m fiber/high speed serial link : 
                 delay : 450ns + 230ns = 680ns;
  
  ⑦=>⑧ : Hear beat check/IO/Backplane : 
                 delay : ~180ns;
Design and implementation of FPS

Time consumption

● Critical paths:

⑦⇒⑨ : Almost same as ⑦⇒⑧ : ~180ns;
⑧⇒⑾ : Almost same as ④⇒⑤ : ~50ns;
⑨⇒⑩ : Almost same as ⑧⇒⑾ : ~50ns;
⑾⇒⑿ : ~1.3μs (~220m fiber/board);
Design and implementation of FPS

Time consumption

- Critical paths:
  - $10 \Rightarrow 12$: $600\text{ns} + 150\text{ns} = 750\text{ns} \approx 100\text{m fiber} \ldots$
  - $2 \Rightarrow 12$ (Interlock to RFQ power), total $1.8\mu\text{s}$.
  - $2 \Rightarrow 13$ (Interlock to IS extraction timing), total $2.4\mu\text{s}$.
Design and implementation of FPS

Time consumption

- Critical paths:

  Response time of power supplies to FPS is $[2.8, 3.4] \mu s$.

  So, total response time (Interlock source, FPS, actuator) is $[4.6, 5.2] \mu s$. 
Design and implementation of FPS

Time consumption

● Beam Loss Monitors:

Response time of Beam Loss Monitors are below 10μs.

So, total response time (Interlock source, FPS, actuator) is 11.8μs.
Design and implementation of FPS

Software development

- IOC : VME 5100/VxWorks
- Periodic readout and comparison.
- Stronger controller may be used later.

FPS EPICS software diagram
Design and implementation of FPS
Software development
Design and implementation of FPS
Software development
Design and implementation of FPS
Software development
Design and implementation of FPS
Software development

![FPS Main Card Heart Beat Diagram]
Next to do

- Whole function test for FPS in field will be done around October, 2015 during the installation of DTL1.

- Whole system of FPS will be settled and put into use around November, 2015.
Summary

- Machine protection requirements and design of the fast protection system are introduced.
- Till now, the system can fulfill the requirements after preliminary tests.
- Backup connections for FPS will be routed to the RCS building for possible fast protection connections in the future.
Summary

- Part of the protection system has been settled, further test and implementation will start soon.

All suggestions are welcome!

Thanks a lot!