Global Trigger with Vertex Fit for low energy neutrino research

--- concept and preliminary study

Guanghua Gong, Hui Gong

Dept. of engineering Physics, Tsinghua University

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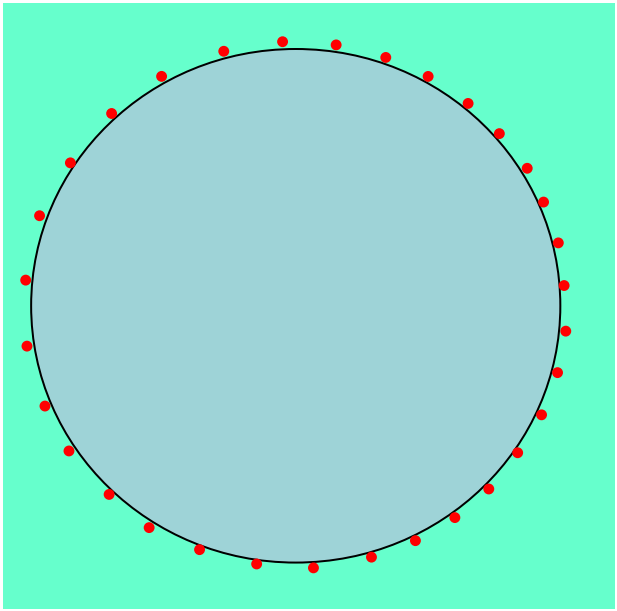
Neutrino experiments

- Important for particle physics, astrophysics and cosmology
- Key points for neutrino experiment
  - Low background
    - underground, low radioactive materials
  - Large detection volume
    - 20kt LS for JUNO
  - High photon collection efficiency
    - High light yield and high transparent LS
    - Coverage, large quantity of HPE PMT

PMT hit distribution



Basic numbers:

- Ø37m sphere vessel
- ~ 15000 20” PMT
- 50K dark noise (new MCP PMT)

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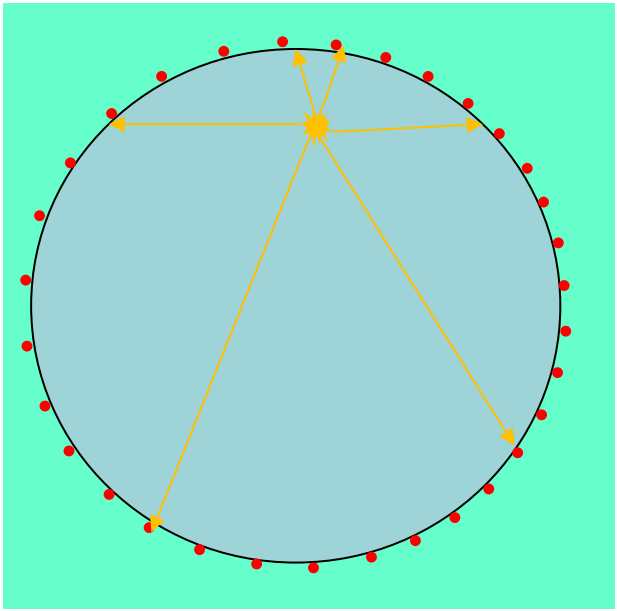

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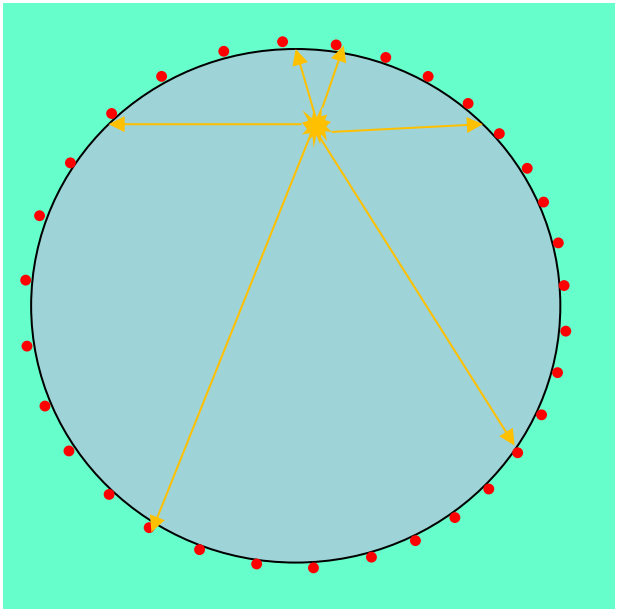

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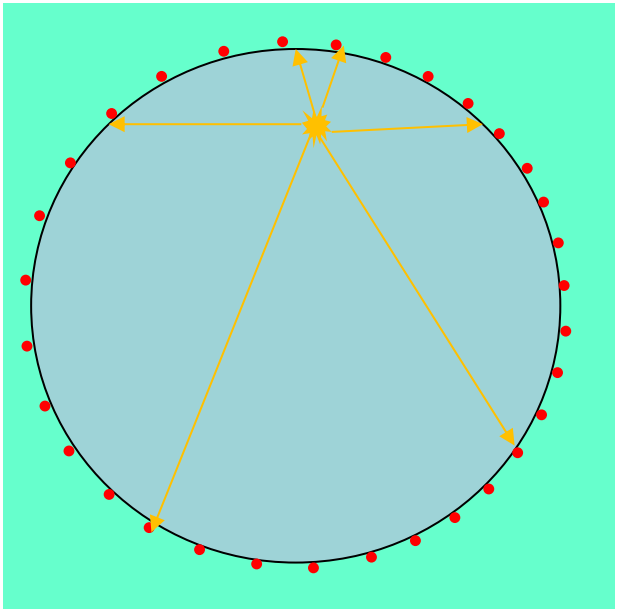

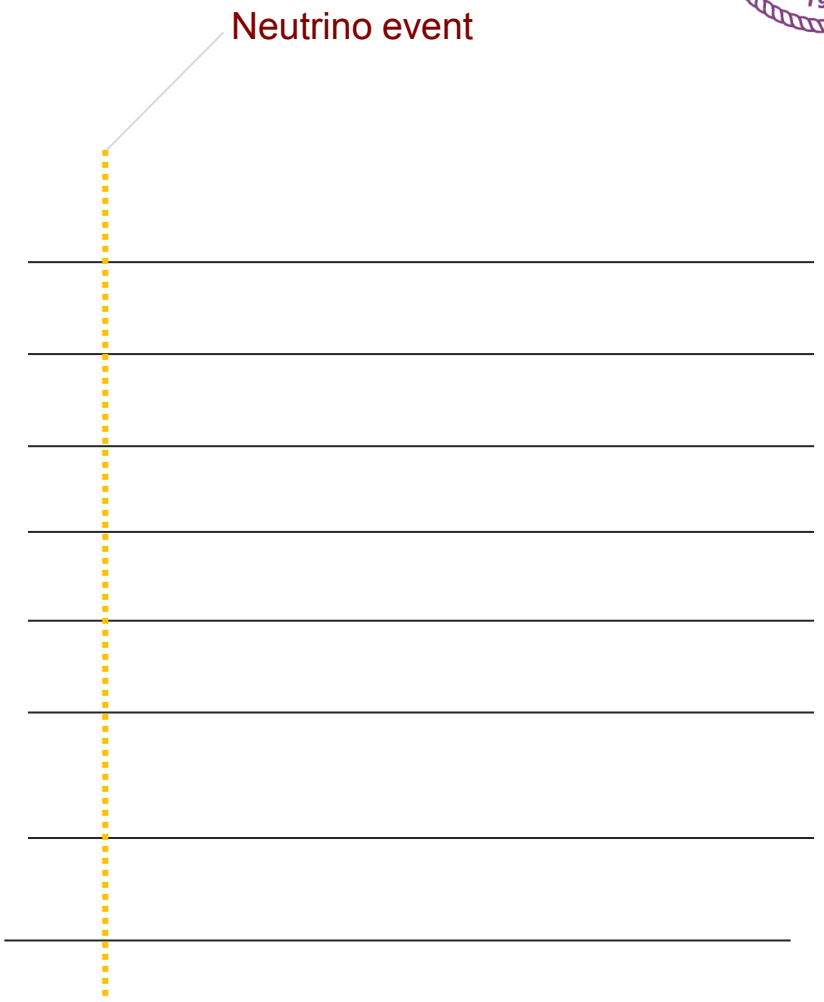

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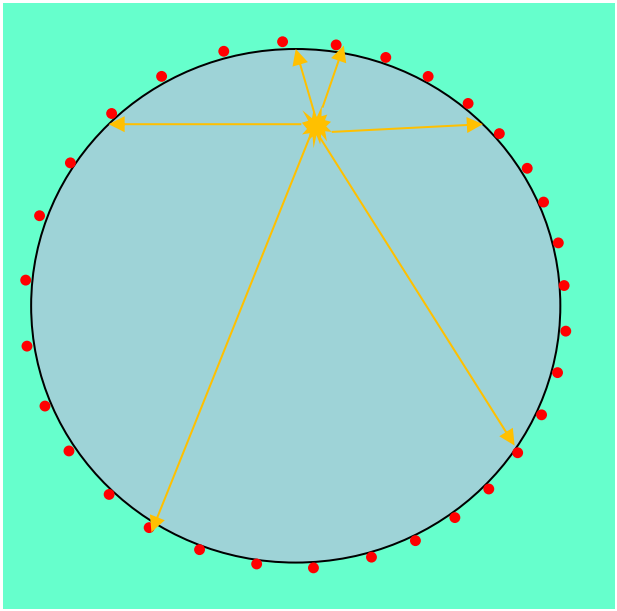

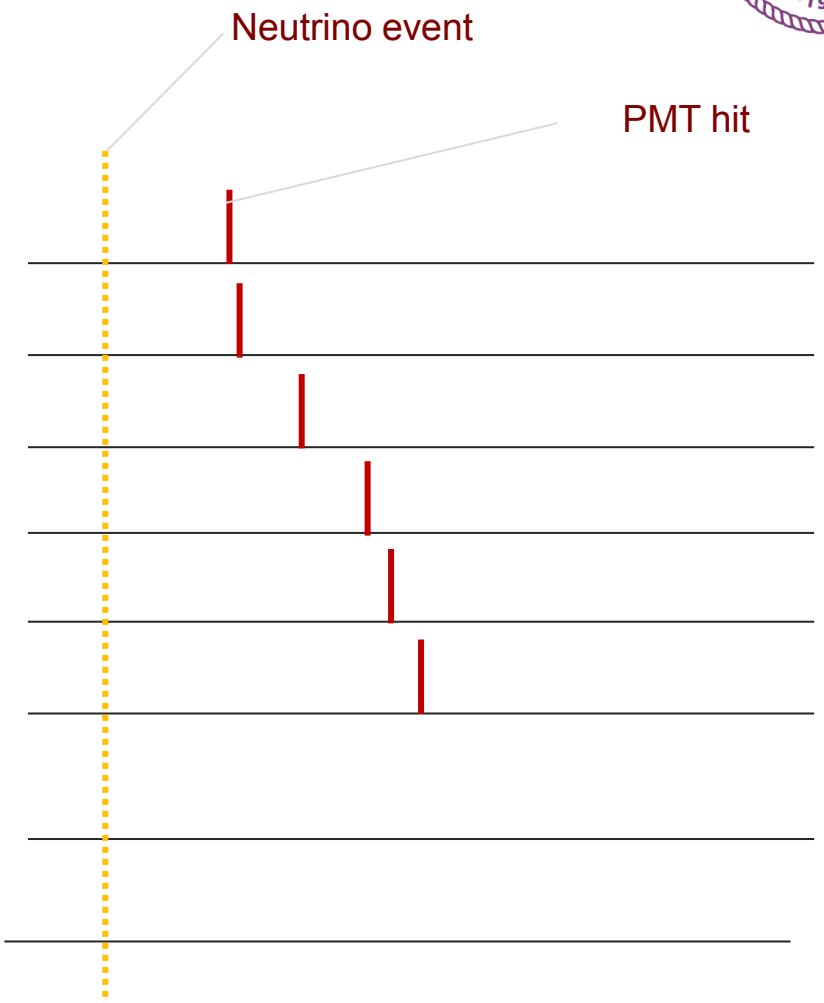

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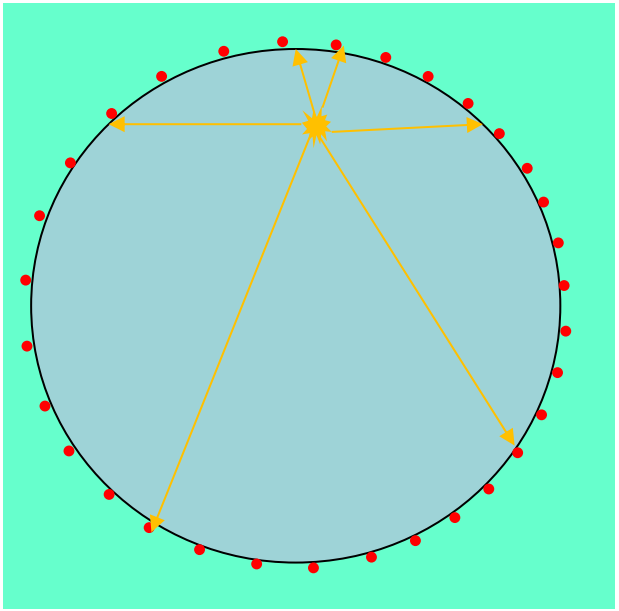

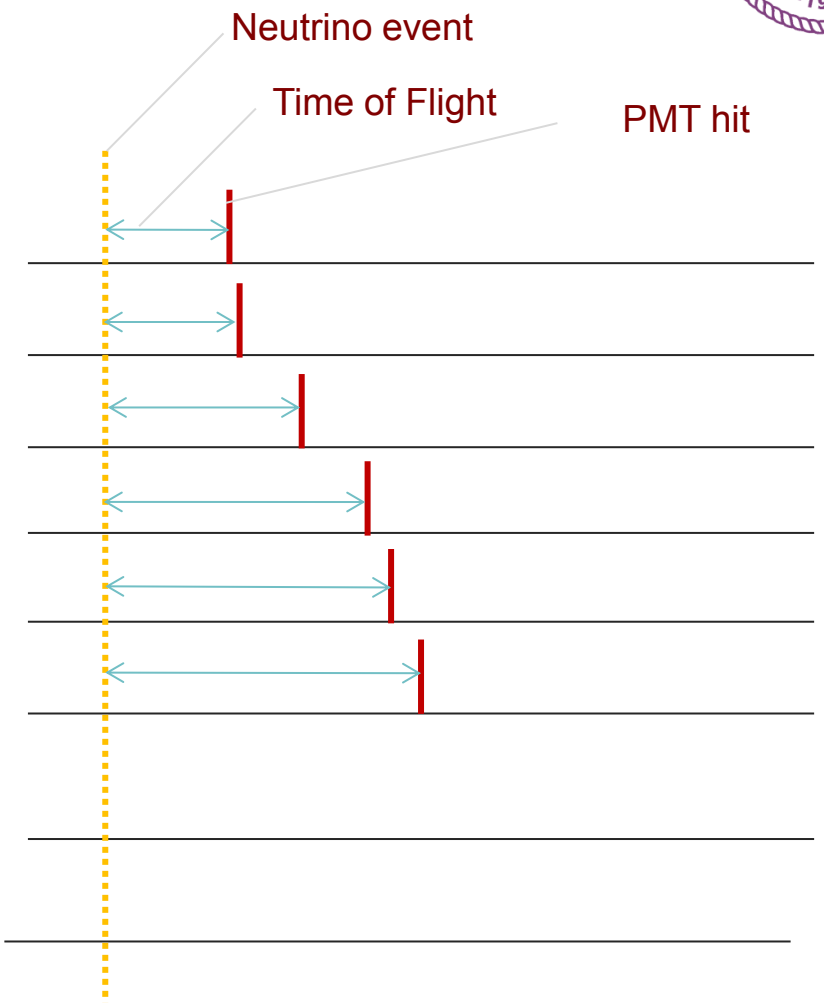

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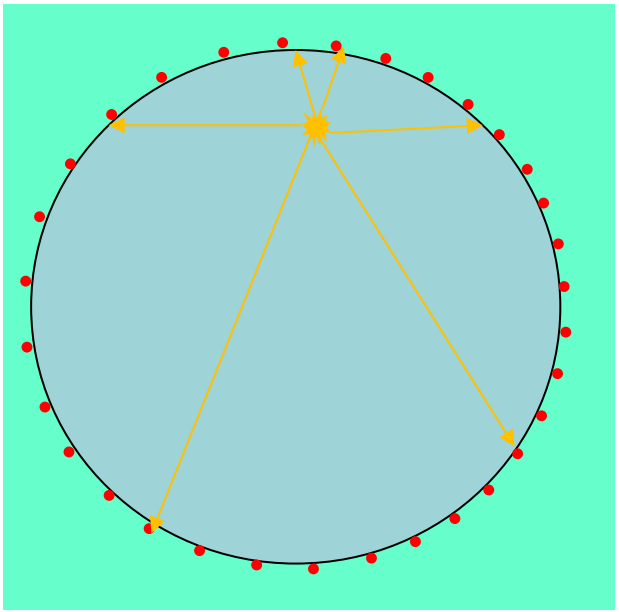

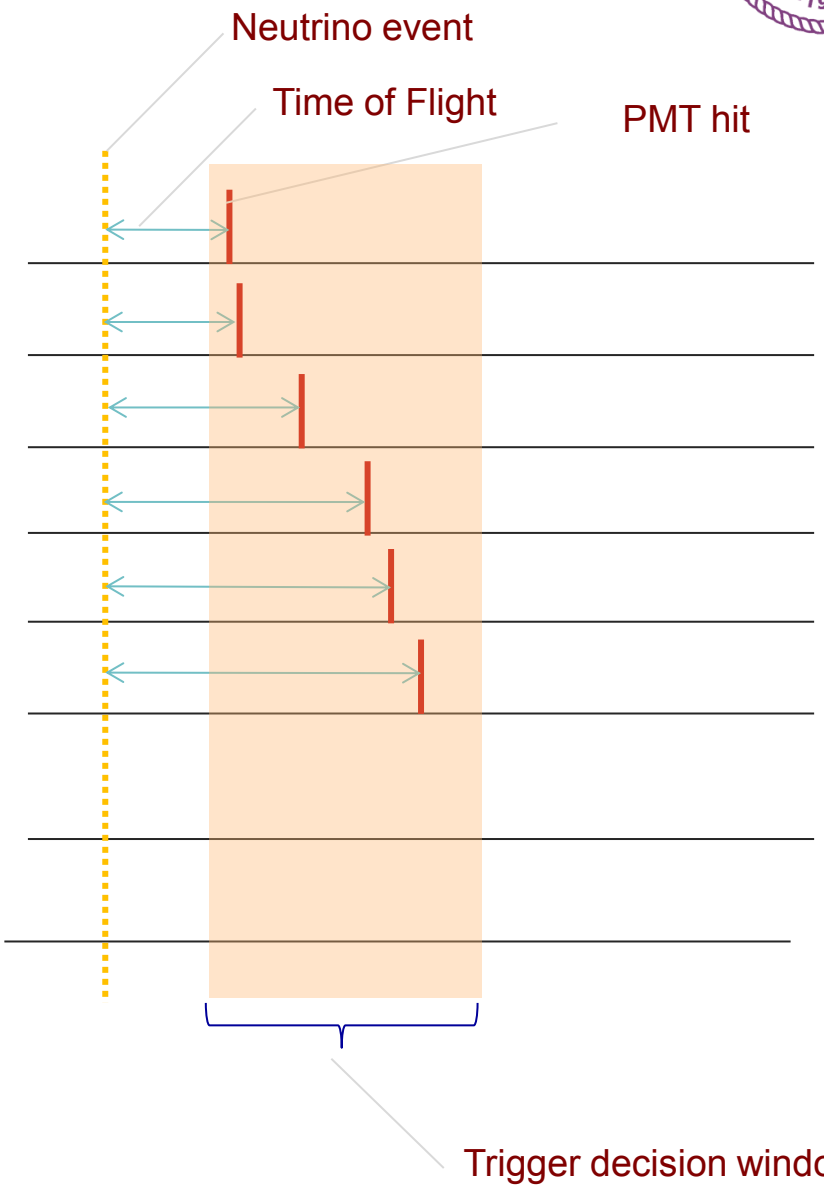

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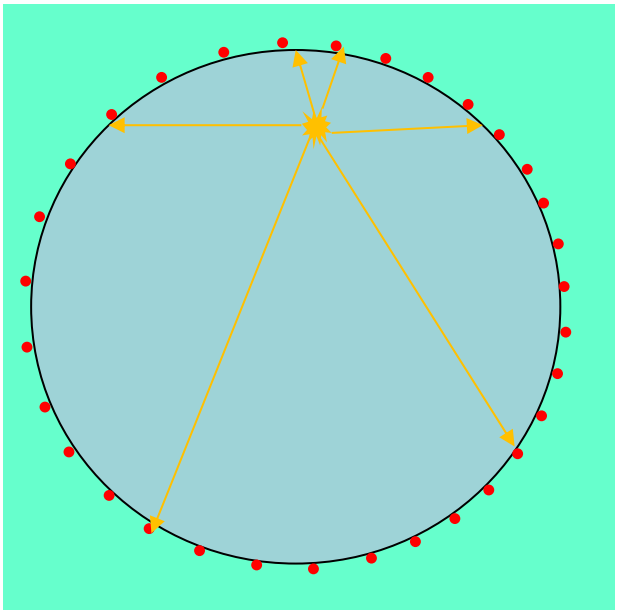

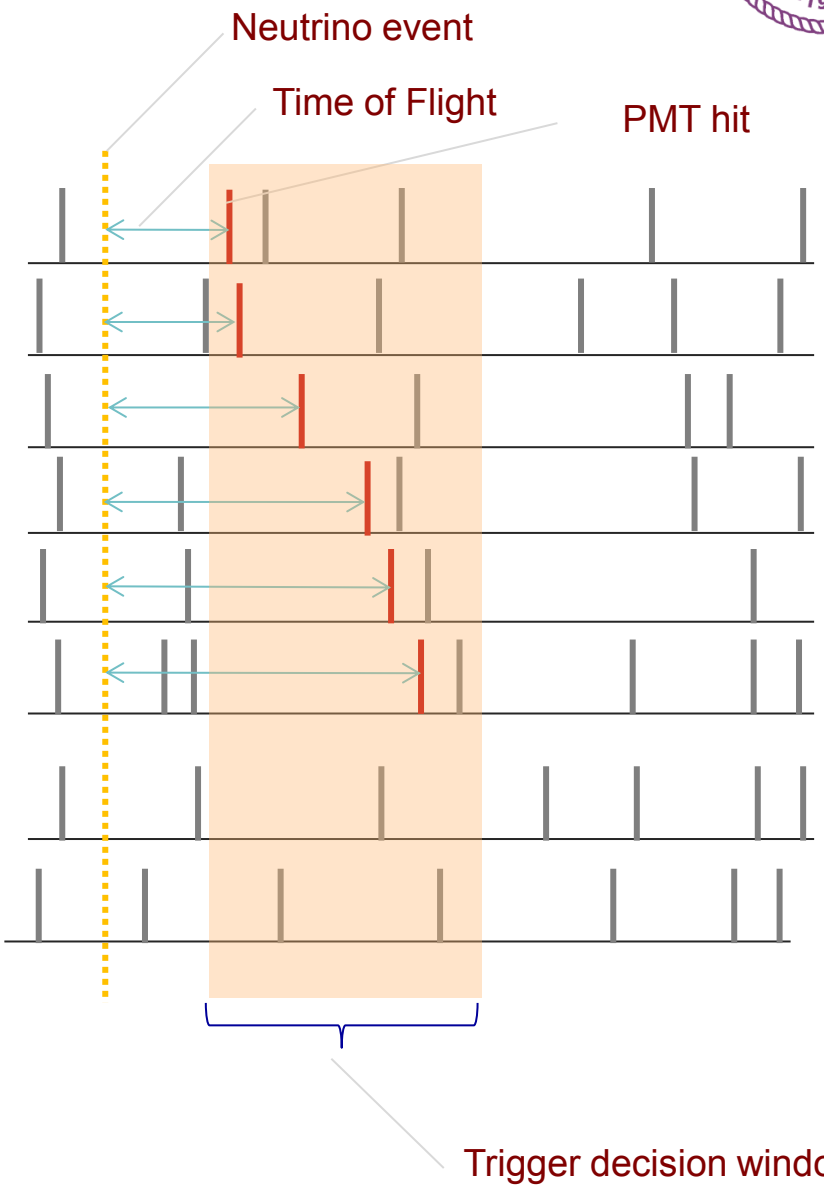

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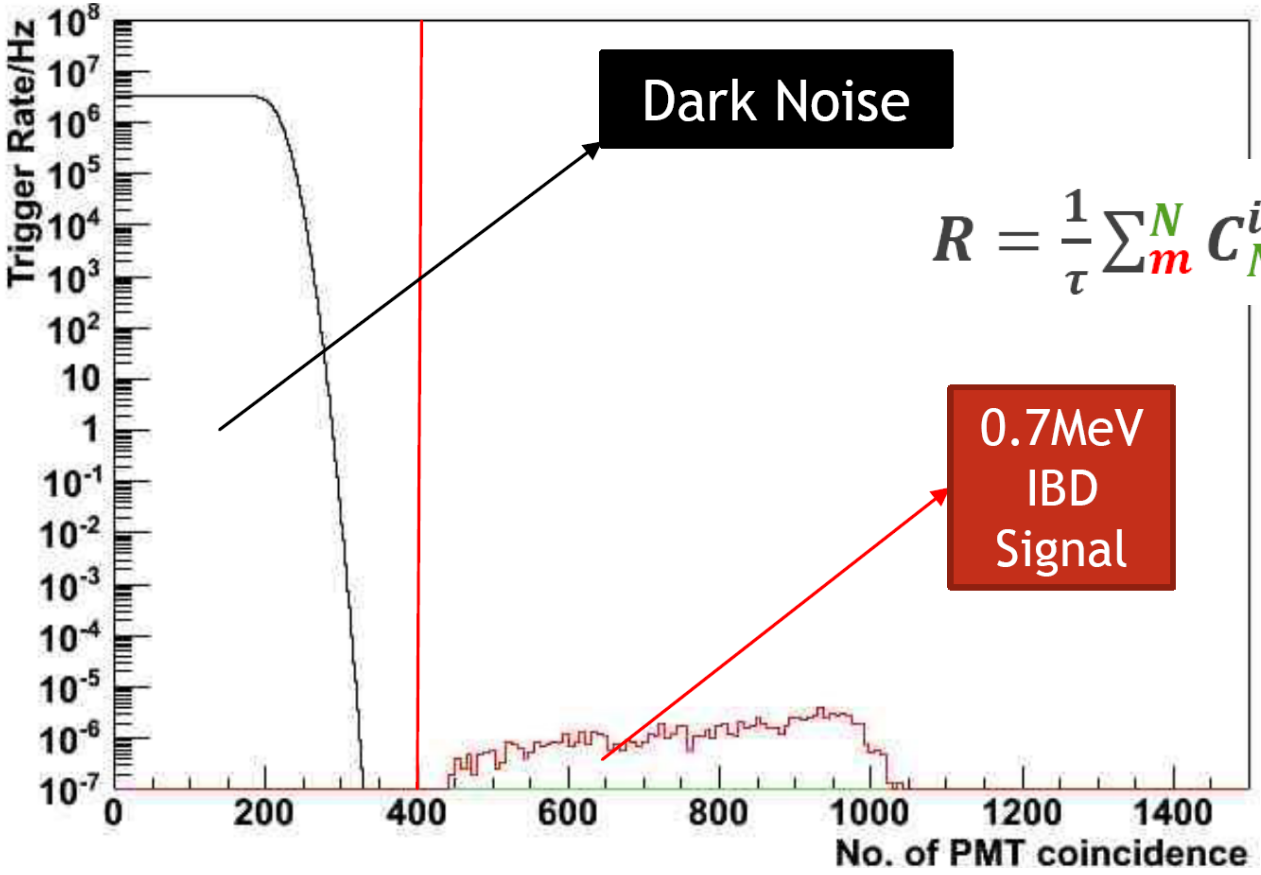
PMT Dark noise



$$R = \frac{1}{\tau}\sum_{m}^{N} C_N^i (f\tau)^i (1 - f\tau)^{N-i}$$

- Single PMT Dark Noise Rate: $f = 50kHz$
- Coincidence Window: $\tau = 300ns$
- Total PMT Number: $N = 14159$

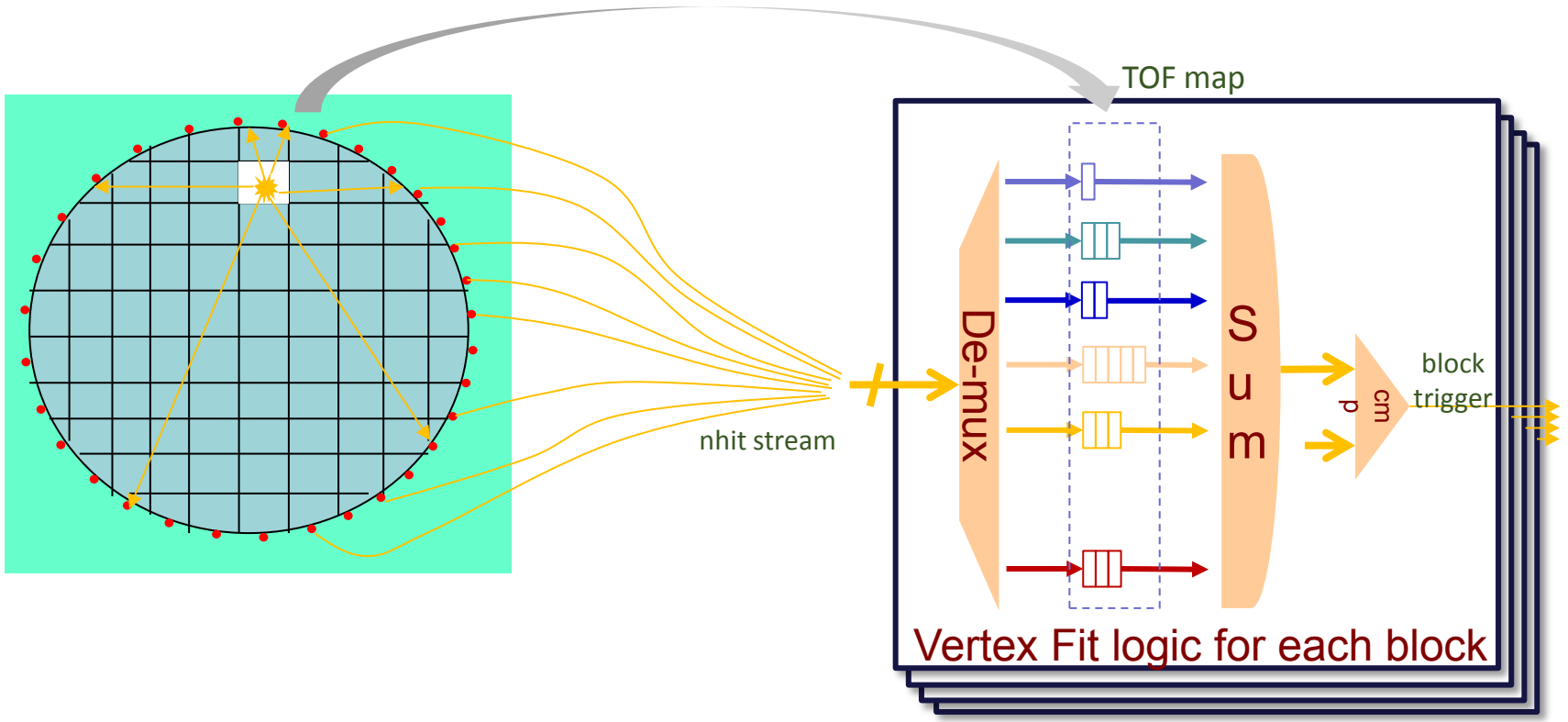
Vertex information

- Vertex information is useful
  - TOF difference can be corrected
    - reduce trigger window, Reduce dark noise coincidence -> lower E threshold
  - Flexible trigger scheme with vertex position
    - adapt the multiplicity threshold to the distance
    - Veto noisy detector volume with high radioactivity background

- Difficult to get real-time vertex information in trigger system
  - “Charge weighted mean center” is complicate to implement in FPGA
  - binary hit information is not sufficient, charge information is needed
    - Dedicated algorithm to extract charge info. From 1Gsps ADC sample stream to be developed
    - Transmit and process of charge information is more costly

Vertex fit method

- ✓ Assume the vertex at certain location
- ✓ Correct TOF for each PMT accordingly
- ✓ Small trigger window and high nHit threshold
- ✓ go through all possible locations



Feasibility

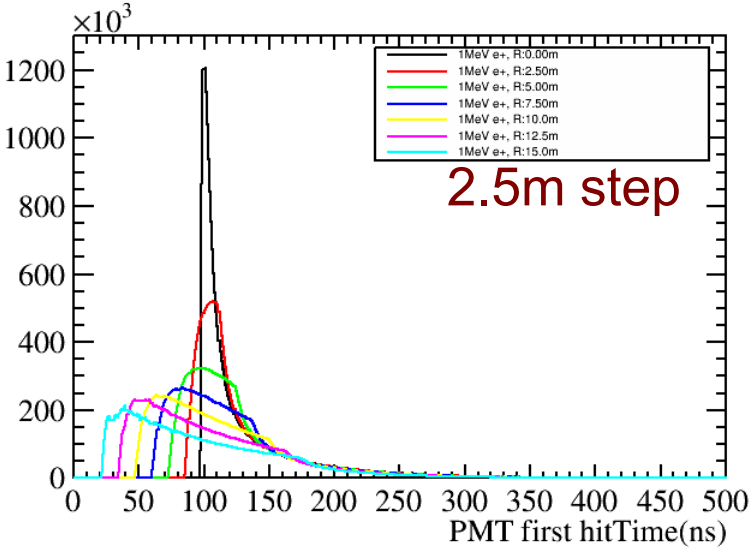
- precise Vertex position is not required
  - **few meters** resolution is good enough for trigger usage
  - 5m : 180 blocks for 20kt LS, 50ns trigger window
- precise timestamp not needed
  - nHit information is time-aligned stream data updated in o(25ns)
  - arrival time of nHit = event time + TOF + electronics-latency
  - Electronics latency is compensated after installation
  - TOF can be corrected assuming the vertex position
  - All operations can be done in 25ns interval
    - Simply handled with system clock
- Parallel processing for each possible location

Advantages

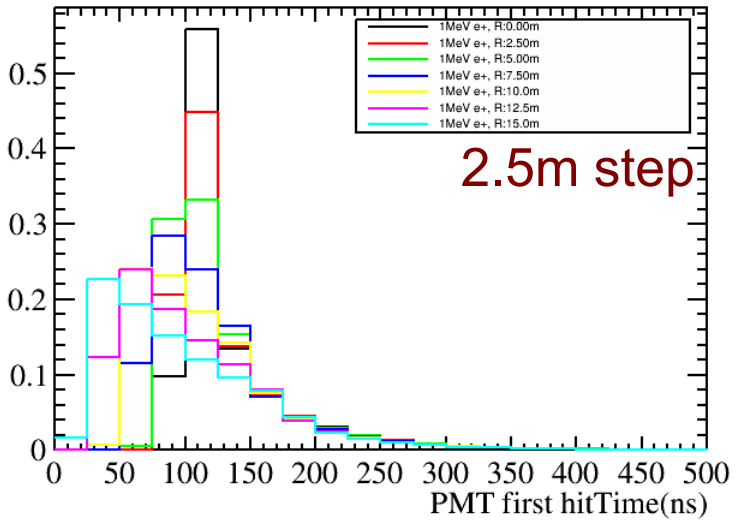
- Compatible with conventional nHit trigger schemes
  - Set TOF correction to zero, set trigger window to 300ns
  - Keep nHit logic working in parallel, to guarantee IBD collection
- extensible and flexible
  - More fit logic -> smaller block -> smaller trigger window -> less noise -> lower threshold
  - simple increase #VFL, not affect anything else
    - expandable even after data-taking
- simple
  - identical logic with TOF correct parameters for different block
  - VFL as simple “logic block”, no need to be a physical board.
  - Multiple VFL can be implemented in a single FPGA
  - Data share inside chip, save input port

PMT hit time distribution

hit time in ns

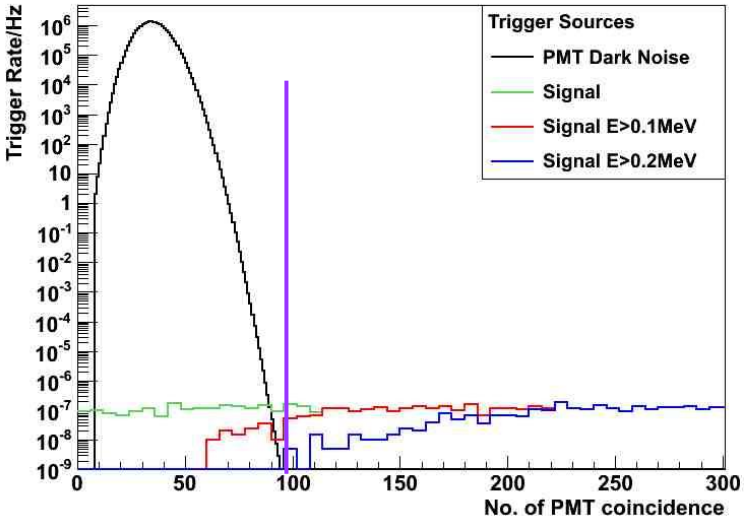


hit time in 25ns bin

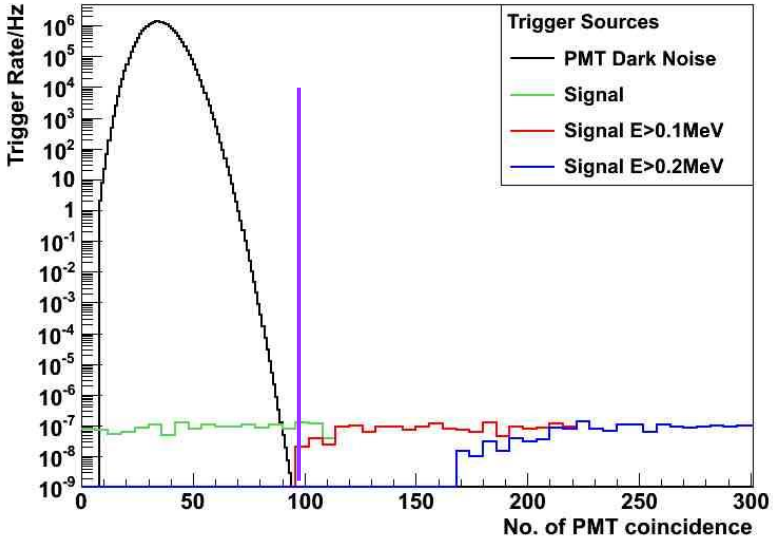


50ns trigger window

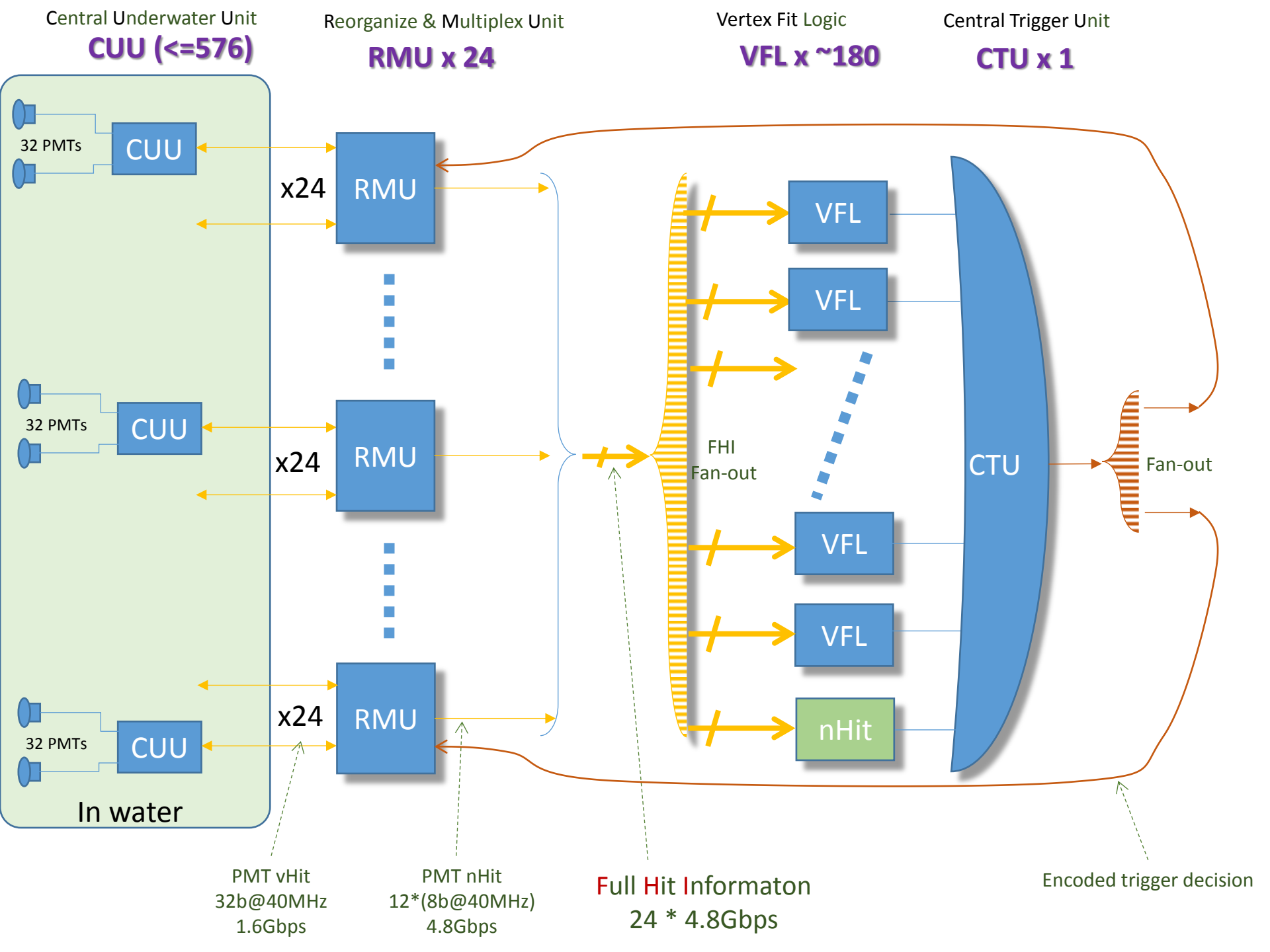
w/o fiducial volume cut



1m fiducial volume cut



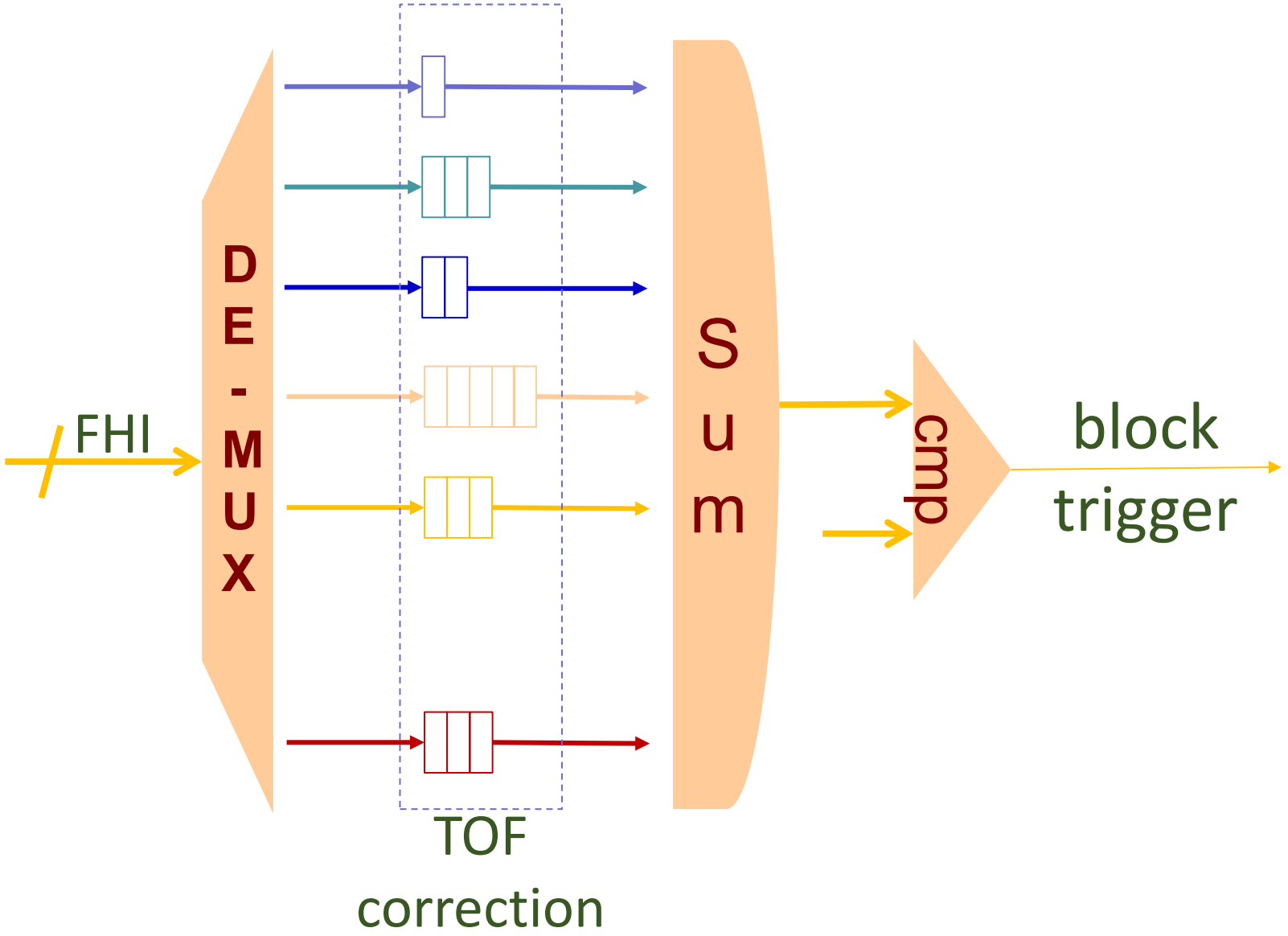
with “nHit(50ns) > 100”, <0.2Mev threshold is achievable


Central Underwater Unit
CUU (<=576)
Reorganize & Multiplex Unit
RMU x 24
Vertex Fit Logic
VFL x ~180
Central Trigger Unit
CTU x 1
32 PMTs
CUU
x24
RMU
VFL
FHI
Fan-out
CTU
Fan-out
nHit
In water
PMT vHit
32b@40MHz
1.6Gbps
PMT nHit
12*(8b@40MHz)
4.8Gbps
Full Hit Informaton
24 * 4.8Gbps
Encoded trigger decision

Hardware modules

- RMU
  - 24 * 1.6Gbps input, 4.8Gbps output
  - Simple processing
  - Central Trigger receive and fan-out to 24 CUU
- Vertex Fit Logic/Unit
  - 24 * 4.8Gbps input, 20Mbps block trigger output
  - Simple processing
- CTU
  - Multiple block trigger signals input
  - Simple processing
  - 20Mbps central trigger fan-out to 24 RMU
- FHI multi-sharing
  - To provide FHI (24 * 4.8Gbps) for all 180 VFL

Vertex Fit Logic



VFL Resource estimation

- 288group x 8bit input
- each group delayed for 12 taps
- configurable taps from each group are summed up
- Comparator

- Vertex5, LX220,
- Precision RTL Synthesis

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Device Utilization for 5VLX220FF1760

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Resource	Used	Avail	Utilization
IOS	11538	800	1442.25%
Global Buffers	0	32	0.00%
Function Gener	4891	138240	3.54%
CLB Slices	1223	34560	3.54%
Dffs or Latches	1	139840	0.00%
Block RAMs	0	192	0.00%
DSP48Es	0	128	0.00%

10 VFL in one FPGA is possible

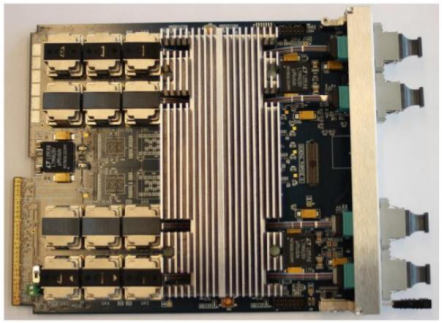
180VFL= 18FPGA = 18/9 cards = 1 crate

Vertex Fit Unit

- 24*4.8Gbps input
- Large logic resource (as much as possible)
- Existing modules from HEP community
  - Already over-qualified for our needs

Production ready modules in CMS

- **MP7**
  - XC7VX690T
  - 72 Rx @ 13Gb
  - 72 Tx @ 13Gb
  - Ports 4-8 populated
    - → 9-11 LVDS

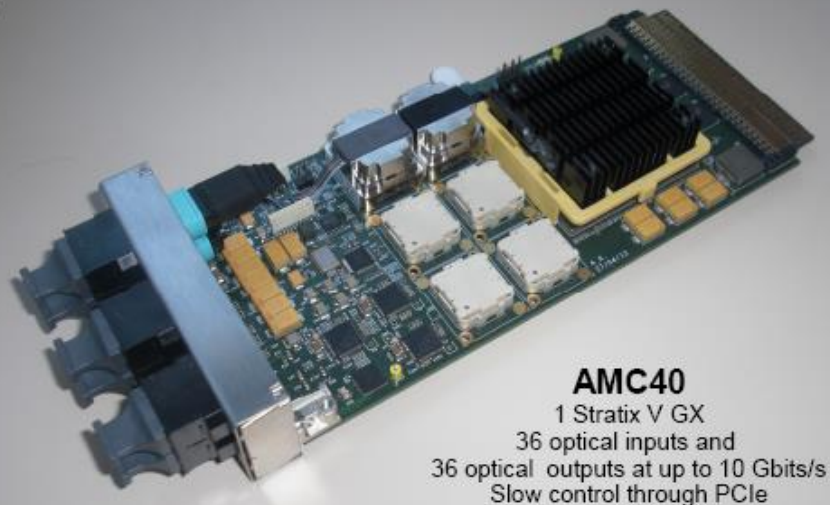


CMS MP7

CMS xTCA M. Hansen, CERN. magnus.hansen@cern.ch

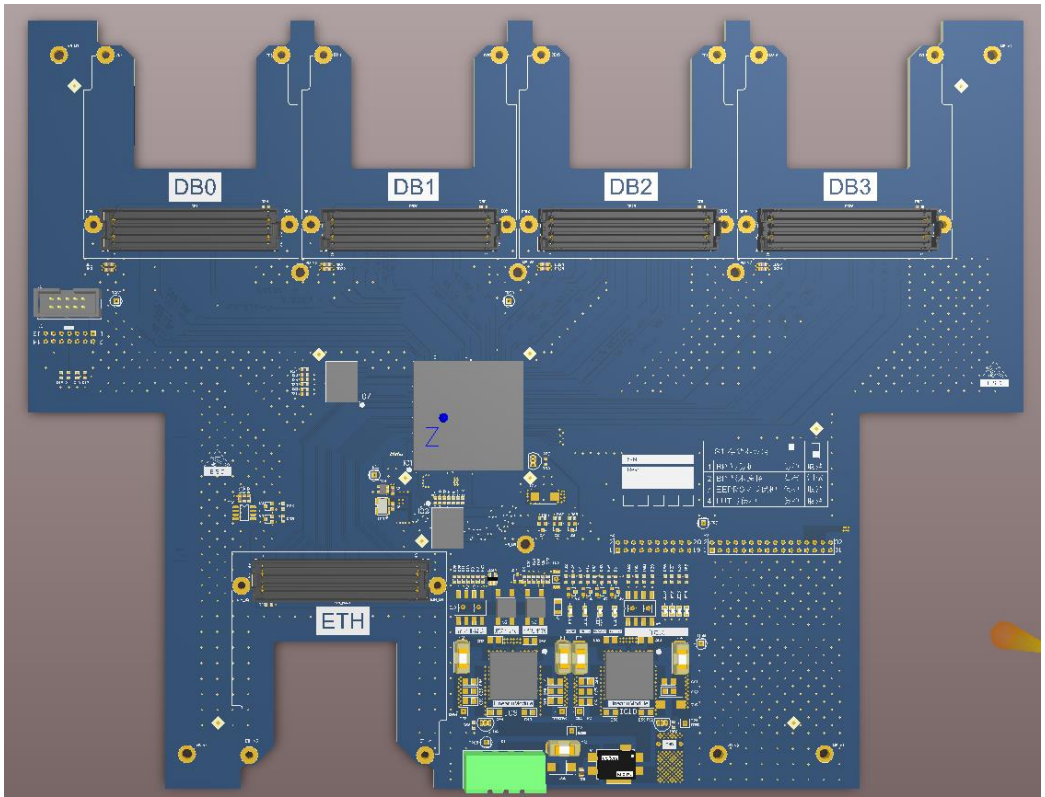
2014-03-17 E. Hazen -- xTCA WG 5 / 17

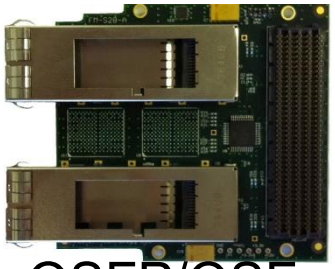
LHCb AMC40



Base evaluate board for RMU/VFL

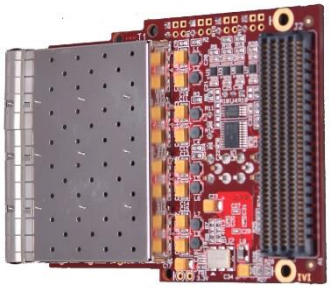
- XC7V585T
- 4 FMC to evaluate different optical Rx Mezz
  - SFP, SFP+,QSFP,QSFP+,SNAP12 Rx/Tx module
- Ethernet mezzanine for testing





QSFP/QSF

SFP+



SFP

FHI multi-sharing

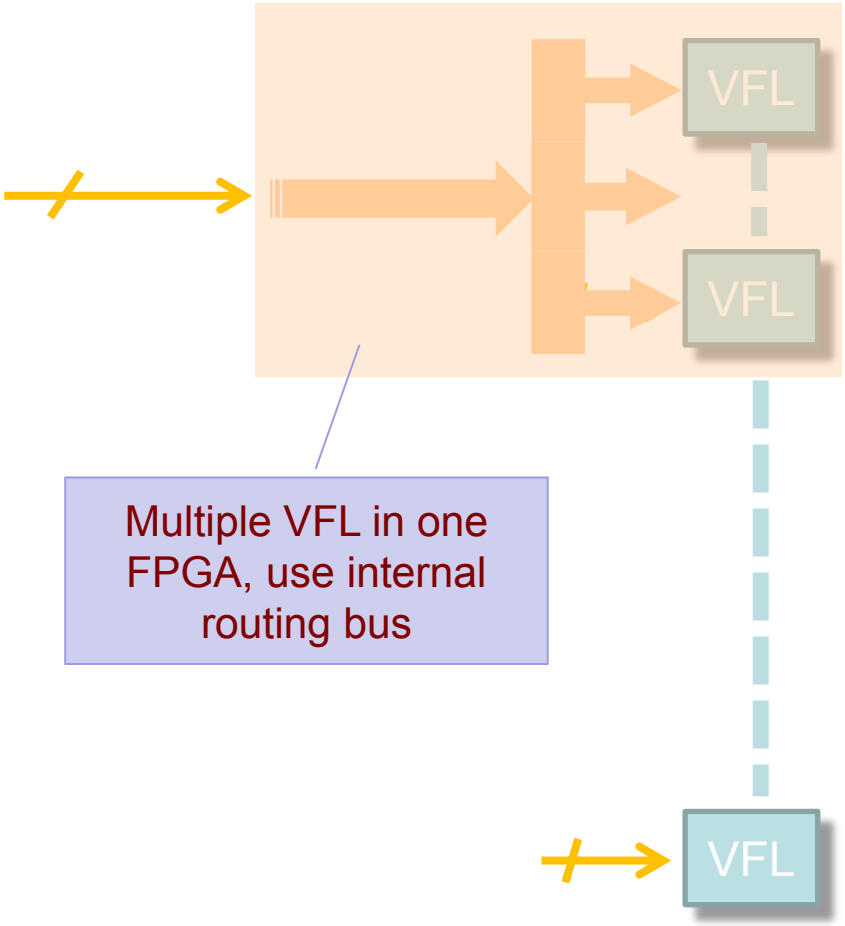
To provide FHI (24 * 4.8Gbps) for all 180 VFL

1 = 180

FHI multi-sharing

To provide FHI (24 * 4.8Gbps) for all 180 VFL

1 x10 = 180



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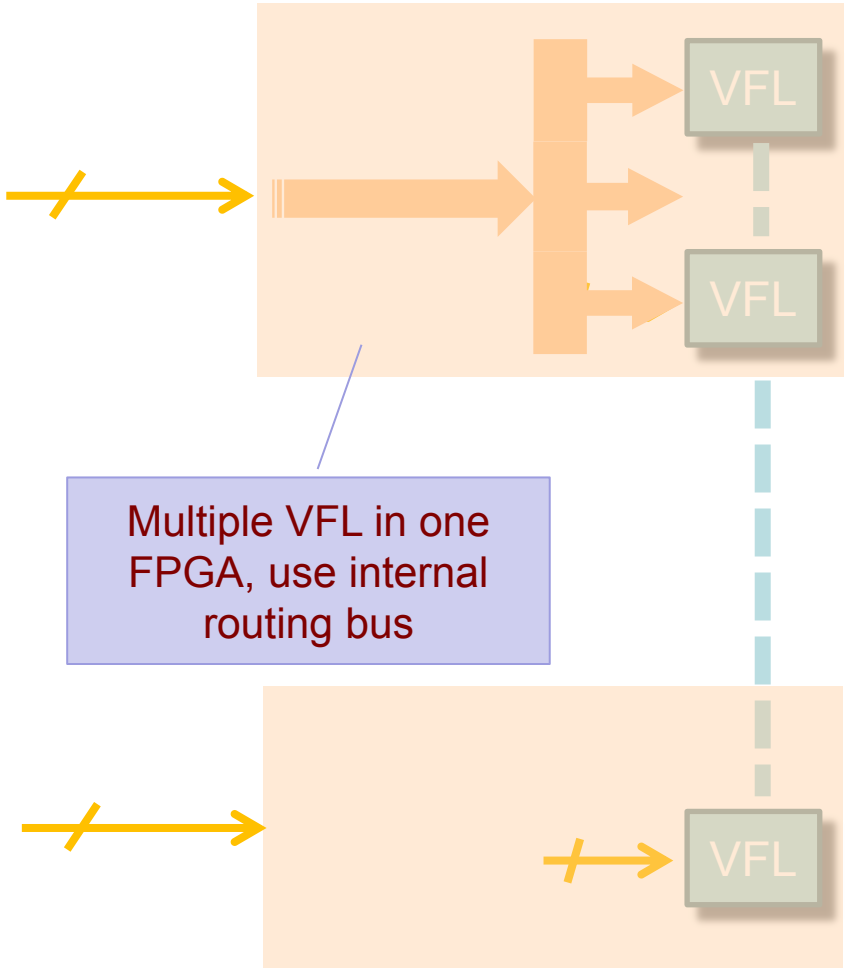
FHI

24 * 4.8Gbps



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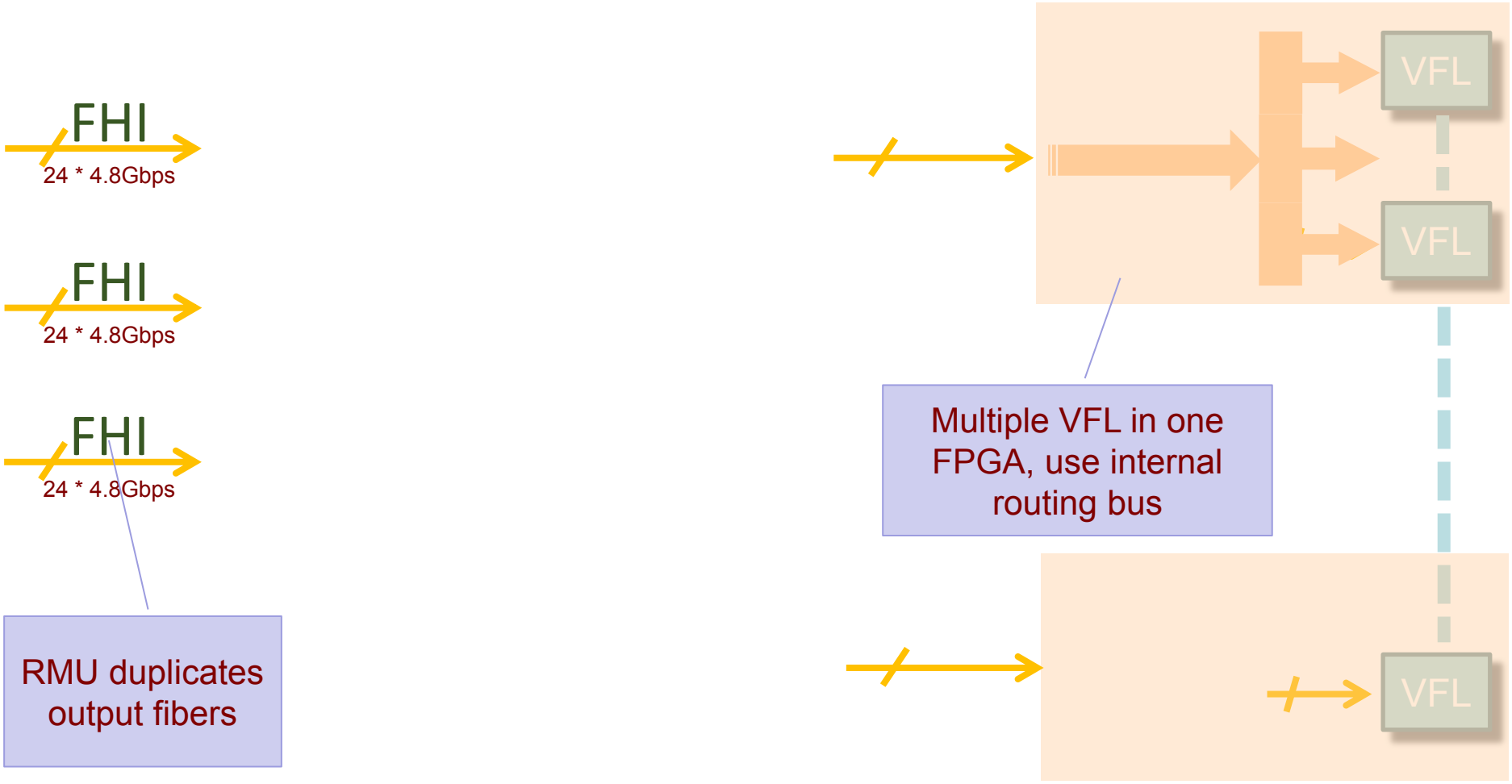
1 x3 x10 = 180



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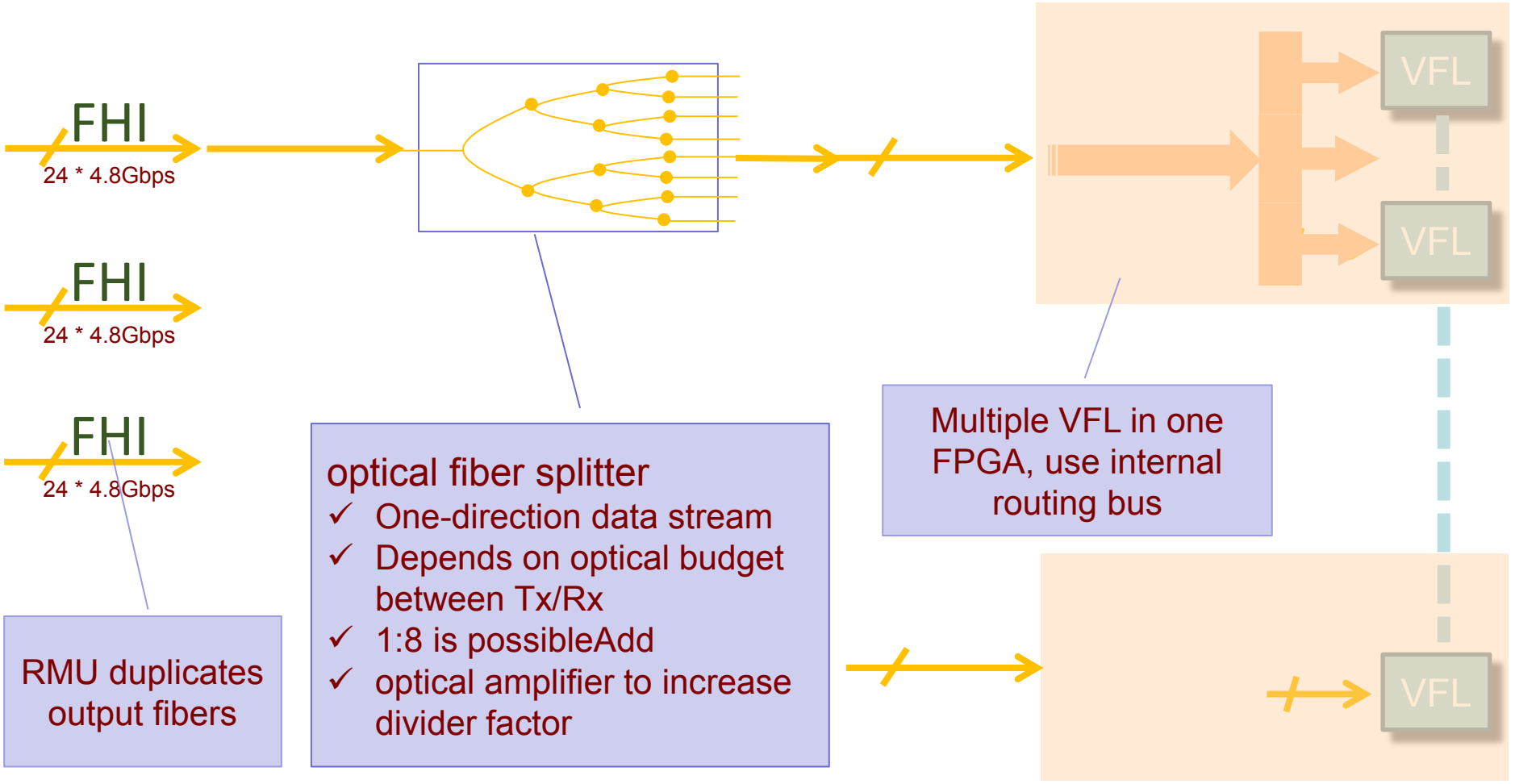
1 x3 x6 x10 = 180



Summary

- Enhanced global trigger system with vertex fitting is proposed
  - achieve lower threshold for low energy physics
  - dark rate is suppressed to reduce DAQ load
- technical possibility been explored, no technical challenges foreseen
- compatible with multiplicity trigger scheme
- flexible, expandable


Thank you!