Preliminary Design of a Real-Time Hardware Architecture for eRHIC

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BROOKHAVEN NATIONAL LABORATORY

a passion for discovery

U.S. DEPARTMENT OF ENERGY | Office of Science

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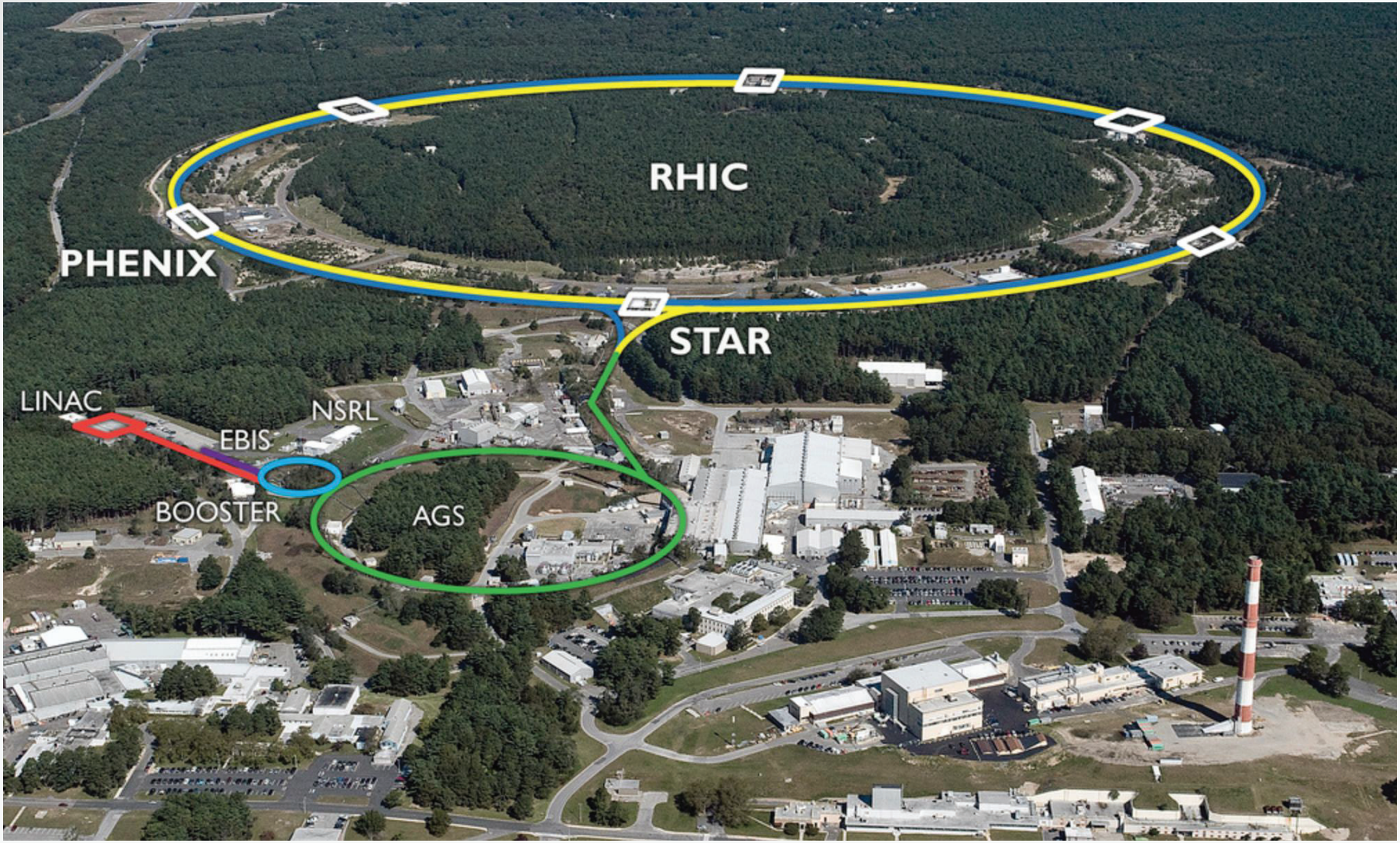
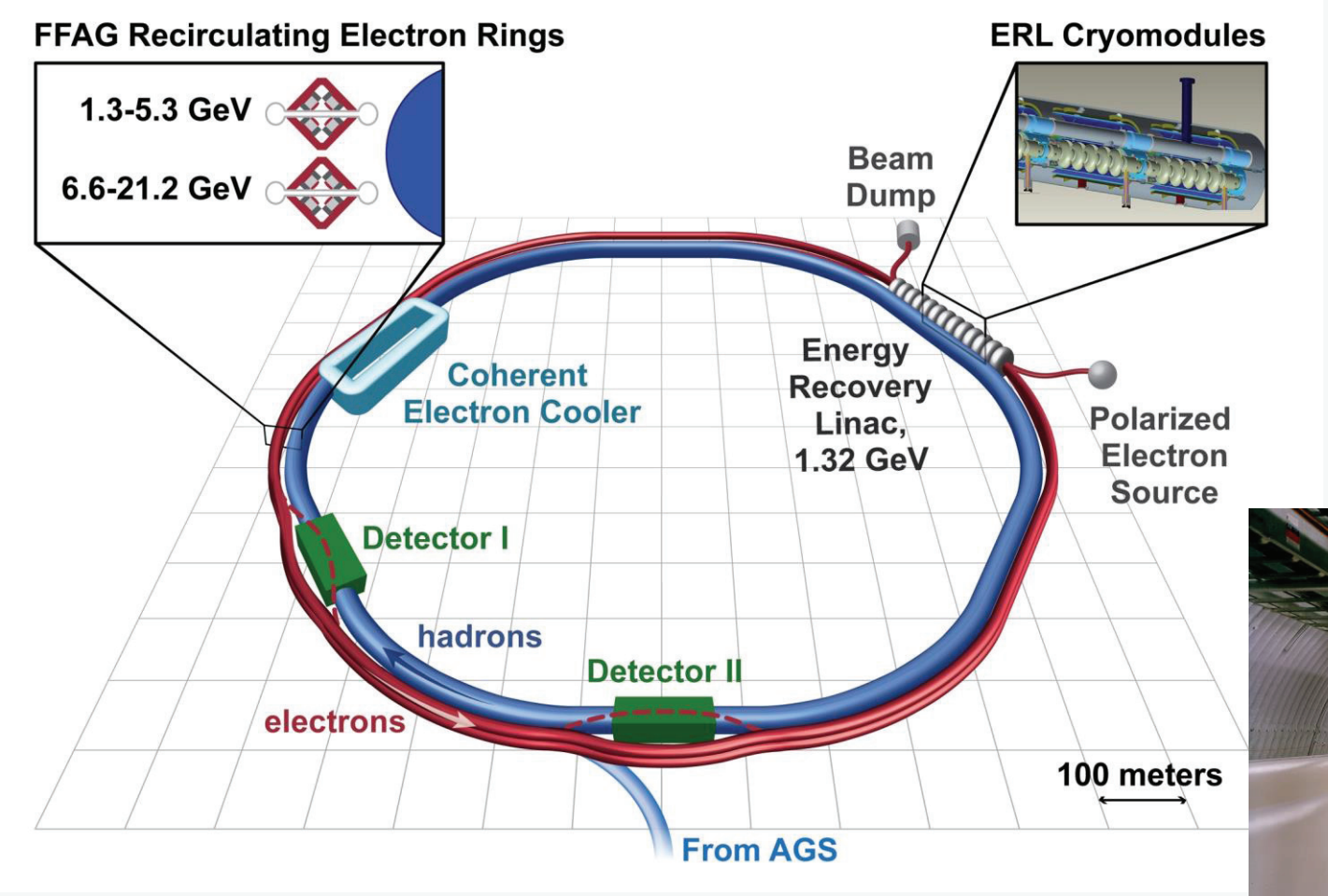
Outline

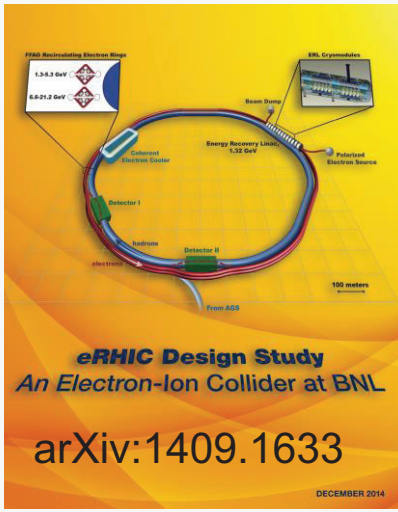
- Overview of eRHIC project
- History of Controls at BNL's Collider-Accelerator (C-A) facility
- Design requirements for eRHIC real-time hardware controls
- Latest developments
- Draft design of inter-module communication
- Backplane selection
- Can we collaborate?

Aerial View of BNL Collider-Accelerator Facility



eRHIC Proposed Design





eRHIC electron-Ion collider to be capable of colliding up to 21.2 GeV electrons with up to 100 GeV gold ions, 250 GeV polarized protons, and other species

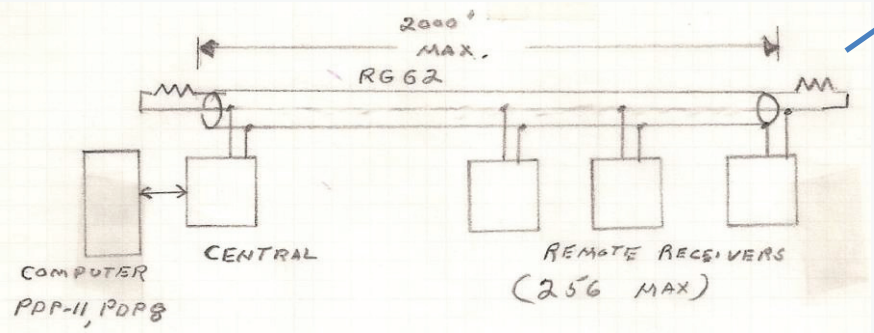
Existing RHIC Tunnel

History of Controls at the BNL C-A Complex 1960's to 1970's

AGS control room, circa 1966.

In the 1960s, everything was hard-wired to the control room.

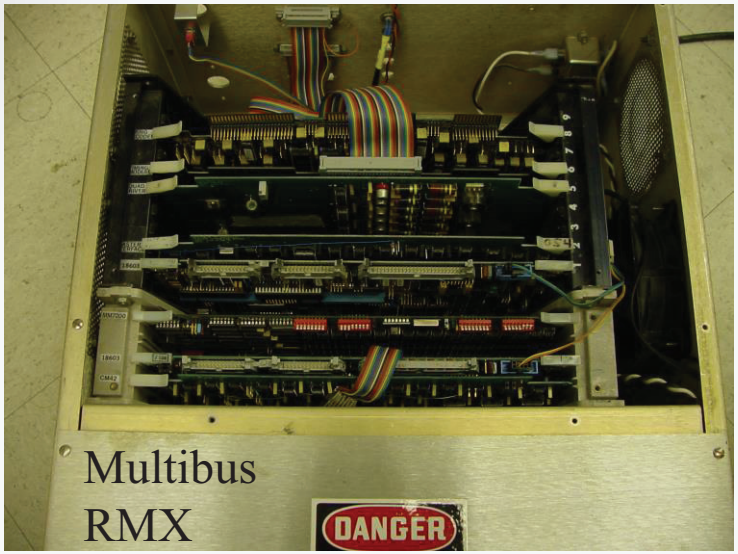
(photo from PDP. net)



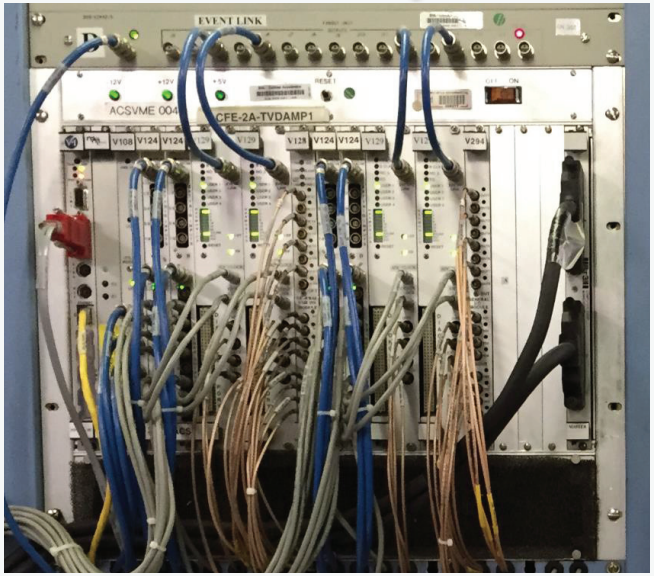
V.J. Kovarik, "Signal Specifications and Transceiver Operation for DATACON II System," BNL EP&S Division Tech. Note No. 58, March 14, 1973

- In the late 1960s and 1970s, the PDP-8/10 were installed, and accelerator control software was developed to automate operations.
- An in-house designed fieldbus called DataCon was created to interfaced the PDP to power supplies and other systems for remote control.

History of Controls at the BNL C-A Complex 1980's to 2000's



Multibus
RMX

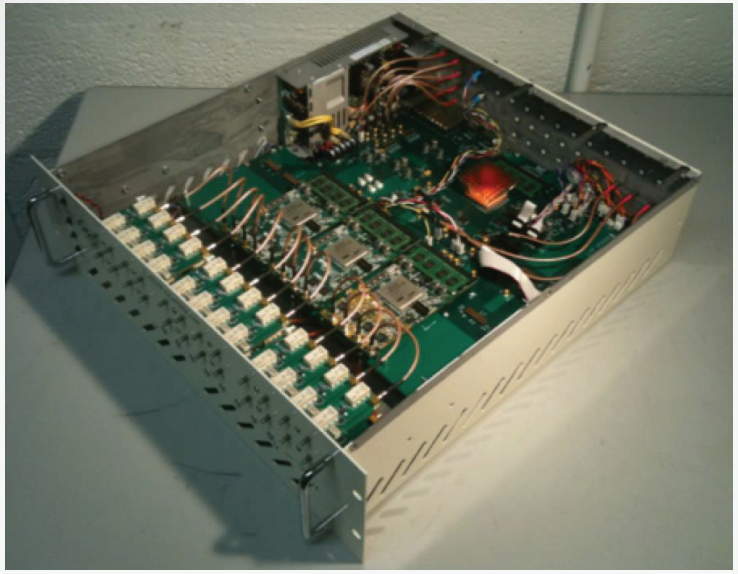


VME
vxWorks

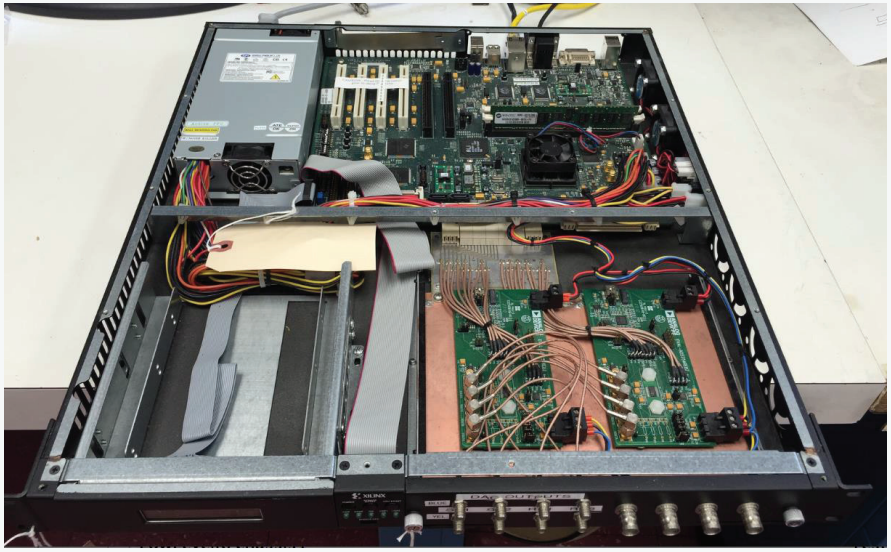
- In the 1980s, hardware with real-time operating systems were installed with communication to higher level servers.
- At AGS, Intel's Multibus (pictured above) running the RMX real-time operating system became a standard.
- But maintenance was difficult because nearly every unit was unique and required a dedicated spare chassis.

- In the 1990s, VME chassis installations became the new standard, with front-end computers running the real-time operating system vxWorks.
- This greatly simplified maintenance. A failed module became very easy to replace.

History of Controls at the BNL C-A Complex Since about 2010



RHIC Low-level RF platform



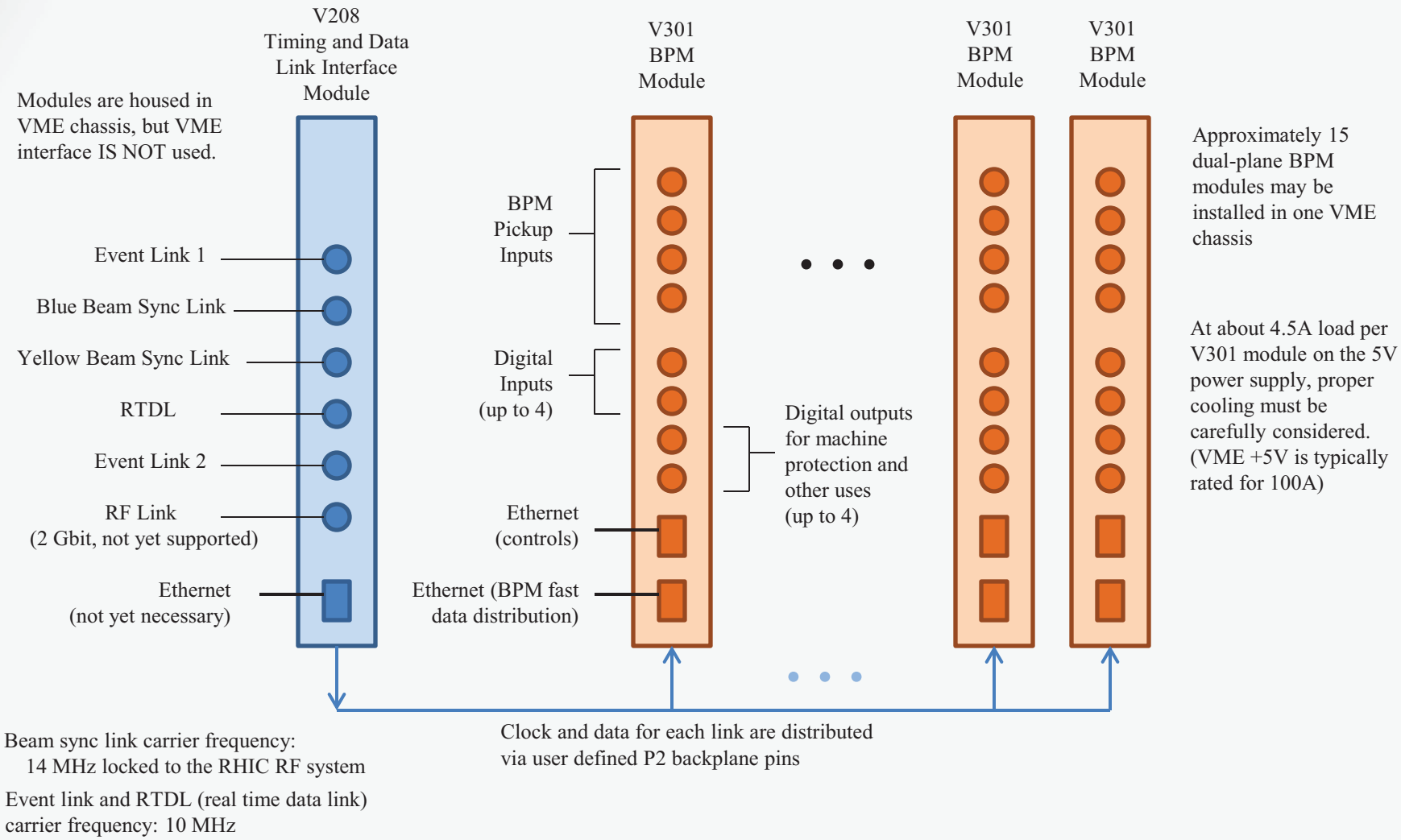
10 Hz Global orbit feedback controller

- More recently, fully integrated systems are being developed with embedded processors built into gate array components, and provide direct Ethernet connections.
- Systems shown above use the Xilinx Virtex 5 w/ embedded powerPC running vxWorks

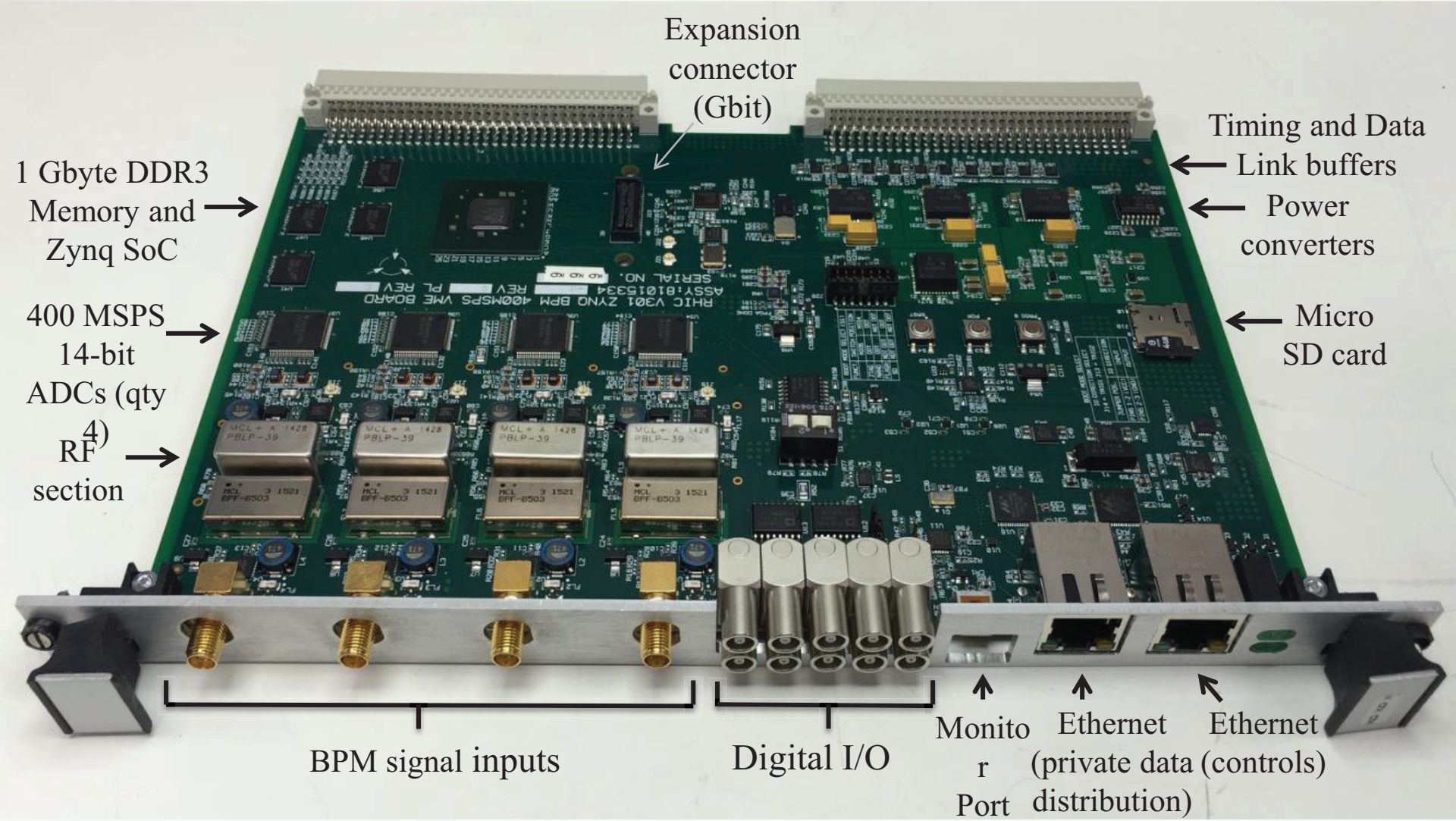
Design Requirements for eRHIC Real-Time Hardware Controls

- Minimization of equipment rack space
- Easy replacement of operational modules
- High reliability
- Simple software configuration of modules
- Simplified interface to machine timing and data links
- High speed processing of I/O signals
- Two or more Ethernet connections on each module
- Embedded operating system on each module with tightly coupled interface to real-time hardware, and with control system software objects resident locally
- Gigabit communication between modules
- Ability to use commercially available modules
- Ability to share custom hardware modules between other facilities

Latest Developments
Block Diagram of Next Generation BPM system as eRHIC Hardware Architecture Prototype

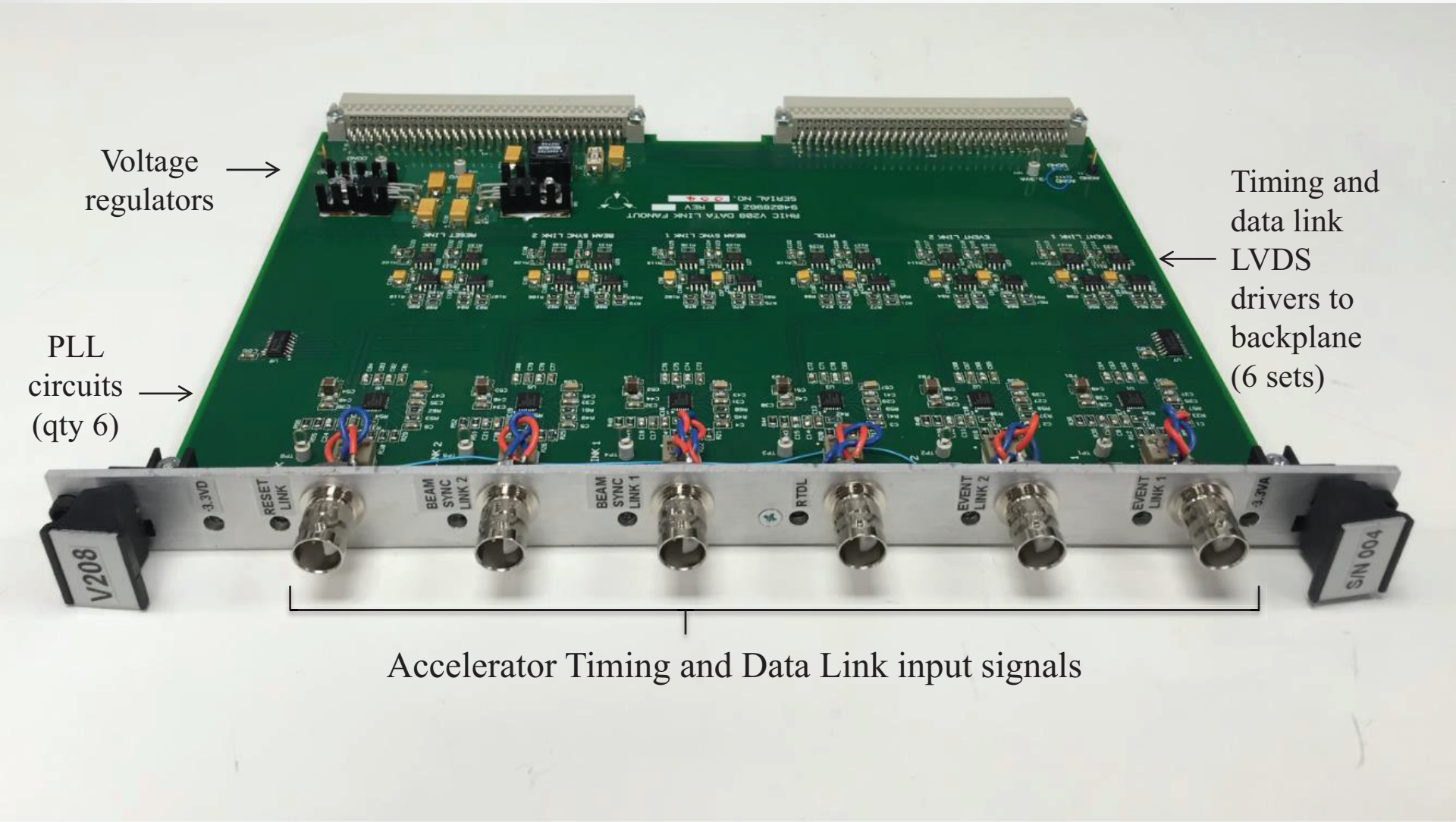


Latest Developments (basis for eRHIC) V301 BPM module

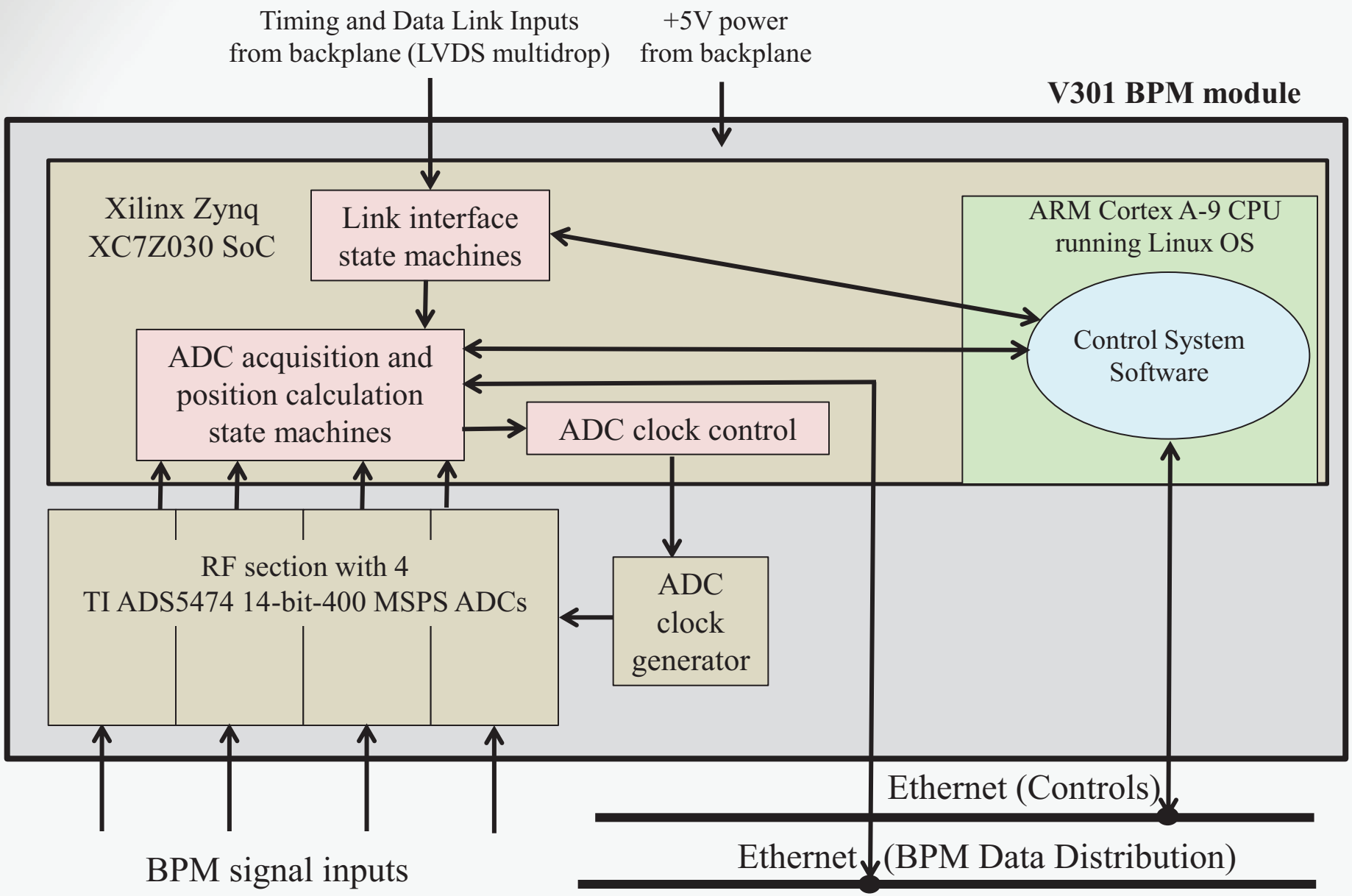


Xilinx Zynq SoC with on-board dual core ARM Cortex-A9 CPUs, one running Linux for execution of control system software objects (RHIC ADOs, which is similar to EPICS IOCs)

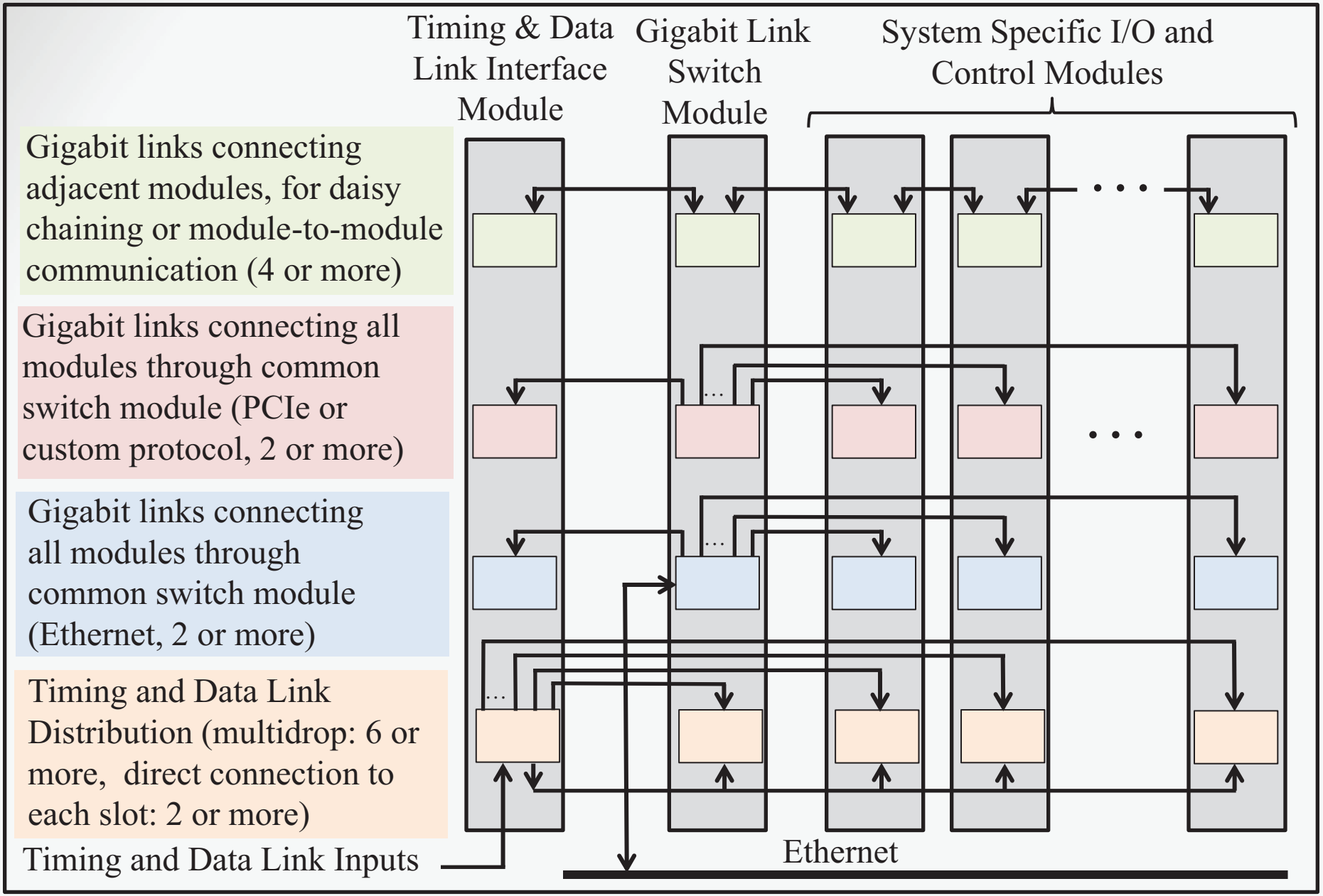
Latest Developments
V208 Timing and Data Link Interface



V301 BPM Module Block Diagram



Draft Design of Inter-Module Communication

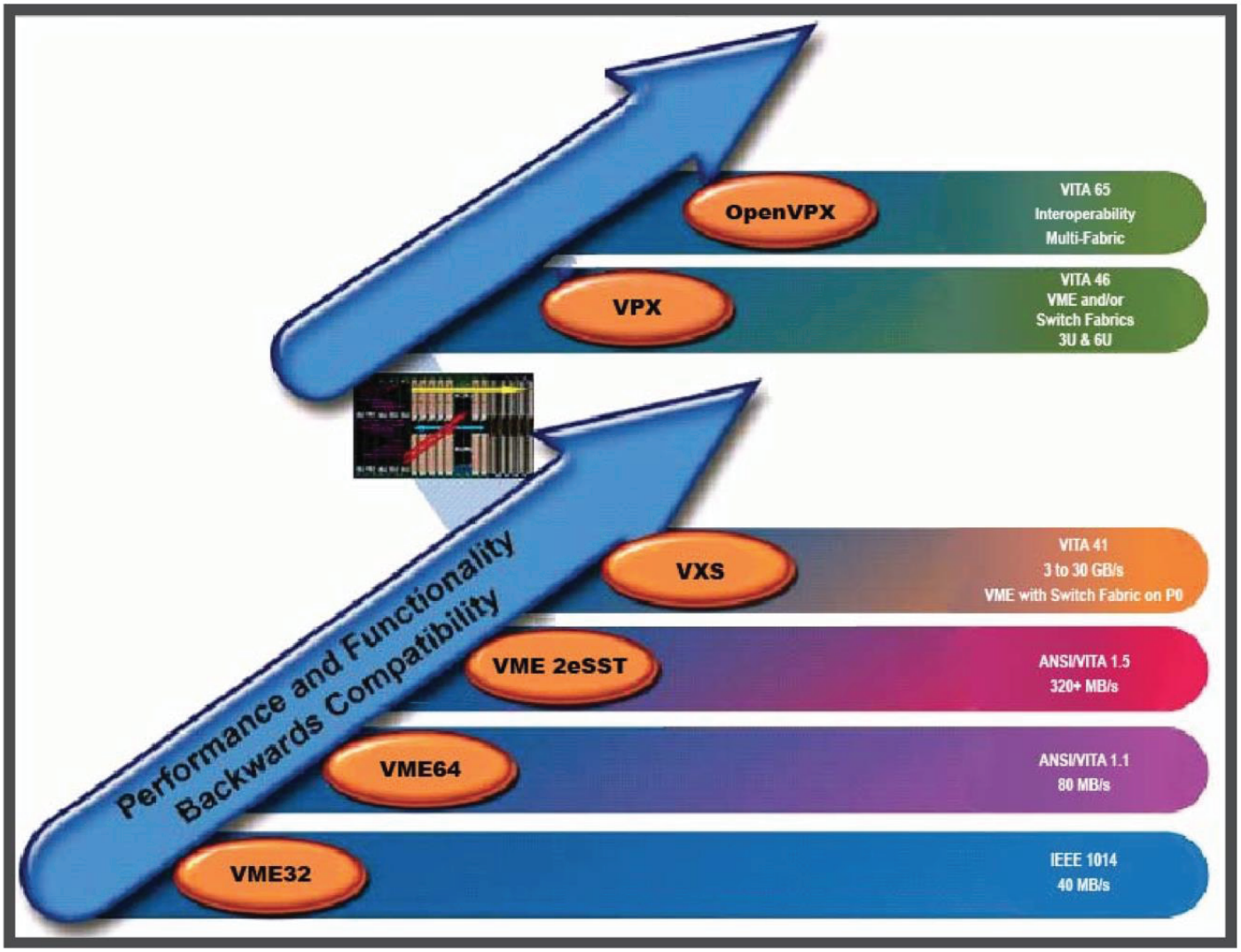


Selecting The Perfect Back Plane

- It hasn't been found yet. Reviewing:
  - VME
  - VXS
  - VPX, openVPX
  - TCA (microTCA, advancedTCA)

- VPX is attractive, but…
  - seems to be missing bussed signals as required to multidrop the machine clock and data link signals

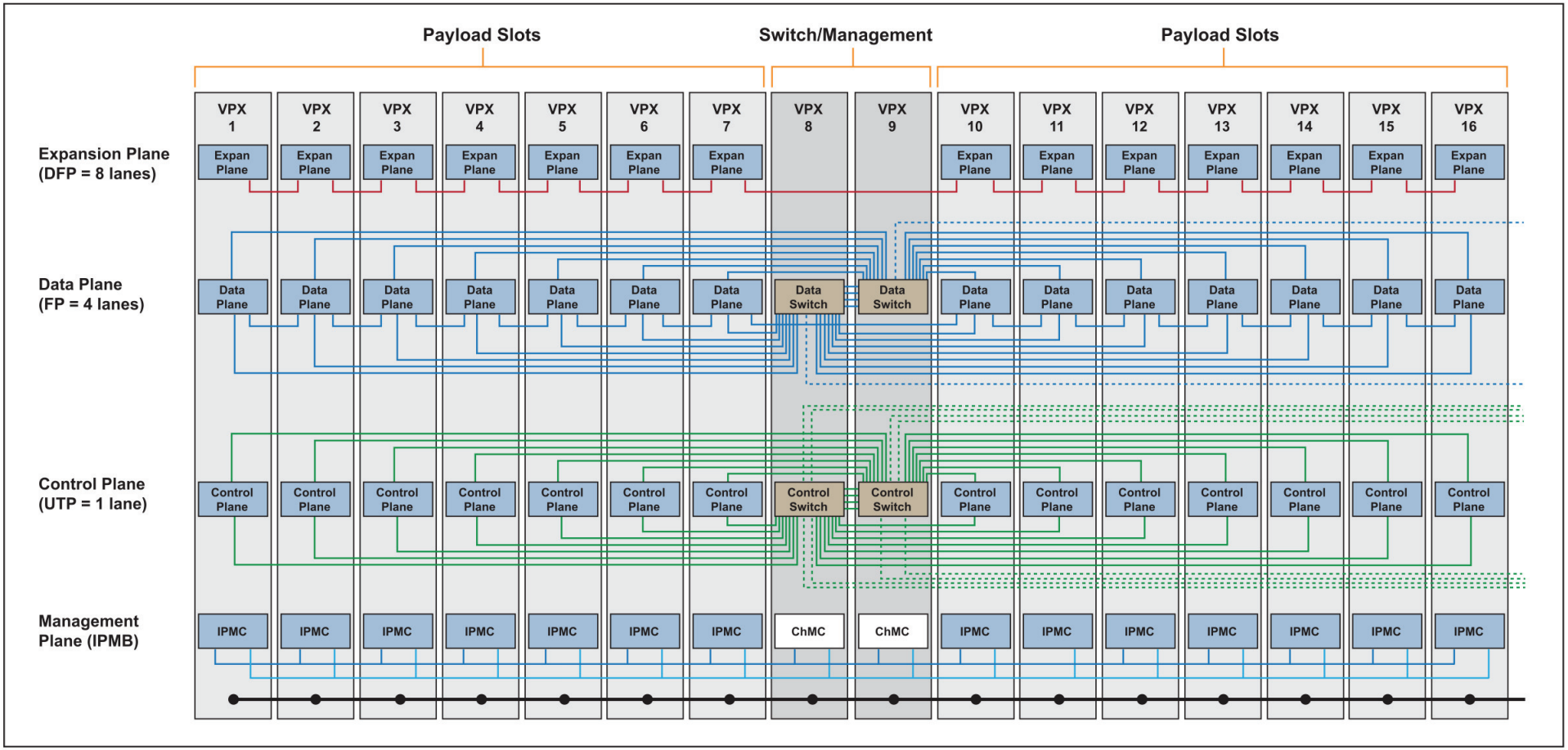
Evolution of Backplanes
VME to openVPX



openVPX	Interoperability Multi-Fabric
VPX	VME and/or Switch Fabric
VXS	VME64 w/ Switch Fabric
VME2eSST	320+ MB/s
VME64	80 MB/s
VME32	40 MB/s

From Elma bustronix white paper: "OpenVPX Backplane Profiles: Making Sense of System Interoperability For VPX"

One version of openVPX backplane



(www.vita.com)

A Pitch for Collaboration

- BNL's Collider-Accelerator department can not be the only facility that would benefit from this architecture.
- So let's collaborate –
  - First, a chassis system needs to be selected that satisfies the needs of the larger accelerator hardware (and software) community
  - Then, hardware and software needs to be developed and shared

Summary

- A general architecture for eRHIC real-time hardware has been designed
- A prototype has been developed and successfully tested using VME chassis (but no VME interface)
- Specific chassis architecture has not yet been selected.
- Collaboration with other institutions will be beneficial to all.

Acknowledgements

Team members

For their developments, support and expertise in this endeavor

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Low-Level RF personnel

For their advancements in embedded systems at the BNL C-A facility

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