STATUS DEVELOPMENT OF SIRIUS TIMING SYSTEM

WEPGF128

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Abstract

Sirius is a new low-emittance 3 GeV synchrotron light source under construction in Brazil. Its timing system, developed by SINAP through a collaboration with LNLS, will be composed of Ethernet-configured standalone event generators and event receivers modules controlled by remote EPICS soft IOCs. This work presents the system structure, the status of the development and some options for integrating it to the Sirius BPM MicroTCA platform.

System Design

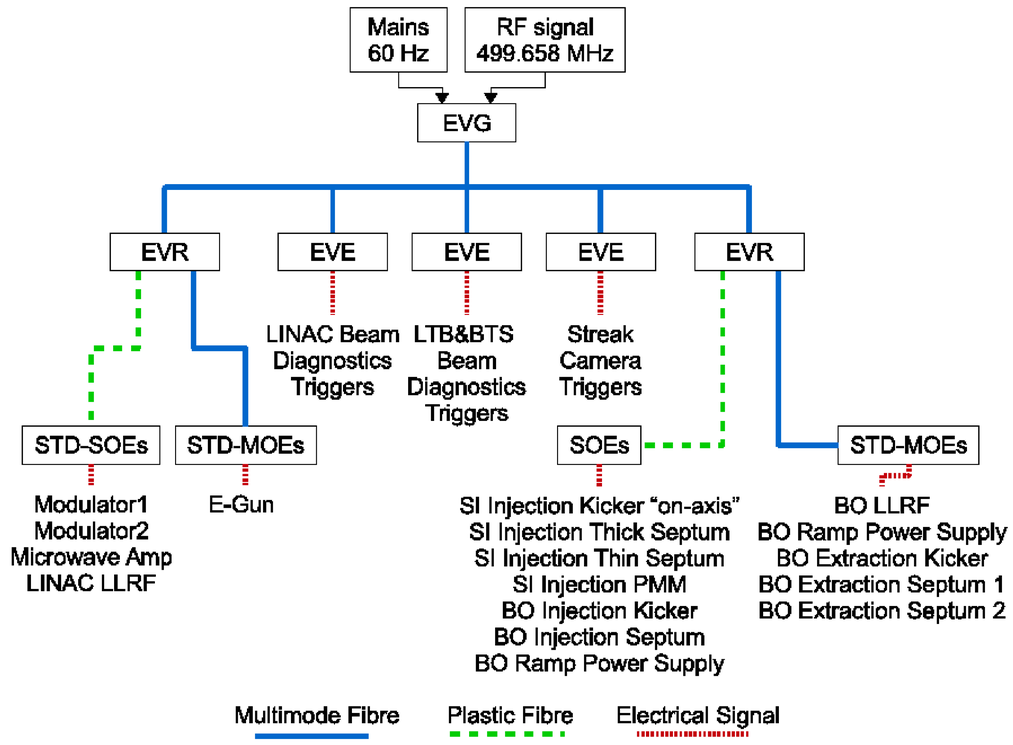

Figure1: Diagram of Sirius timing system concerning injection process. An event generator (EVG) broadcasts event frames to event receivers (EVR and EVE) through a star topology optical fibre network.

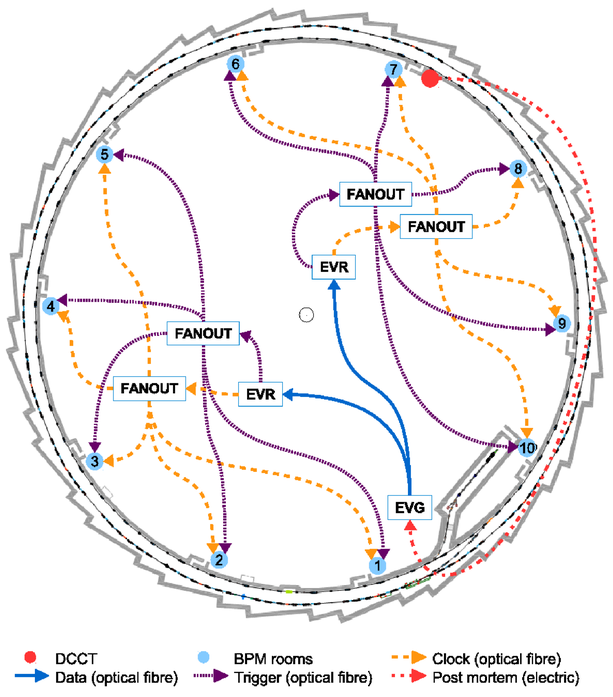

Figure 2: Simplified diagram of Sirius timing system concerning triggers and reference clocks distribution.

Table 1: Main Sirius parameters and timing specifications.

Parameter	Value
RF freq. (Storage Ring & Booster)	499.658 MHz
Storage ring circumference	518.4 m
Storage ring harmonic number	864
Storage ring revolution freq.	0.578 MHz
Booster circumference	496.8 m
Booster harmonic number	828
Booster revolution freq.	0.603 MHz
Coincidence number	19872
Coincidence frequency	25.144 kHz
Linac RF frequency	2.997 GHz
Repetition rate	2 Hz
Specification	**Value**
E-gun rms jitter	< 50 ps
E-gun trigger coarse delay step	2 ns
E-gun trigger fine delay step	20 ps
General trigger delay step	8 ns
Electrical outputs	TTL level
Event clock freq. ($\frac{RF\ freq.}{4}$)	124.915 MHz

Table 2: Timing system modules.

Module	Quantity
EVG	1
EVR	5
EVE	3
STD-MOE	5
STD-SOE	3
SOE	12
MicroTCA timing board	20

Table 3: Optical fibres and cables

Fibre & Cable	Quantity
Level-1 glass fibre (250 m)	8
Level-2 glass fibre (150 m)	13
Level-3 glass fibre (150 m)	20
Polymer fibre (50 m)	20
Electrical cable (20 cm)	35

Hardware

Figure 3: Optical to electrical converters developed by SINAP. Up to down are SOE, STD-MOE and STD-SOE.

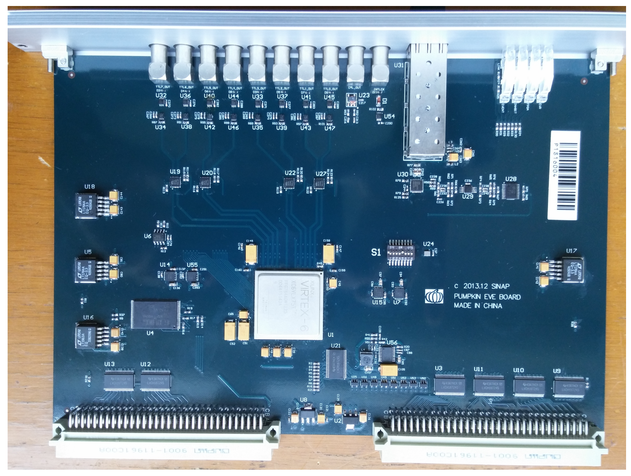

Figure 4: Inside an event receiver EVE, by SINAP.

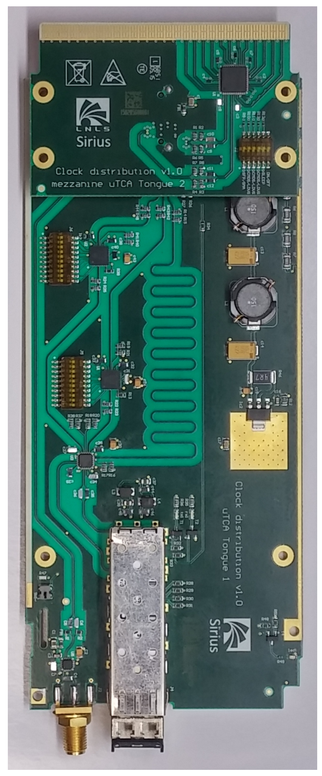

Figure 5: Conceptual prototype of a MicroTCA clock distribuition board developed by LNLS.

Test Results

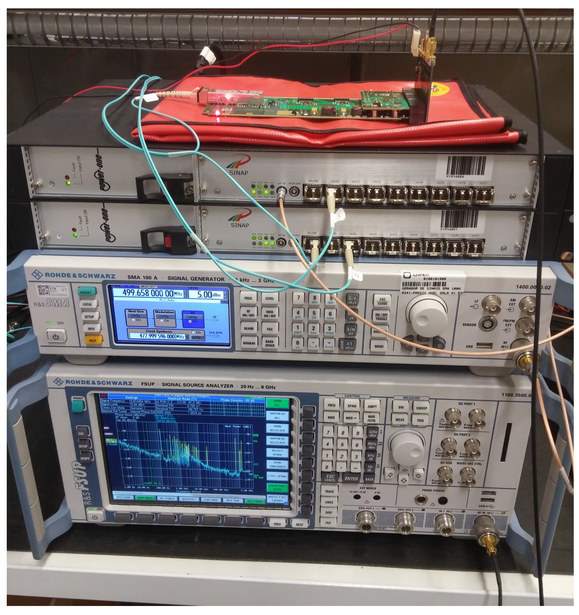

Figure 6: Test setup of MicroTCA timing board. Up to down: MCH board, EVG, EVR, signal generator and signal analyzer.

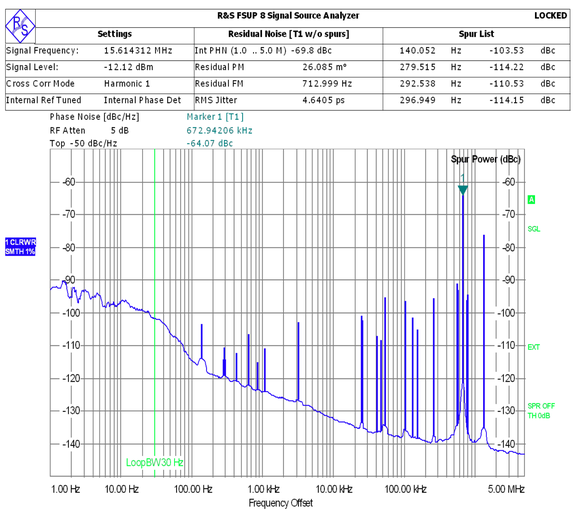

Figure 7: Phase noise analysis of MicroTCA clock distribution board.

- Structure completely defined
- Specifications achieved
- Flexible to future developments
- MicroTCA timing boards on the next year.

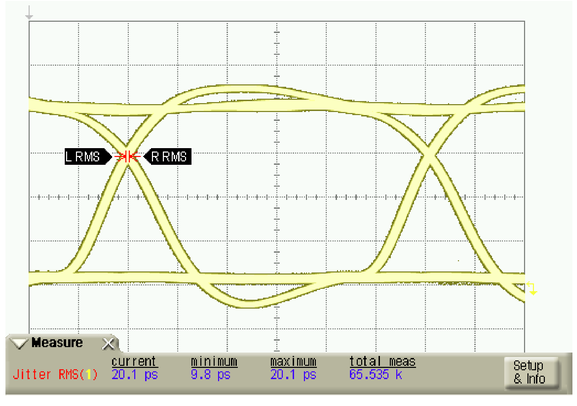

Figure 8: EVE long-term (24 hours) jitter test result.