

ENCODER INTERFACE FOR NSLS-II BEAMLINE MOTION SCANNING APPLICATIONS

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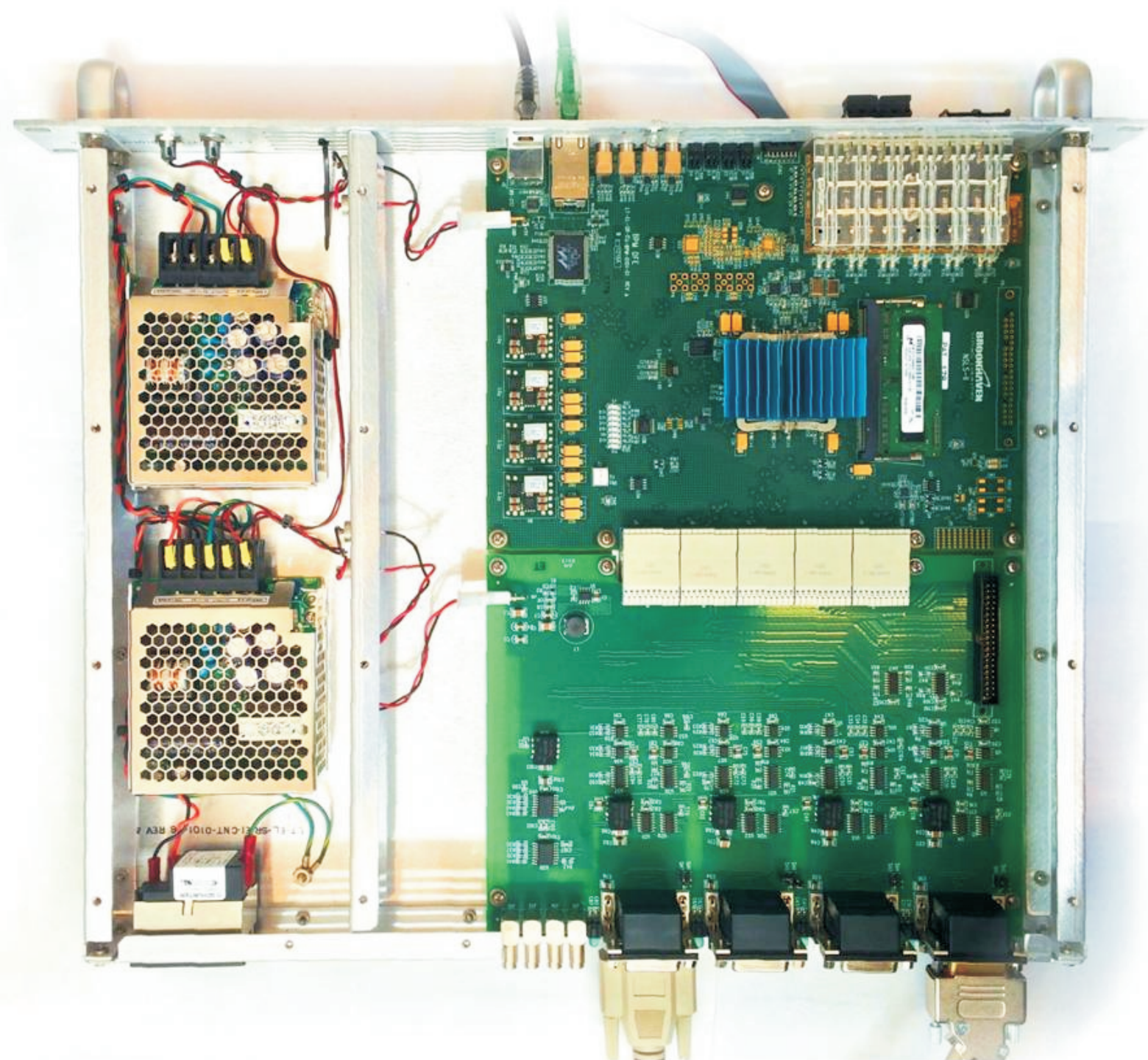
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Requirements

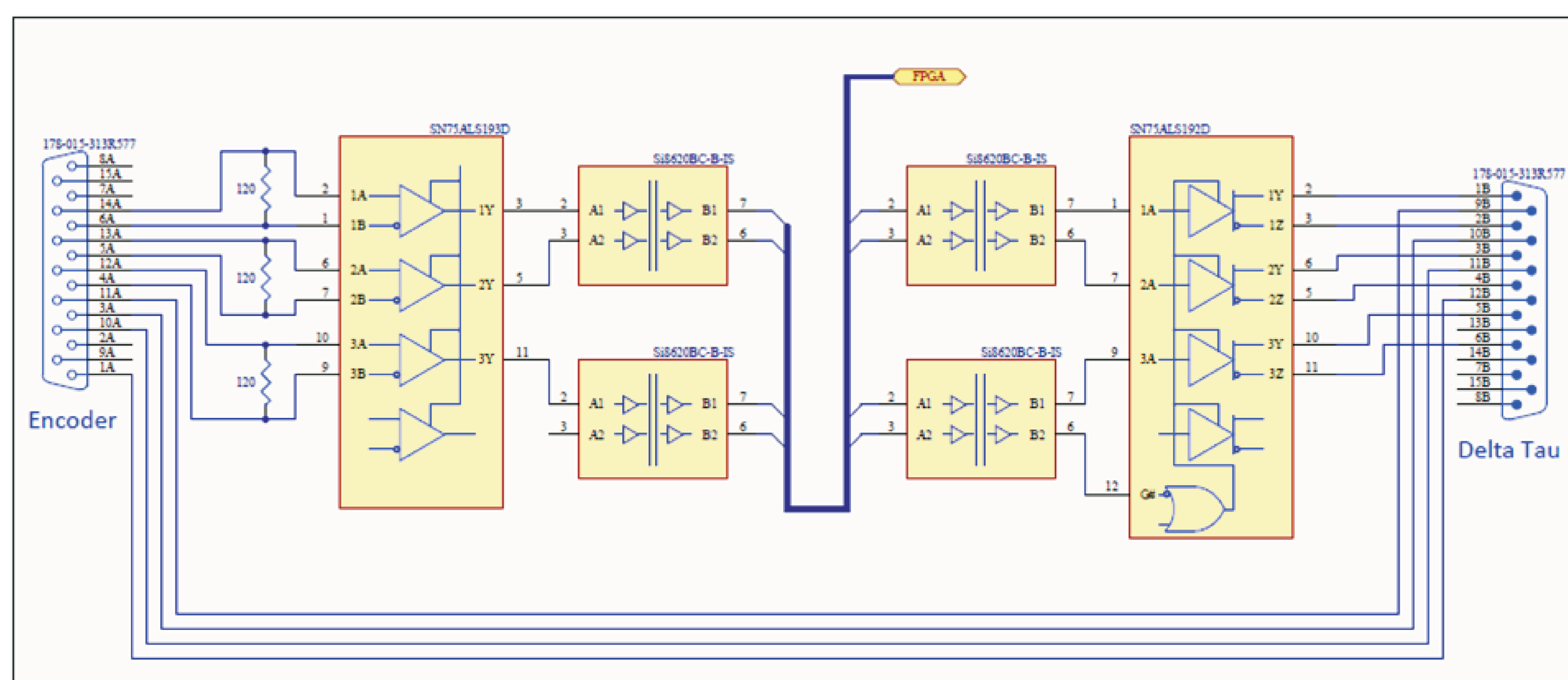
- Handling a Renishaw quadrature incremental encoder with 10 MHz operating frequency,
- Retransmit encoder interface signals for a motion controller allowing bypass connection,
- Relative encoder position is timestamped and saved to be restored at 10 kHz rate,
- Standard EPICS driver,
- Start capturing on external trigger or on EPICS PV write,
- Compatibility with existing timing system,
- Flexibility to custom experiment needs, generating triggers.

Instrumentation Base

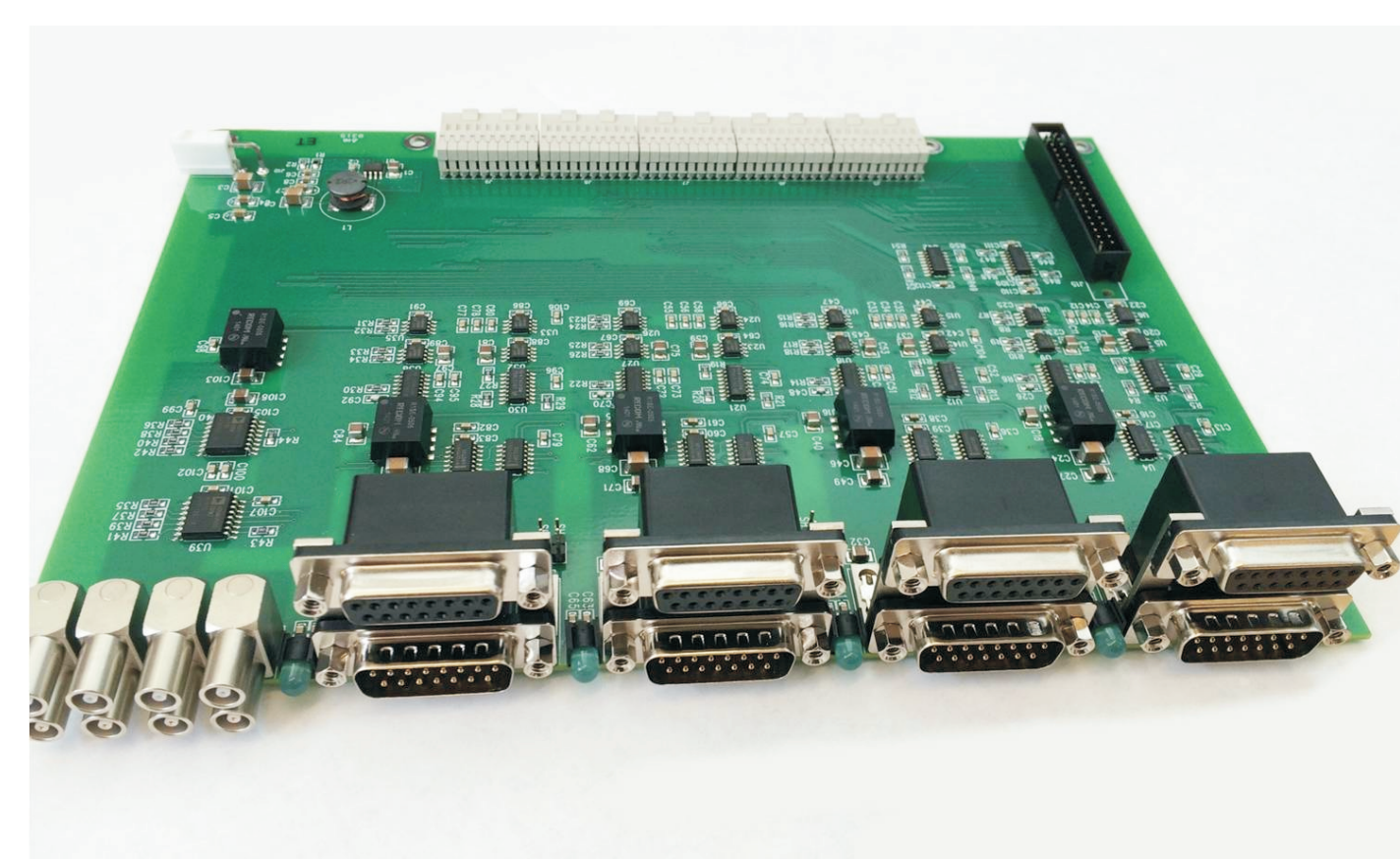
- 2U 19" chassis,
- Four channels,
- Main board with Xilinx Virtex-6 FPGA,
- Interface board for signal conditioning,
- Shares same platform with other NSLS-II designs.



Hardware



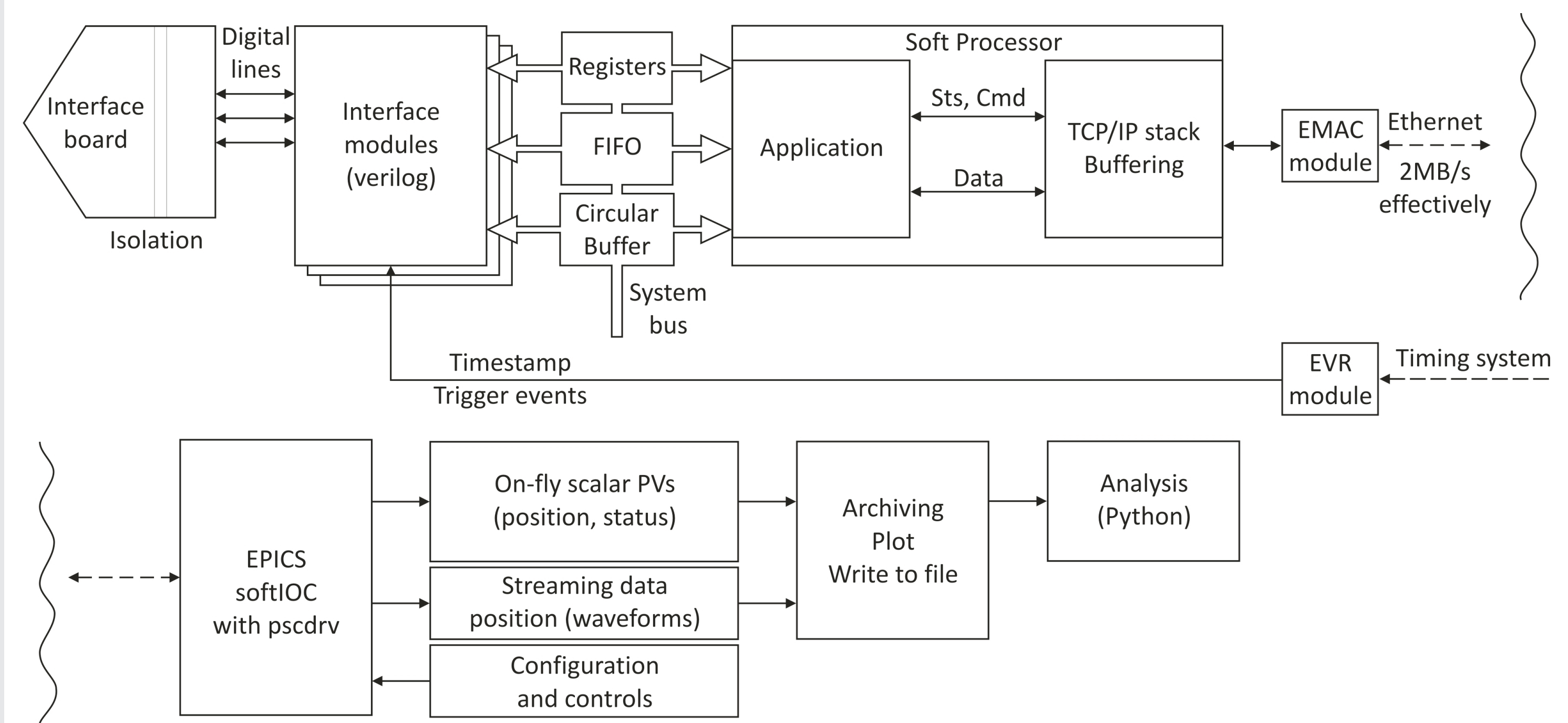
Channel circuitry



- Four identical individually isolated channels;
- Input and output interfaces are RS-422A compliant;
- Interface re-transmitted for a motion controller;
- Encoder supplied from the device or directly from the motion controller;

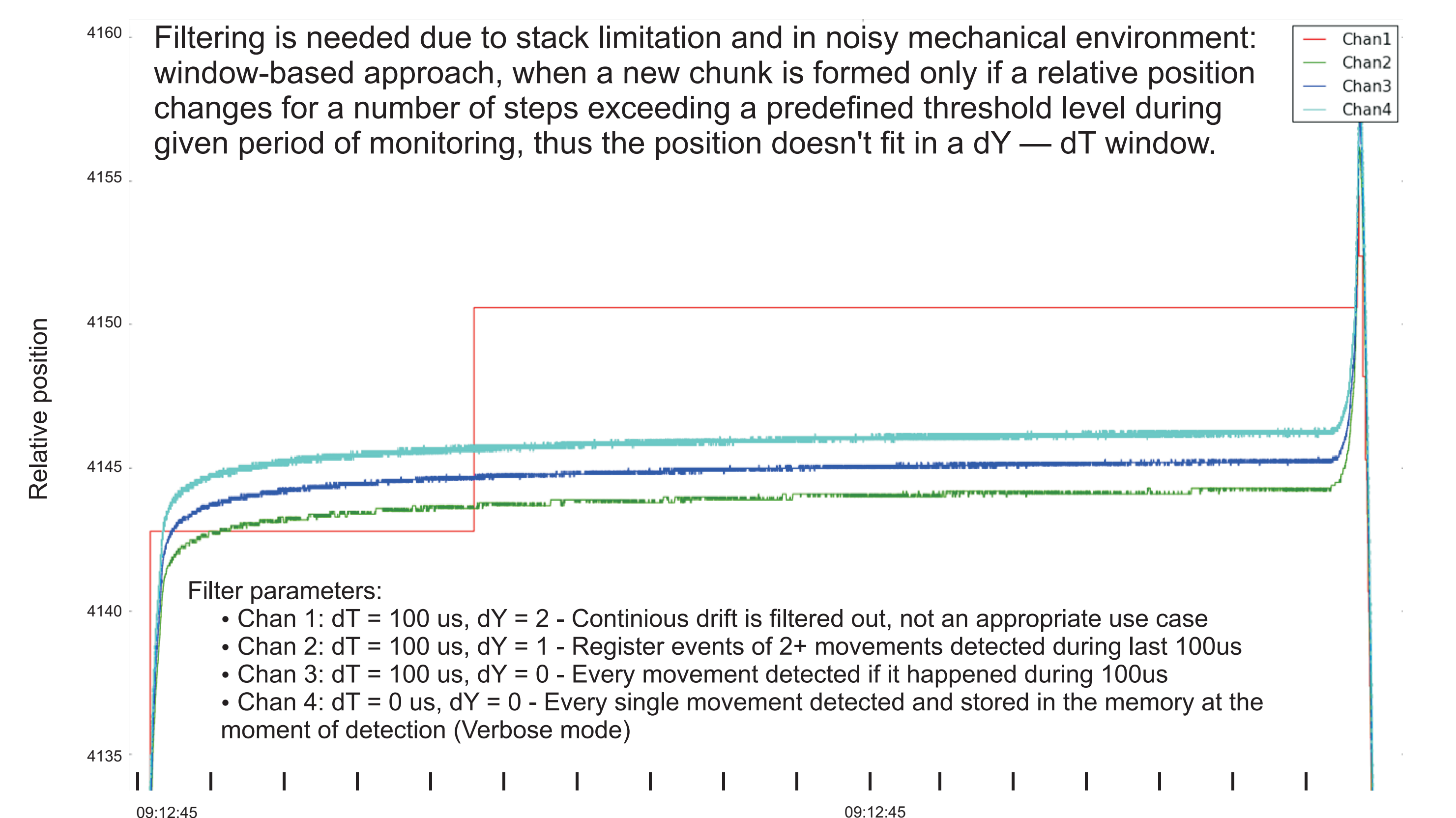
- Can be installed between an encoder and the motion controller with no interference to the system;
- Encoder supplied from the device or directly from the motion controller;
- Pinout matching Delta Tau GeoBrick and Renishaw encoder means straight cabling;

Firmware

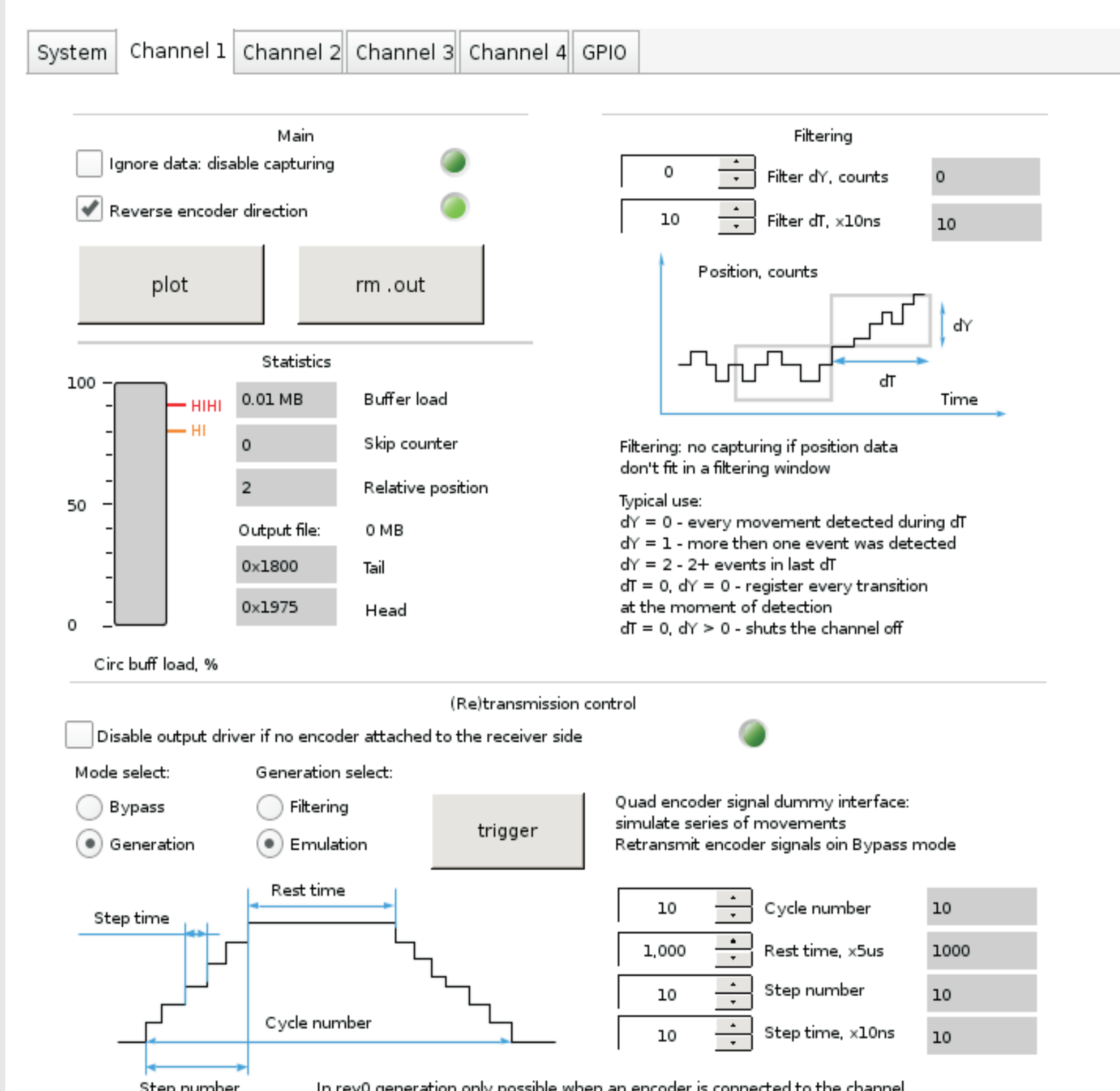


Simplified design dataflow

Position Capturing



Software



- EPICS soft IOC with Pscdrv, a portable streaming controller
- EPICS generic FPGA driver toolkit,
- Multiple socket connections,
- Waveforms written to file using EPICS aSub routine,
- Operator screen developed using Control system studio,
- Built-in Python scripts for data plot and work directory management.

Summary

Position capturing for quadrature incremental encoders, fits. 2U 19" platform. The Logic Leverages Virtex-6 FPGA. Encoder signals are re-transmitted for the motion controller, allowing the device to be installed between encoder and motion controller with no interference to the system. Option to supply the encoder directly from the board, generating internal timestamp. First series of eight pieces built and tested. Waiting for commissouing at Inner Shell Microscopy (ISS) beamline. Similar design concepts are realized in a new design of general purpose data acquisition and control board.