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Control of Fast-Pulsed Power Converters at CERN using a Function Generator Controller

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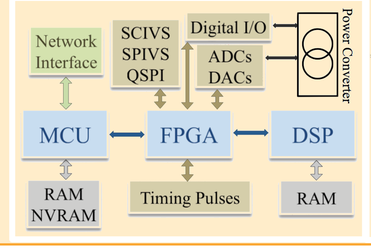
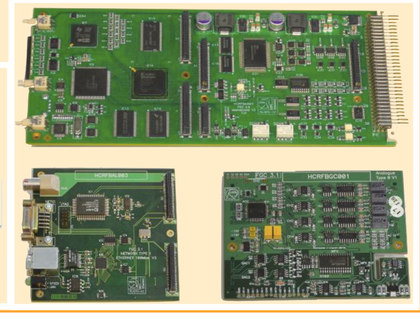
Function Generation Controller

CERN employs over **5,600 power converters**.

Cycling fast-pulsed power converters generate a **pulse** with a flat-top duration of just a **few milliseconds**.

The third generation of Function/Generation Controller (**FGC3**) is the latest platform for the control, monitoring and diagnostics of power converters.



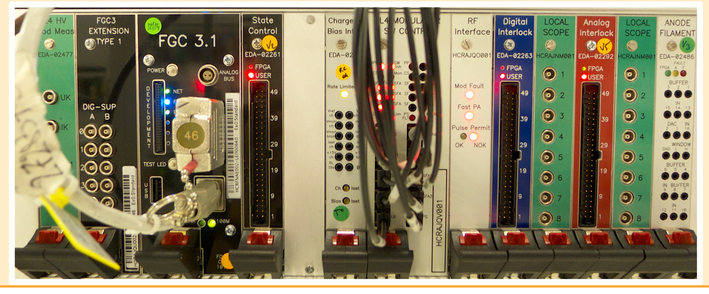


The FGC3 encapsulates three cards: a **mainboard** with an RX610 **microcontroller,** a TI TMS320C6727 floating point **DSP** with a 10 KHz interrupt-driven task and a Xilinx **FPGA** for glue logic and peripheral handling; an **analog card** with four high precision ADC channels and two 16-bit DACs; and an **Ethernet**-based communication card.

RegFGC3 chassis

FGC3s are typically integrated within a CERN-designed chassis called **RegFGC3**.

A common backplane links the FGC3 with a variety of cards and communication buses used to send the reference value, transmit configuration parameters and retrieved detailed diagnostics.

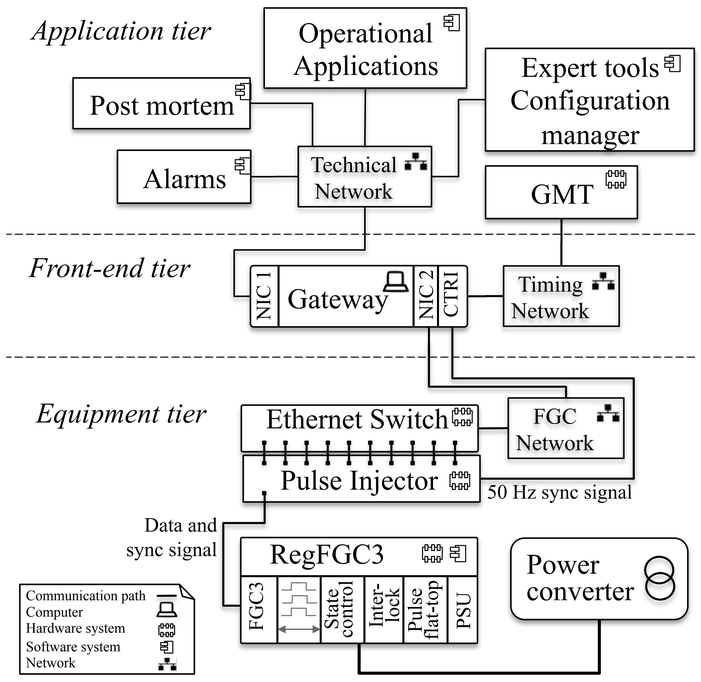


Control of power converters

The power converter control system is based on three layers:

- Control applications
- Linux based front-ends (gateways)
- Equipment devices (FGCs)

A **timing network** distributes real-time timing events. An **Ethernet network** is used to monitor and control the equipment devices via get, set and subscribe commands on properties.

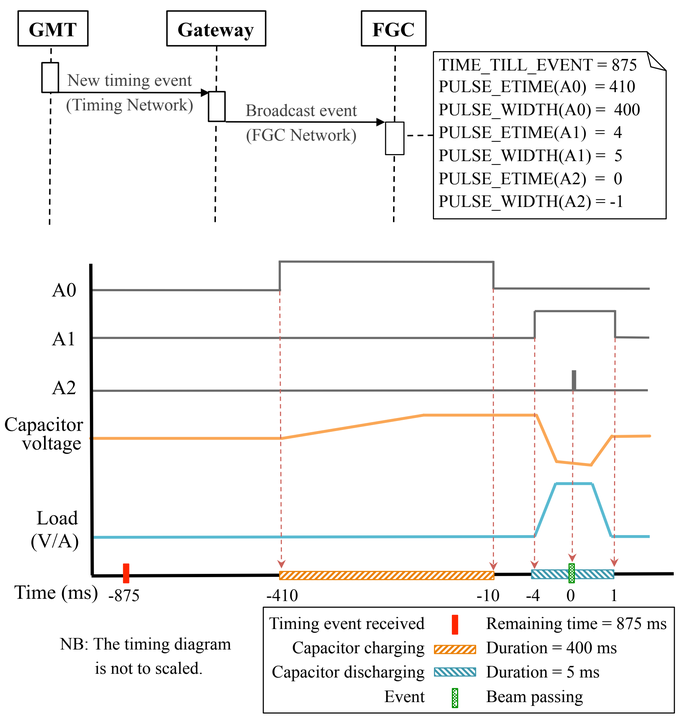


Timing distribution

The General Machine Timing distributes events containing the remaining time before the start of a cycle, beam injection or extraction. The gateways receive these packets in the CTRI and broadcasts it to the FGC3s.

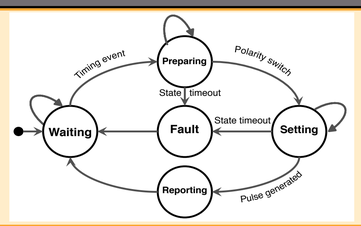
In addition, a **50 Hz synchronous signal** originated in the CTRI is routed to the FGC3 to discipline a **PI-based PLL**, which synchronizes a 25 MHz Voltage Controlled Crystal Oscillator. The resulting clock is fanned out to the MCU, DSP and FPGA making the software and firmware synchronous with the GMT.

FGC3 Software: state machine and timing pulses



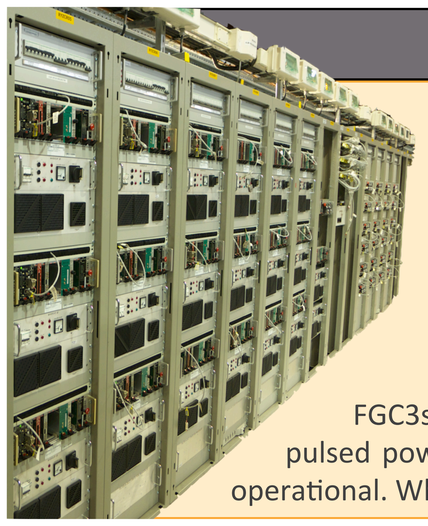
A sub-state machine has been added to sequence the generation of pulses.

- **Waiting**: waits for a timing event.
- **Preparing**: verifies if the current cycle is enabled and latches relevant parameters.
- **Setting**: configures the timing pulses and sends the reference value.
- **Reporting**: publishes the current and voltage measurements.
- **Fault**: logs error information.



The FGC3 outputs **timing pulses** to orchestrate the use of the capacitors stocking the energy needed to generate the current or voltage pulses.

FPGA registers define the time of the rising and falling edge of each pulse with respect to the event (beam). These registers are initialized based on the requirements of the fast-pulsed power converter. Converters with different topologies can thus be controlled homogenously.



FGC3 at Linac4

Name	Power	Pulse	FGC3s
Mididiscap	30 kW	5 ms	50
Maxidiscap	4 kW	2 ms	48
Modulator	5.5 MW	1.8 ms	14
H-Discap	150 kW	1.2 ms	3

FGC3s are used to control four types of fast-pulsed power converters. Currently, 29 circuits are operational. When complete, Linac4 will require **115**.

Results: time accuracy and precision

Timing accuracy is **~170 ns**. Inter-FGC3 time precision is **negligible** for FGC3s in the same gateway and cable length dependent for FGC3s in different gateways O(100) ns.