

Quick Experiment Automation Made CNPEM **Possible Using FPGA in LNLS**

M. P. Donadio^{*}, H. D. Almeida, J. R. Piton - CNPEM / LNLS, C. P. 6192, Campinas - 13083-970, Brazil

* marcio.donadio@Inls.br

The application

This system is designed for a synchrotron experimental station (a "beamline"). In this case, its purpose is SAXS/WAXS (Smalland Wide-angle X-ray scattering) measurements.

The system contains 2 main detectors: a Pilatus 300K (Dectris) to measure SAXS and a Pilatus 100K to measure WAXS. Pilatus 300K is configured to collect images at a given rate and sends a trigger TTL signal while an acquisition is being done.

Hardware used by LNLS SAXS1 beamline

cRIO with a FPGA algorithm: receive trigger signal \rightarrow open shutter \rightarrow collect voltage from SR 570 preamplifier until trigger signal is down \rightarrow close shutter \rightarrow calculate voltage average during the time the trigger signal was high \rightarrow save the data



A module of distributed I/O over EtherCAT, cRIO (NI), detects the trigger, opens the fast shutter and sends a TTL trigger to Pilatus 100K as it can start acquisition.

Two photo-diodes provide the beam intensity data through a SR 570 preamplifier that converts the current into voltage. cRIO reads this voltage and calculates its average while the trigger signal is high. The voltage average data is sent to PXI to be distributed to EPICS clients over the network.

FPGA code running in cRIO

Sum of the voltage from Stanford until Pilatus 300K sets the trigger signal low. After this, the average is calculated.

Receive Scan Engine raising edge and transfers voltage average from FIFO to 100 shared-variables to EtherCAT.

Communication loop

Real-time loop synchronized with Scan Engine receives data from EtherCAT and saves in an internal FIFO. This FIFO is read

Software in PXI





inside PXI and passed to a Linux IOC by a shared-memory.



Results

Trigger signal that is sent to the system, with 1.25 µs high and 20 µs low, resulting in a total period of 21.25 µs.



Signal that indicates when FPGA stopped to read the voltage signal and detects that the trigger signal was low.

The minimum period we get in the worst case was **21.25** μs.

