LANSCE CONTROL SYSTEM UPGRADE STATUS AND CHALLENGES*

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Abstract

The Los Alamos Neutron Science Center (LANSCE) linear accelerator drives five user facilities: Isotope Production, Proton Radiography, Ultra-Cold Neutrons, Weapons Neutron Research, and Neutron Scattering. In 2011, we started an ambitious project to refurbish key elements of the LANSCE accelerator that have become obsolete or were near end-of-life. The control system went through an upgrade process that affected different areas of LANSCE. Many improvements have been made but funding challenges and LANSCE operational commitments have delayed project deliverables. In this paper, we will discuss our upgrade choices, what we have accomplished so far, what we have learned about upgrading the existing control system and what challenges we still face.

INTRODUCTION

The LANSCE accelerator looks back at almost 45 years of operations. It was one of the first accelerators to use computer technologies to control and monitor its beam line components. It started out with a custom in-house design called RICE (Remote Instrumentation and Control Equipment) which was installed in the early 1970's when the facility was built. Since then, the facility has seen partial upgrades and extensions utilizing CAMAC, VME, and PLCs while introducing EPICS (Experimental Physics and Industrial Control System) in the 1990's as a supervisory software control application.

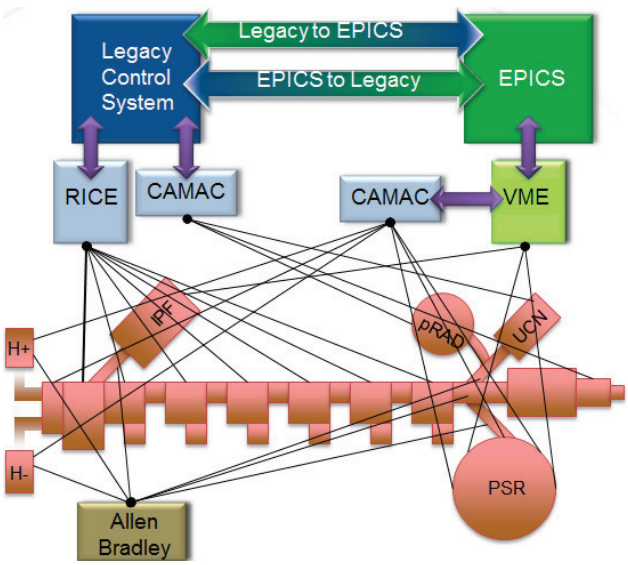

Figure 1: LANSCE Control System 1970-2010.

In 2011, LANSCE started a nine year rolling upgrade project which eventually will result in the complete replacement of the low-level RF system, the timing system, the timed data system, industrial control system, the beam-synchronized data acquisition system (including Beam Phase & Position Monitors (BPPM)), the fast protect reporting system and, wire scanner diagnostic equipment [1].

This upgrade project is primarily focused on ensuring reliable beam operations for a viable user program at the five experimental facilities. It will also benefit Los Alamos National Laboratory's future signature science facility called Matter-Radiation Interactions in Extremes (MaRIE) since, at its core, the 42-keV XFEL will be coupled with the existing LANSCE accelerator [2].

UPGRADE SCOPE

The monumental challenge of upgrading the control system is focused around the need to replace our VAX-based legacy control system which goes hand-in-hand with our RICE system. The VAX system has reached end of-life and the RICE systems, while a novel invention when it was designed in the late 1960's, is getting harder to maintain, and lacks the flexibility and performance of a modern distributed system with processing power near the front end.

RICE is a star configured control and data acquisition system that supports industrial control and beam-synchronized type of data acquisition. At its heart, the RICE Interface Unit can issue a parallel RICE module read request that provides a transverse snapshot of the accelerator. This implementation resembles the functionality of a timing system which provides trigger gates to distributed data acquisition equipment.

Given the complex functionality, replacing the RICE system is not an easy task and one starts to appreciate the engineer's ingenuity to design such a system about half a century ago.

Industrial Control

The first part of our RICE upgrade project addresses the Industrial Controls (slow control). We chose a Programmable Automated Controller (PAC) built by National Instruments (NI). The controller is called CompactRIO (cRIO) and is a reconfigurable control and data acquisition system which is supported by EPICS [3]. The NI cRIO–9024 embedded real-time controller features an industrial 800 MHz processor and contains, 512 MB DDR2 RAM, and 4GB of non-volatile storage. The removable cRIO controller sits in an NI cRIO-9118

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chassis with eight accessory slots, and a user programmable Xilinx Virtex-5 LX110 Field Programmable Gate Array (FPGA). The most noticeable advantages are reliability, high performance and hot swappable modules and a high performance FPGA. For our application, the cRIO is hosted in a commercial BiRIO rack-mount chassis which interfaces to commercial BiRIO interface boards that in turn provide interfaces to the device field wiring.

Figure 2: cRIO in BIRO chassis.

National Instruments provides a wide variety of modules that cover most of our needs. Beyond that third-party products complement the NI module product line. If that still doesn't meet the needs, a Module Development Kit (MDK) allows the development of custom modules to meet the unique needs of particular products and applications.

The cRIO is a fast and flexible solution at a reasonable price point. The typical response time is in the µsec range vs. msec in Programmable Logic Controllers (PLC). In addition, the cRIO provides more programming flexibility than a PLC. The cRIO FPGA and Real Time Controller (RTC) running VxWorks, are programmed in LabVIEW. The RTC embedded EPICS IOC (with a complete environment - all record types and fields are visible and available) makes this solution a standalone EPICS IOC which communicates with the RTC LabVIEW Real Time code via a shared library. Another advantage is that the independently running FPGA, interfacing directly with the cRIO I/O modules keeps running even though the EPICS IOC is rebooted. This can be helpful if interlock functionality needs to continue even when the IOC has to undergo maintenance. Last, but not least, the whole system maximizes its flexibility through the freedom on how an application is partitioned between the FPGA, LabVIEW RTC, and EPICS database code [4].

Beam-Synchronized Data Acquisition

The second part of the RICE system replacement effort focuses on the beam-synchronized data acquisition. The hardware solution chosen is a cPCI/VPX architecture in one crate allowing the communication between both sides via a PCI Express communication bridge. VPX is an ANSI standard (ANSI/VITA 46.0-2007) that provides VMEbus-based systems with support for switched fabrics over a new high speed connector [5].

Figure 3 provides the front view of our cPCI/VPX chassis. On the left we have three 250W, 3U high plug-in power supplies with an additional power supply expansion slot for redundancy. Located to the right of the power supplies are the six 3U VPX slots. The picture shows two test cards inserted, one of which is an Ethernet controller providing network connectivity to all VPX slots via the backplane. On the right side of the chassis are eight 6U cPCI slots.

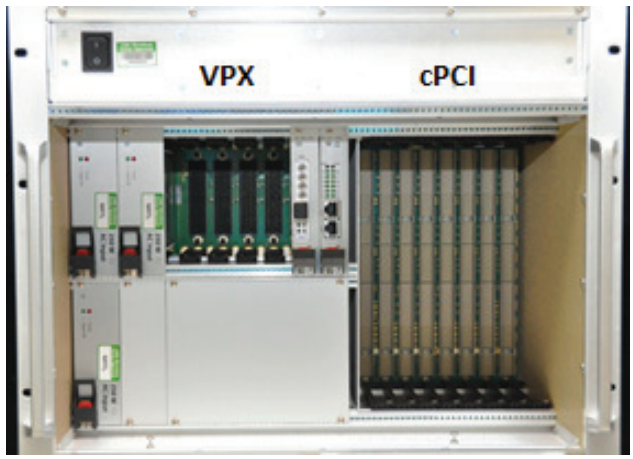

Figure 3: cPCI/VPX Chassis Front View.

This architecture will be used for the BPPM system. On the cPCI side the signals from 4-electrodes (top, left right, bottom) are captured along with the accelerator reference signal. The signals are then conditioned to 201.25 MHz RF waves and then transported to the VPX side where a high speed digitizer captures the data at 4-nanosecond time increments in order to analyse beam position and phase variations that occur throughout the 1 millisecond pulse cycle. Timing for synchronous measurements between BPPMs and beam specific information is provided by an event receiver (connected to the master timer via optical links) on the cPCI side that provides the timing and beam species information prior to submission to the EPICS database. A soft core processor, which resides in FPGA fabric, is used to store the results to the EPICS database for use by beam operators [6].

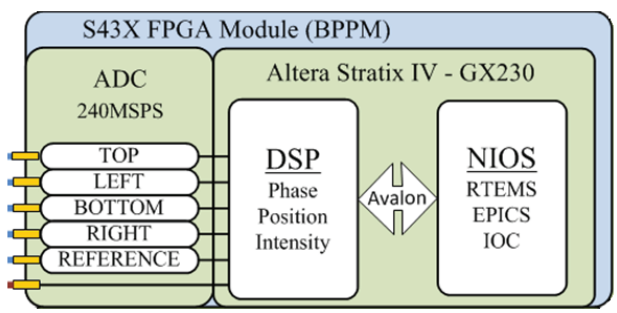

Figure 4: FMC Carrier Board with Altera Stratix IV FPGA and front end ADC.

The BPPM hardware solution on the VPX side shown in Figure 4 is very adaptable and will be used for our other beam-synchronized data acquisition application needs. It consists of a FPGA interfaced Mezzanine Card (FMC) [7], that hosts an Analog Digital Converter (ADC) and an Altera Stratix IV-GX230 [8]. The latter hosts an

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embedded EPICS IOC running the RTEMS operating system on a NIOS-II softcore. The hardware/software solution has numerous advantages:

- Enables buying hardware COTS but still employs high performance hardware design
- FMC enables custom Digital Signal Processing (DSP) solutions in hardware without custom board design
- Ensures an independent and incremental upgrade path for AFE (ADC), DSP, or IOC
- Integrates ADC, digitizer module, signal processing EPICS IOC all into one board
- Highly distributed, therefore increased fault tolerance

Timing System

Essential to beam-synchronized beam operations is the timing system which undergoes a change from a centralized gate generating system to a distributed event-based system where timing gates are generated locally. The new Timing Pattern Generator (TPG) is a dual-redundant system. Each of the redundant TPG's has a VME-64x crate, a MVME-6100 processor, a set of Micro Research Finland (MRF) event-generator modules, and an AC zero-crossing detector and beam-enable logic module (implemented in a cRIO system). The cRIO FPGA-based beam enable logic has been used to implement specific features, such as enabling or disabling a beam from the operator consoles, single-shot mode, single-burst mode, continuous-burst mode, burst of bursts mode, and cycle stealing. The new TPG has performed successfully during the 2014/15 run cycle interfacing to the old (RICE) and new timing distribution system (fibre optics to local Event Receiver). While the TPG work is complete the distributed event-based generating devices (Timing IOCs), some of which are tightly coupled with our Low Level RF system, still need to be installed during future maintenance periods [1].

Wire Scanner

The cRIO platform is also used to upgrade our aging Wire Scanner control and data acquisition system that has been using RICE and CAMAC (Computer Automated Measurement And Control) technology. Beyond the cRIO Industrial Control configuration, the Wire Scanner cRIO chassis has an NI TPC-2206 Touch Panel Computer integrated into the chassis front panel to provide real-time visual display of wire-scanner operation and direct manual control of the wire-scanner actuator [9].

Furthermore, the project took advantage of the cRIO National Instruments MDK to design a specific, commercially unavailable, cRIO AFE module. The design has been built by and is available through National Instrument's Alliance Partner BiRIO. This Analog Front End (AFE) module is a dual channel, transimpedance amplifier with dual summed inputs and true DC coupling to collect the charge signals from the sense wires. It is designed to accommodate comparatively long macro pulses (>1ms) with high repetition rates (>120Hz) without the need to provide integrator reset signals. The basic AFE bandwidth is flat from true DC to 35 kHz with a well-defined first-order pole at 35 kHz. Numeric integration is utilized in the cRIO FPGA to provide pulse-to-pulse numeric integration of the AFE signal to compute the total charge collected in each macro pulse [10].

Other Controls and Diagnostics Equipment

Beyond what has been described so far we have other systems that need to be upgraded to allow us to retire RICE and the associated Legacy Control System. Among others, this includes the Harp and Emittance diagnostic equipment mostly located along our linac.

For the Harp, a cRIO based system is in production at our 1L target. This design will be leveraged to replace the remaining Harp systems. The current design has three AFE boards and one integrity board outside the cRIO but housed within a BiRIO chassis. Logic signals for beam synchronization and AFE control connect to the cRIO through a single NI-9401TTL logic module. Signals generated by the AFEs are digitized by three NI-9220 ADC modules. Finally, one NI-9475, 60V-source module is incorporated for integrity pulse generation that used is to check continuity of the Harp wires [11].

For the Emittance stations we are still working on our design but we are confident that the cRIO system will meet the requirements and become the platform of choice.

Another system in need of replacement is our CAMAC system that provides timing and data acquisition solutions. For the most part we have been very successful and found cRIO modules with similar functionality of the CAMAC module that needed to be replaced. Other CAMAC module functionalities are not that easily replaceable and we are diligently working on a path forward.

UPGRADE STATUS & CHALLENGES

At the beginning of the project we focused on engineering solutions that would minimize the number of hardware platforms we would need to introduce and still meet all our technical requirements. We believe that our cRIO and cPCI/VPX based platforms meet that objective. The controls upgrade project is only one part of a larger investment to upgrade the LANSCE accelerator. Funding levels have been flat for the project and did not consider the year to year funding needs to execute the project in the most effective fashion. This, combined with some unexpected funding adjustments for other non-controls project scope elements, added a great deal of uncertainty to whether we would be able to do everything we had planned for.

Therefore, after the design phase, we chose to focus the majority of our controls scope elements on the purchase of the equipment vs. purchase & installation. Hoping that if we have all the hardware in hand, we will find the funding to install it either through remaining project funds, one-time funding, and/or through our maintenance budget.

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Table 1: Control System Upgrade Project by Numbers; (#) Number of WS Ctrl. & Data Acq. Chassis only.

	RICE to Industrial Controls	RICE to Synchronized Data Acq.	BPPMs	Wire Scanner	CAMAC to cRIO	HARP	Emittance
Total Number of Systems to be upgraded	66	66	34	53	38	32	3
Upgrades Installed / In Production	9	0	0	4	28	1	0
Equipment on Hand but Not Installed	27	31	7	8 (40)	2	0	1
Remaining Systems to be Purchased	30	35	27	41 (9)	8	31	2

This, however, has led to some unintended consequences. Not all of the control subsystems and/or related non-control subsystems designs are at the same maturity level. For example, while the majority of the wire scanner controls equipment (Table 1: #s in brackets) is ready for installation, the associated actuator has not been funded at the level that would allow us to install a completely new system. This in turn, made us explore the possibility of retrofitting our new Wire Scanner controls chassis to the old actuator still in the beam line. Furthermore, our RICE to cRIO (Industrial Control) upgrade has progressed with nine units installed while we don't have a RICE to cPCI/VPX (Synch. Data Acq.) unit in production. This is inefficient since we will need to get back to those systems that have been upgraded to the new cRIO subsystem in order to install the cPCI/VPX subsystem in order to retire a whole RICE unit. So far we still have all of our RICE units in production. However, 9 of them only run the beam-synchronized data acquisition.

Table 1 shows a numerical overview of our controls subsystems that need to be upgraded (row 1); subsystems hardware that have been upgraded (row 2); hardware that has been purchased for a pending upgrade (row 3); and subsystem hardware that still needs to be purchased such that a system can be upgraded (row 4).

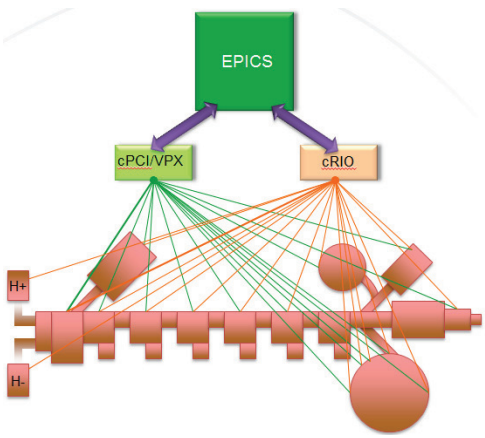

Figure 5: LANSCE Control System 2020.

Our progress has been hampered by the funding limitations and uncertainty. Furthermore, all installation work needs to be done during our 4 month maintenance period on top of all other maintenance that needs to be done without additional labor resources. Our ultimate goal is shown in Figure 5 (compared to Figure 1) with EPICS as a supervisory control system.

CONCLUSION

The cRIO and cPCI/VPX are flexible hardware and software solutions and therefore adaptable to a wide range of control and data acquisition problems. With most of the LANSCE Control System design work complete the project has transitioned to purchasing and installation. Significant work still lies ahead to complete this monumental control system upgrade task by 2020.

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