CNPEM
Brazilian Center for Research
in Energy and Materials

Brazilian Synchrotron
Light Laboratory

Development of an Open-Source Hardware Platform for Sirius BPM and Orbit Feedback

ICALEPCS 2013, San Francisco

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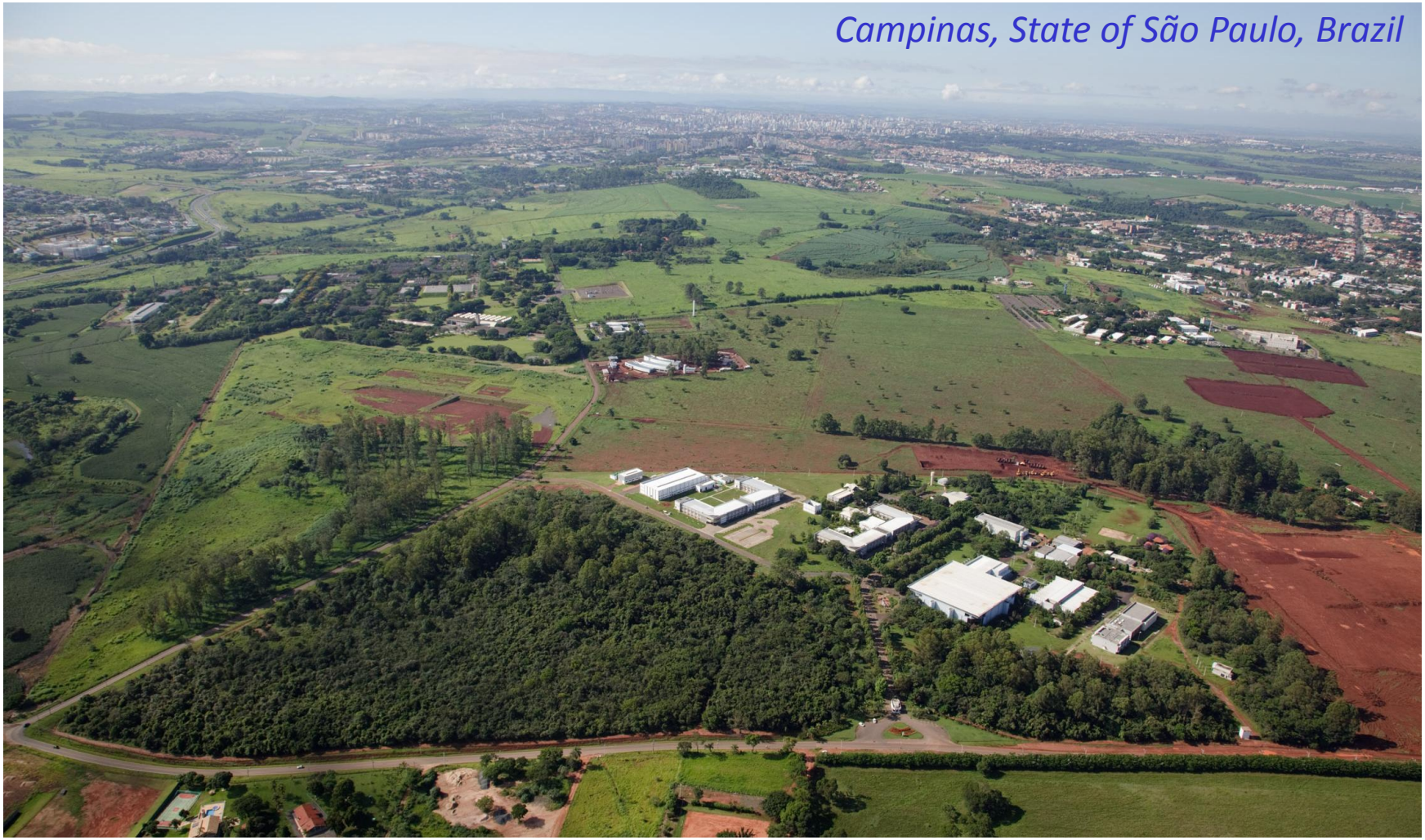
October 9, 2013

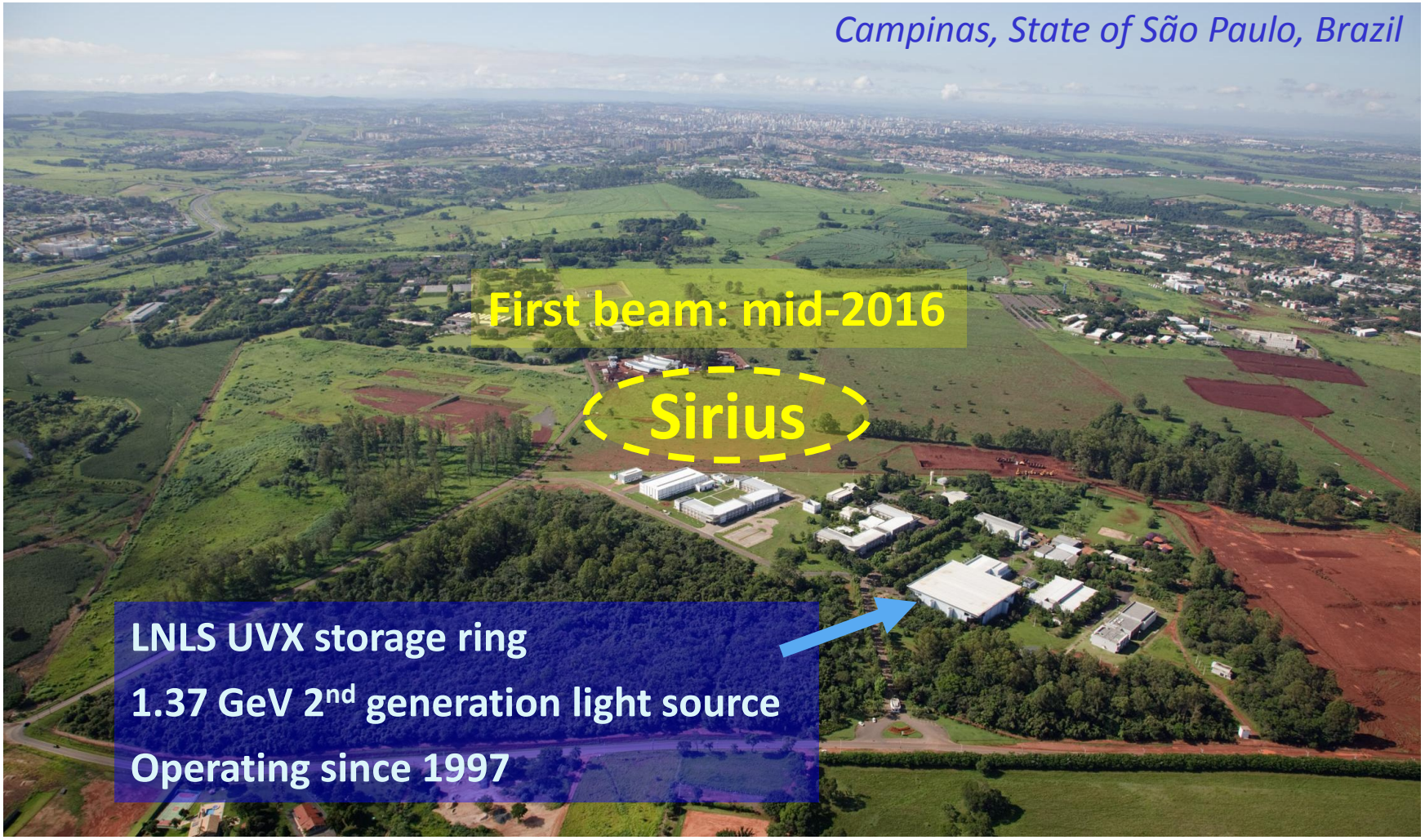
Outline

- Introduction
- System Requirements
- System Architecture
- Hardware designs
- HDL and Software designs
- Results and Issues
- New developments
- Collaboration
- Conclusion

Introduction



Introduction

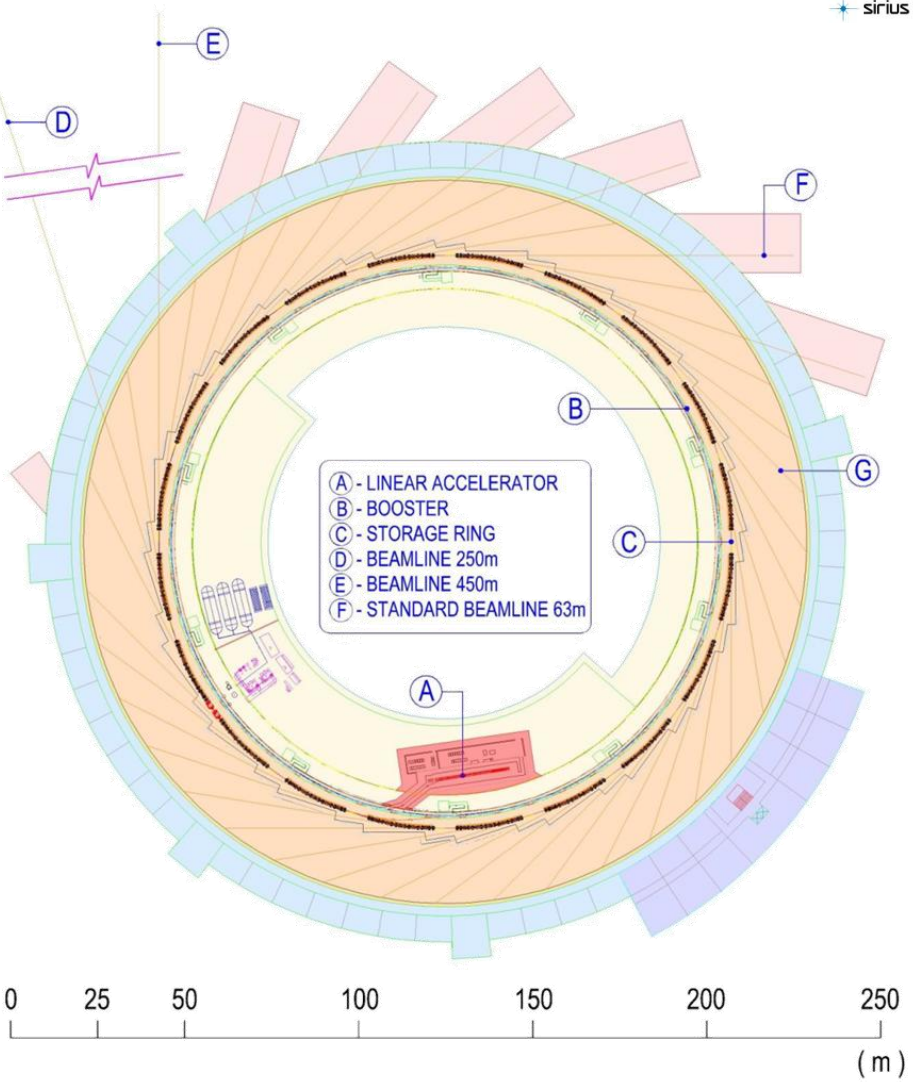


Introduction

Introduction

Sirius light source

- 3rd generation light source providing diffraction-limited photon beams
- Vertical emmitance @ 1% coupling: 2.8 pm.rad
- RF frequency: ~500 MHz
- Natural bunch length: 8.8 ps
- Circumference: 520 m
- Tightest BPM/orbit feedback requirement: **vertical beam position RMS displacement < 140 nm (0.1 Hz to 1 kHz bandwidth)**

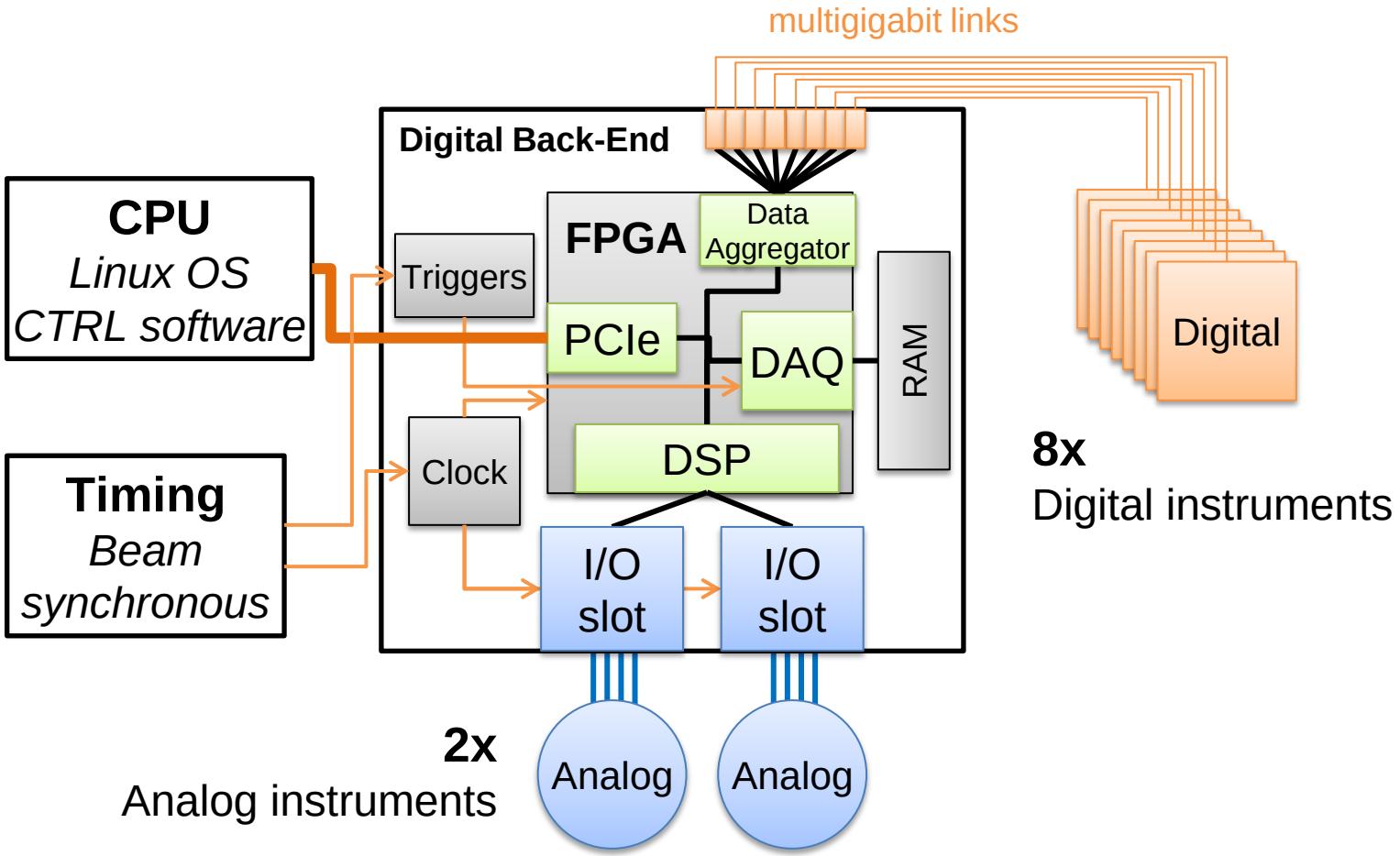


System Requirements

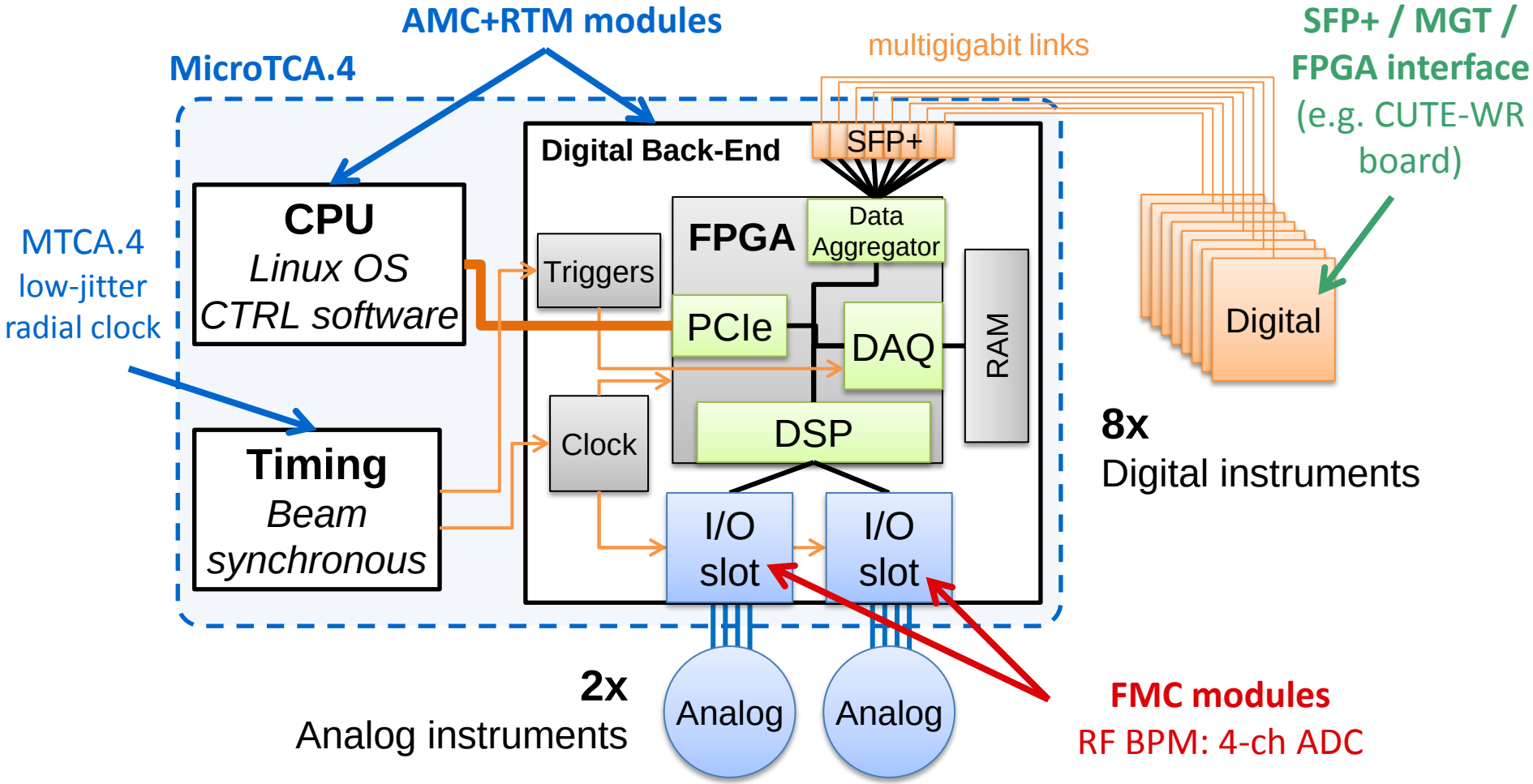
- Sirius Beam Position Monitor (**BPM**) system:
  - Ordinary accelerator data acquisition system requirements:
    - **Beam synchronous**
    - Triggered acquisition – **100 MB** to **1 GB** range
    - Programmable logic resources (basically **FPGA**)
    - Integration with accelerator-wide **distributed control system via 1 Gb Ethernet**
  - Special requirements for analog/mixed-signal performance:
    - **SNR > 100 dB** (per channel) @ orbit feedback bandwidth
    - **Gain long-term drifts < 1 mdB RMS** (temperature + beam current dependences)

- Sirius storage ring Fast Orbit Feedback (**FOFB**) system:
  - Update rate: **> 100 kS/s**
  - Closed-loop latency: **< 25 μs**
  - Sensors: **240** RF BPMs, **17** insertion device gap/phase encoders, **~70** X-Ray BPMs
  - Actuators: **~440** orbit corrector power supplies

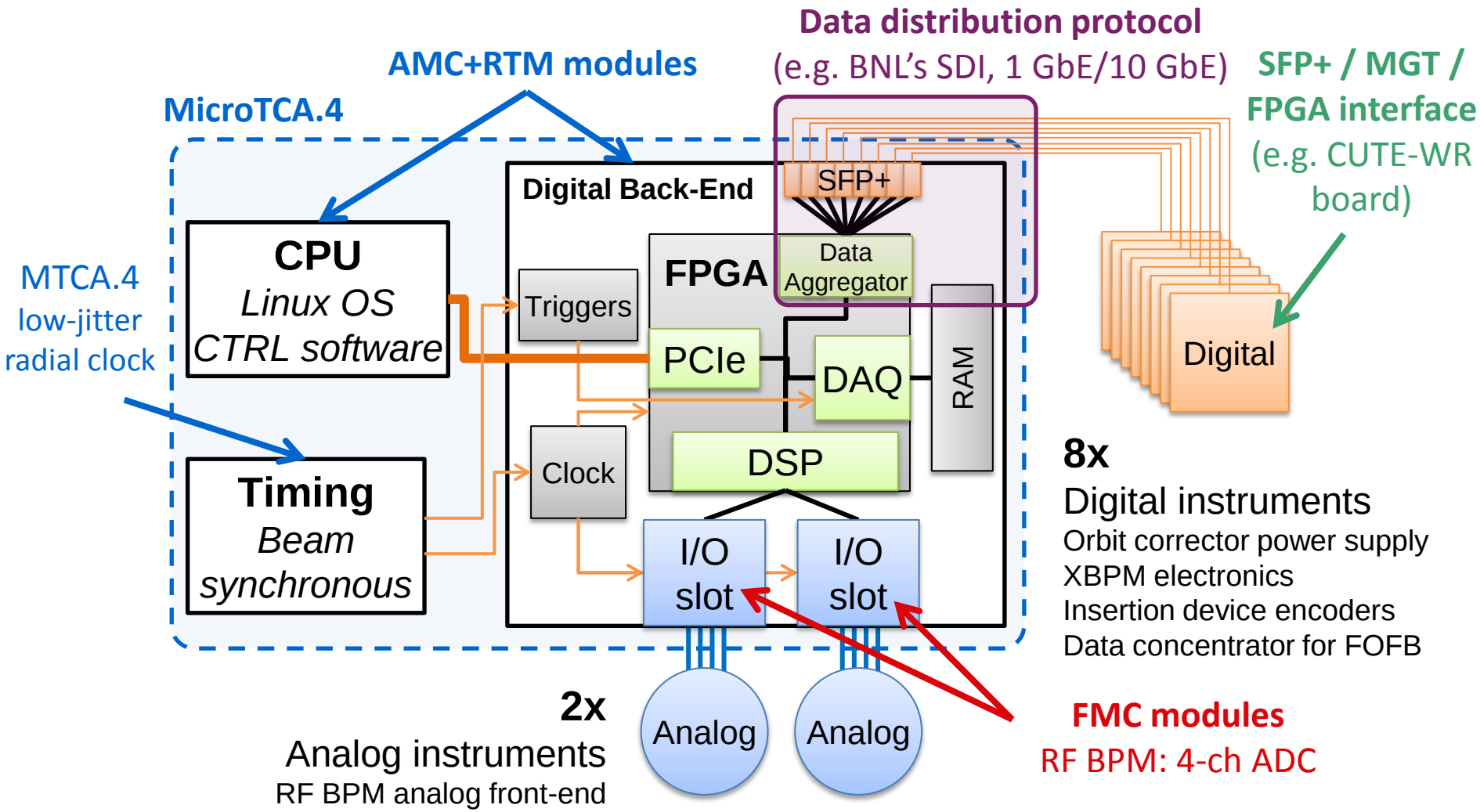
System Architecture



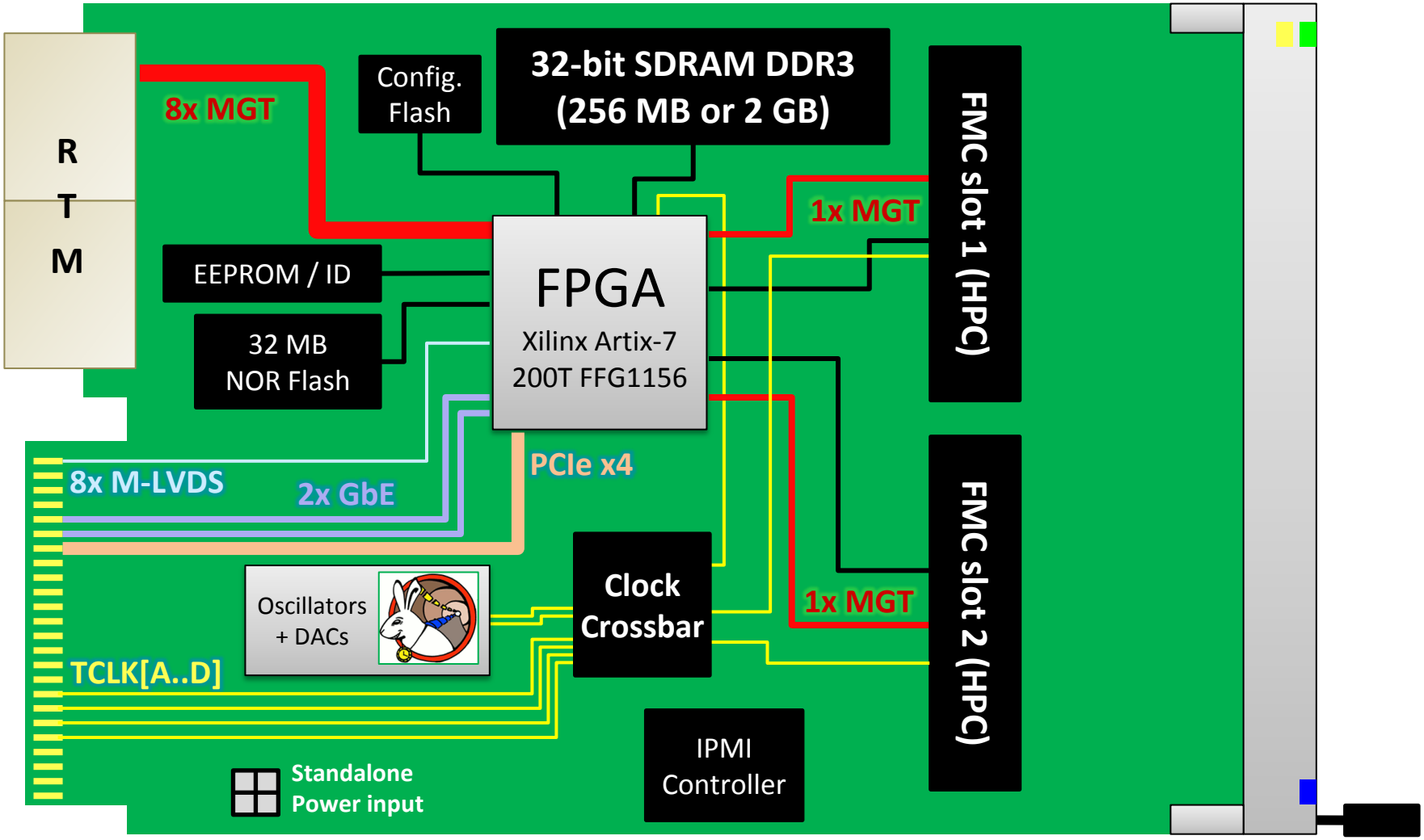
System Architecture



System Architecture



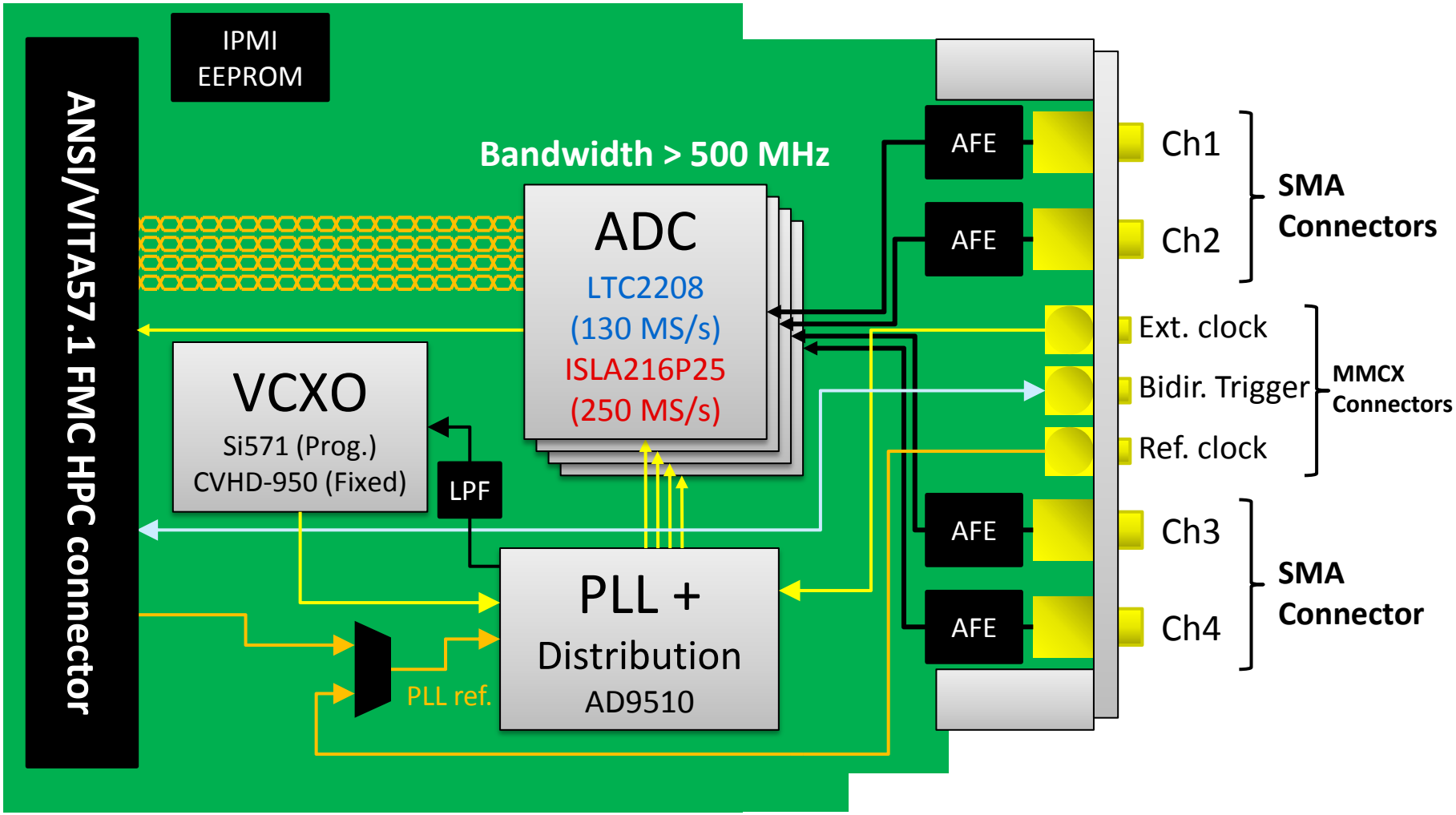
Hardware designs (AMC FMC Carrier)



Hardware designs (AMC FMC Carrier)

Designed by Warsaw University of Technology (WUT) for LNLS

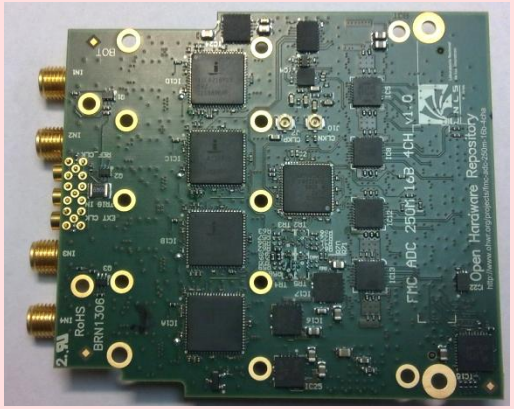
Hardware designs (FMC ADC)



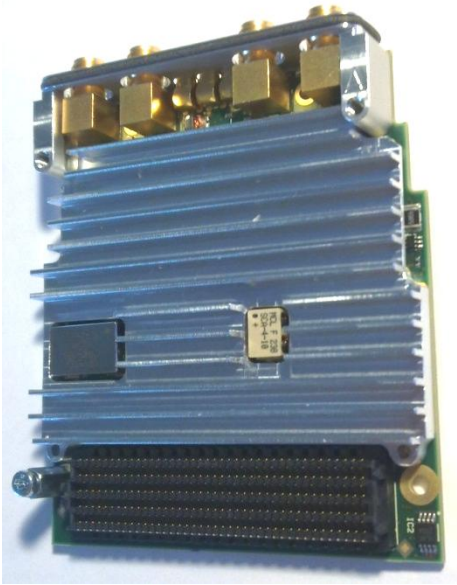
Hardware designs (FMC ADC)

LTC2208 (130MS/s) - LNLS design

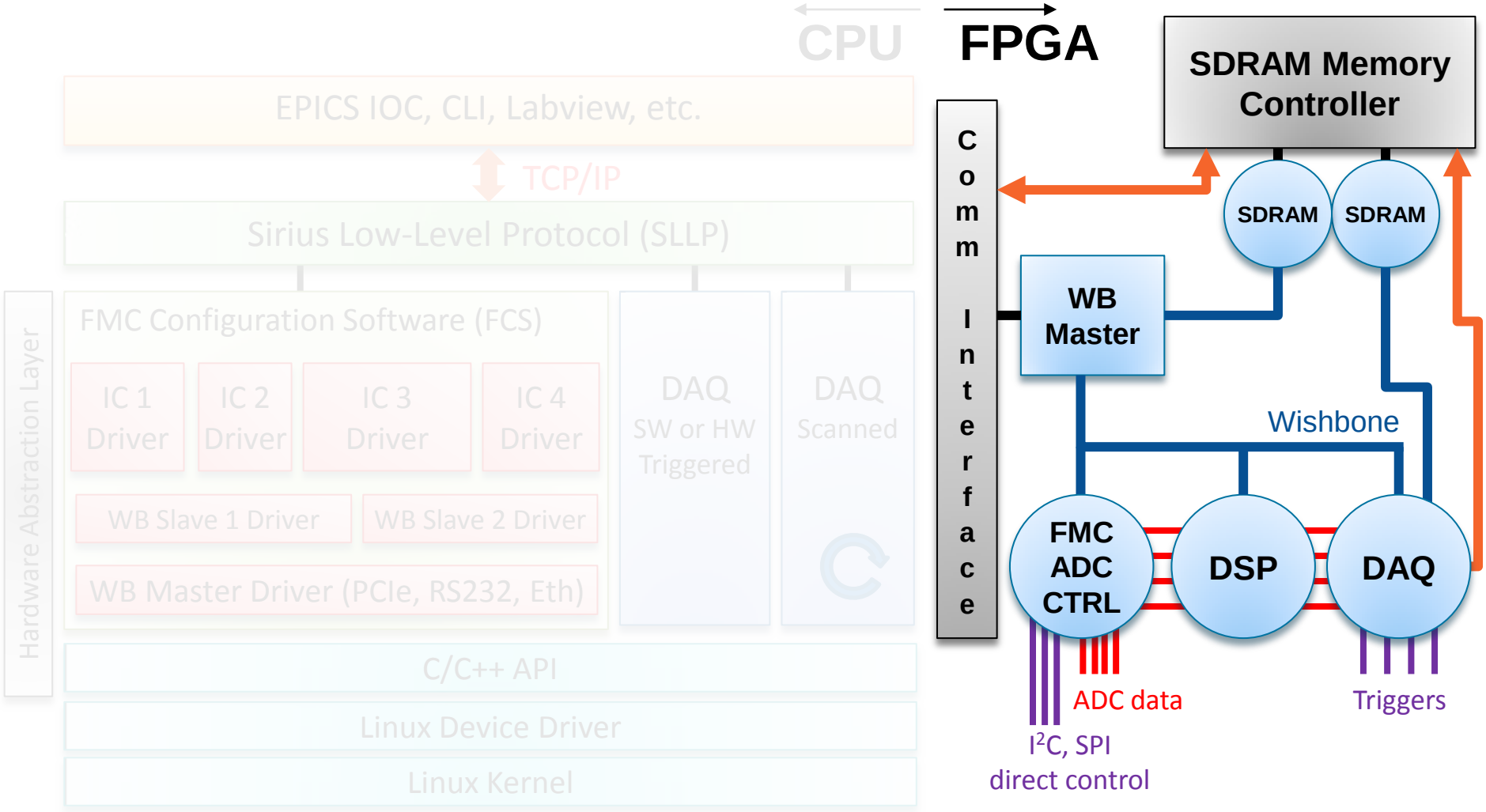
ISLA216P25 (250 MS/s) - WUT design



Common shielding/heatsink, front panel and connectors



HDL and Software designs



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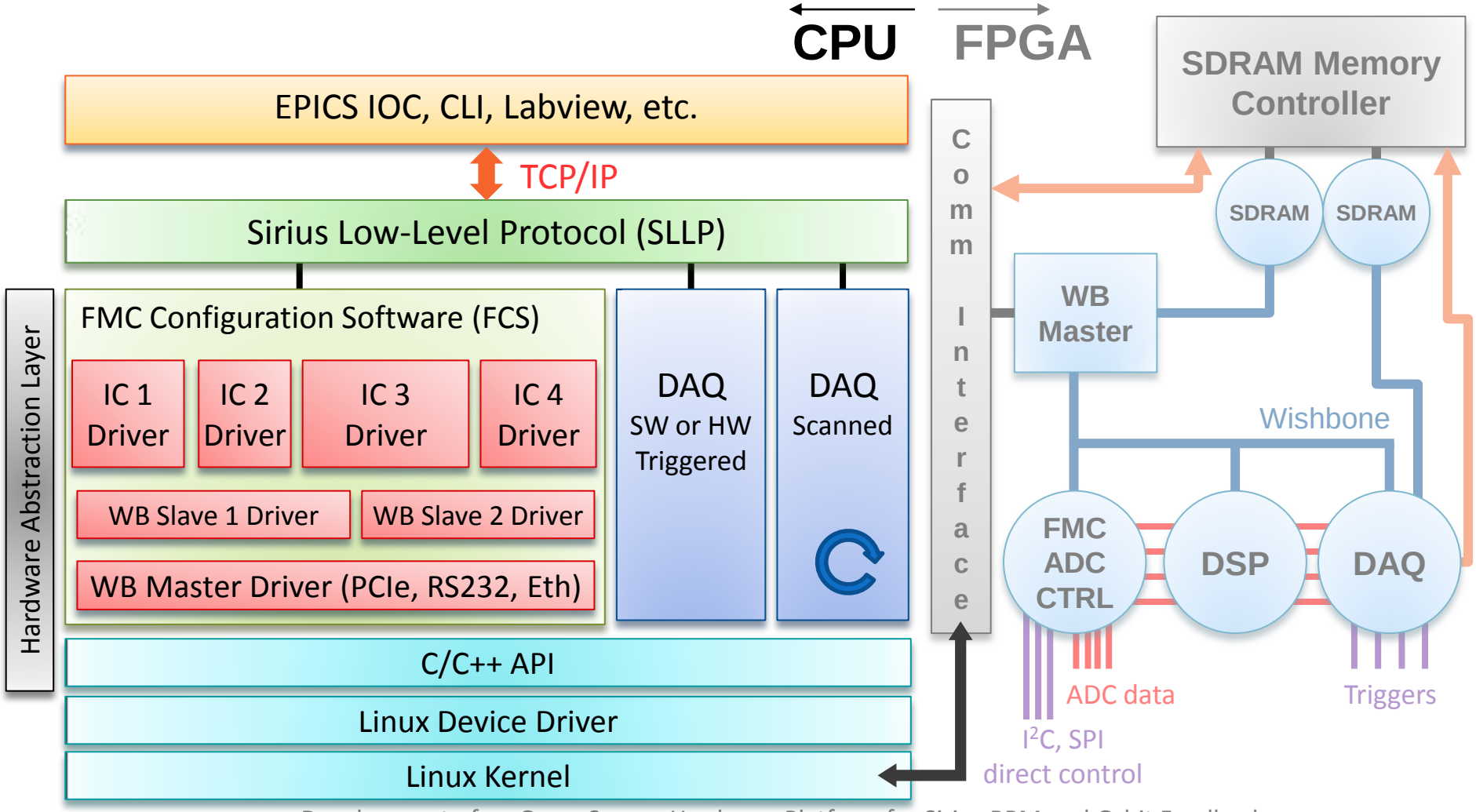

Results and Issues

Sirius BPM RF Front-End	☺	1st version layout 100% correct, standalone performance meets specifications. **Details in IBIC'13 papers: WEPC07, MOPC09**
AMC FMC Carrier tests	☺	No major problems found on 1st prototype tests
Digital Signal Processing	☺	Basic Beam Position Monitor math is currently done with System Generator (porting for open-source HDL is still pending)
Local Bus	☺	Wishbone B4 sucessfully employed, seamless substitution of bus master (PCIe, LM32, RS-232 controller), large reuse of HDL code
PCI Express	☺	130 MB/s(read) and 170 MB/s (write) performace on PCIe Gen1 x1
FMC ADC 130 MS/s	😐	High distortion (THD > -65 dBc) for input powers > -8 dBm
FMC ADC 250 MS/s	😐	High attenuation @ 500 MHz (> 12 dB) + poor S11
MicroTCA platform	😐	IPMI incompatibility between Vadatech MCH and N.A.T. power supplies → severe startup and cooling failures
AMC CPU	☹	PowerPC P2020 → strong ties to vendor's outdated Linux SDK Moving to x86 → easier software development, better support

Collaboration

- CERN Open Hardware Licence + GNU General Public License (GPL)
- Designs and codes hosted at:
  - http://www.ohwr.org/projects/bpm
  - http://www.ohwr.org/projects/bpm-rffe
  - http://www.ohwr.org/projects/bpm-sw
  - http://www.ohwr.org/projects/afc
  - http://www.ohwr.org/projects/fmc-adc-130m-16b-4cha
  - http://www.ohwr.org/projects/fmc-adc-250m-16b-4cha

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WARSAW UNIVERSITY OF TECHNOLOGY

OPEN HARDWARE REPOSITORY

Conclusion

- The concept:
  - **Modular**
  - Based on proven and emerging **standards**
  - **Open-source** hardware and software
- Current status:
  - Overall hardware functionality and performance have been proven
  - Efforts for **improvements on ADC** boards are ongoing
  - New round of board prototypes is foreseen to **December 2013**
- Next steps (6 – 12 months):
  - Improve existing hardware designs
  - Build remaining hardware: RTM with 8 SFP+ cages, universal FOFB node
  - Refinements on DSP chains + data acquisition engine
  - Control software integration: EPICS IOC, CLI utility, Labview, etc.
  - Timing system interface
  - Fast Orbit Feedback data distribution

Thank you!

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