Why a new kit	Introduction to OH	OH products	Gateware architecture	New tools	Future work & conclusions

CERN's FMC kit

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CERN, Geneva, Switzerland

ICALEPCS 2013, San Francisco, 9 October 2013



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- Introduction to Open Hardware
- Open Hardware products
- Gateware architecture
- 6 New tools



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Why a new kit ●○○ OH products

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CERN Beams Controls group

Responsible for

- Specification, design, procurement and operation of electronic modules
- Linux device drivers, C/C++ libraries, test programs

Hardware kit

- Analog and digital I/O
- Level converters, repeaters
- Serial links, timing modules

Currently, October 2013

- About 120 module types
- Most are custom designed: only 1 in 4 is commercial

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Whv a	new kit?				

Motivations to design a new kit

- \bullet Obsolete components/modules \rightarrow can't build/buy
- Limited stock \rightarrow no new installations
- Incomplete/nonexistent documentation

New approach

- Open and modular designs
- Compliant with existing standards

Carrier-mezzanine concept

- Only one complex design per platform (carrier)
- Reduce number of supported modules

Use of s	standards				
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Based on standards

- Platform bus: VME, PCI, PCIe, PXIe
- FMC (FPGA Mezzanine Card, ANSI/VITA 57.1)
- Wishbone FPGA internal bus
- Linux device drivers

Contribute to standards

- Wishbone pipelined mode: Wishbone spec Rev.B4 (2010)
- FMC bus Linux driver structure: in Linux v3.11
- ZIO Linux framework for DAQ and CTL hardware: RFC made to Linux Kernel list

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Why we use Open Hardware

Fully specify the design

Avoid black boxes.

Better designs

• Peer review by experts, including companies.

Knowledge sharing by design re-use

- One of CERN's key mission.
- Stimulates collaborations, inside and outside CERN.

Healthier relationship with companies

- No vendor-locked situations.
- Small companies can play important role.

OH repository and license

Open Hardware Repository – ohwr.org

- Web-based collaborative tool for electronics designers
- Wiki, File repository, Issues management, Mailing list, News
- Readable by everyone, without registration

CERN Open Hardware License – ohwr.org/cernohl

- Developed by Knowledge Transfer Group at CERN.
- Better suited than non-HW licenses (GPL, Creative Commons...)
- Defines conditions for using and modifying licensed material.

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Open Hardware products

More than just a board

- Hardware board
- FPGA gateware
- Linux driver
- Production test system

Carriers

- Three fully supported (VME, PCIe, PXIe)
- Six other carriers (VXS, AMC, stand-alone)

Mezzanines

- Four fully supported (ADC-100M, TDC, DIO-5ch, FD)
- About a dozen other mezzanines (ADC, DAC, DDS, DIO)

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Commercialised in Germany



Matthieu Cattin CERN's FMC kit

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SPEC - Simple PCI Express FMC carrier Commercialised in Spain, The Netherlands & Poland



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A modified SPEC board



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FMC mezzanine: 5-channel 1ns TDC A joint development by TE/ABT, TE/CRG & BE/CO



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FMC mezzanine: 100 MSPS 14-bit 4-channel ADC



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Project	Producers	Users	Produced
SPEC carrier - PCIe	3	41	300
SVEC carrier - VME	2	4	105
SPEXI carrier - PXIe	1	2	(proto) 3
ADC 100M 14b 4ch	2	11	70
TDC 1ns 5cha	1	3	70
FMC DEL 1ns 4cha	3	4	108
FMC DIO 5ch	3	10	92
WR switch 18 ports	1	11	77

Table: eight CERN OH designs found producers and users

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Gateware architecture

Wishbone for modularity

- Open standard
- Simple, uses few FPGA resources
- Collection of cores already available (OpenCores)

New cores developed

- At CERN: VME64x, PCIe, DDR3, ...
- By collaborators: Wishbone crossbar (GSI), ...

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Future work & conclusions

Example: FMC-ADC gateware architecture



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Gateware design tools

hdlmake: Automating HDL design flow

- Generates Makefiles for synthesis and simulation.
- Project structure described in Manifest files.
- Solves dependencies (fetches remote ones).

wbgen2: Wishbone slave generator

- Describes structure in a single text file.
- Automatically generates HDL source, C header and documentation.
- Generates registers, RAM, FIFO, interrupt controller.

Both FOSS tools available on ohwr.org

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wbgen2: HTML documentation example

	exampt	e_csr						
HW address	: 0x0							
C prefix:	CSR							
C offset:	0x0							
31	30	29	28	27	26	25	24	
			TYPE	[15:8]				
23	22	21	20	19	18	17	16	
			TYPE	E[7:0]				
15	14	13	12	11	10	9	8	
			RESER	VED[7:0]				
7	6		5	4	3	2	1	0
ED DED		EN OVO						
PCB_RE Binary co	ED_GRE V [read-only] ded PCB lay ES [read-onl	EN SYS_ : PCB revision out revision.		FMC_PRES		PCB_I	REV[3:0]	
 PCB_RE Binary co FMC_PR FMC s FMC s SYS_PLI Crottode Locked. LED_RE Manual co LED_RE Manual co 	LED_GRE V [read-only] ded PCB lay ES [read-onl lot is populat lot is not pop LCK [read/w bother [read/w pontrol of the f D [read/write] pontrol of the f	EN SYS_ : PCB revision out revision. y]: FMC prese ed ulated. -only]: System rite]: Green LI ront panel gree [: Red LED ront panel rec	PLL_LCK n ence n clock PLL sta ED een LED (unused	EMC_PRES atus sed in the fmc-adc I in the fmc-adc ap	application)	PCB_1	REV[3:0]	

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Testing environment

Production test systems

- Performs automated production tests.
- Includes a software framework to run the tests (Python).



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Future	work				

Consolidate our designs

- Consolidate documentation (starter guides, ...).
- Continue to tranfer knowledge to companies.

Facilitate sharing with FOSS EDA tools

- Tools are expensive and do not interoperate.
- Existing FOSS tools not usable for complex designs.
- We contribute to the development of FOSS tools:
 - Extension of **Icarus** Verilog simulator with VHDL and SystemVerilog support.
 - Enhancement of KiCAD (schematics & PCB editor).

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Conclu	sions					

- CERN's FMC kit is not only a set of hardware modules.
 - HDL cores, drivers, test systems, tools
- Eight CERN designs are already commercialized.
- Open Hardware has many advantages.
 - Make better designs: peer review, user feedback
 - More collaborations inside and outside CERN
- OHR site is practical for engineers and is stimulating.
- New users and collaborations are welcome.
- Four years of experience show it works!

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Open products are real products[™]

Selections		322.2
Home Projects Services Products Compa		Design and Manufacturing
		2 SV F For technical
WR Switch (18/8 SFPs)	Horre News Products Exhibit	es References Support Contact
The White Rabbit Switch (WRS) is the key component precision timing and high synchronization over an Ethernet	Products by Standard + PMC + 4ck SIS Maps 30 Miler 14 bit ADC	
Actually it exists two standalone SFP versions:	4ch 105 Msps 30 MHz 14 bit ADC	58
The WRS-3/18 version which is the standard version The WRS-3/8 version with only 8 SFP connectors us	Features:	
Main Features	4 channel FMC ADC module Max, sample rate 105 Mass	
Virtee-6 FPGA (XC6VLX130T) ARH (Azmel AT915AH9645) @ 400HHz 18/8 : 55P capes 32M x 16 DDR2 Two 512x026 QDRII SRAM	Analag bandwardt 30 Meil, DC coupled Bhylwengin 4 Mit DNOO LL, 11.5, 11.7 bit (0 +/-50mit, +/-6.5%, +/-57 arage) Channels 4 Carlentotes 4 x LEMO 00 for signals, 1 x LEMO 00 for trigger byget signalence 1 ADMn / 50 Ohn - software	
Ethernet 10/100 PHY 255 PH Bhard Flash BHS PI Boot Flash SHC coasial Clocks (PPS I/O, 125Mbz I/O, 10Mbz 1.6 Glav VCG (APS16-4)		
References		4
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Want to know more? Take a tour on ohwr.org

Matthieu Cattin

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