An Upgraded ATLAS Central Trigger for 2015 LHC Luminosities

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CERN

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Outline

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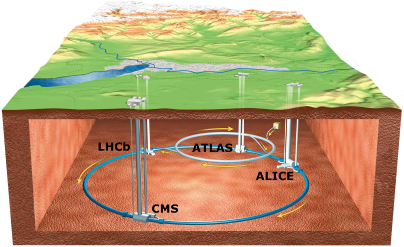
The ATLAS experiment at CERN's Large Hadron Collider

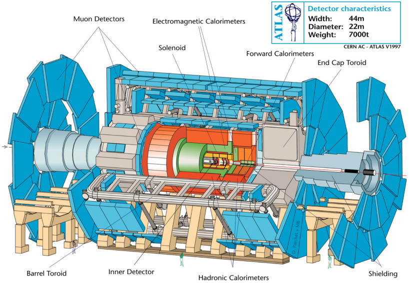


The ATLAS experiment

- General-purpose detector: from precision SM measurements to Higgs and BSM searches
- Interested mainly in rare processes $\Rightarrow$ need to select most interesting collision events $\Rightarrow$ trigger system

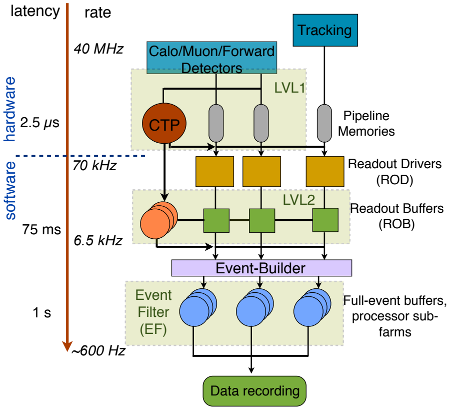
The Large Hadron Collider (LHC)

- Collides protons (and/or Pb ions) at 40 MHz in a 27-km tunnel
- Run I: 2010-2012:
  - $\sqrt{s} = $ 7-8 TeV (pp)
  - $\mathcal{L} \sim 10^{33}$ cm^{-2}s^{-1}
- Run II starting in 2015:
  - $\sqrt{s}$ for pp: 13-14 TeV
  - $\mathcal{L} \gtrsim 10^{34}$ cm^{-2}s^{-1}



The trigger and data acquisition system in ATLAS

The trigger system decides what collision events are saved for offline analysis!



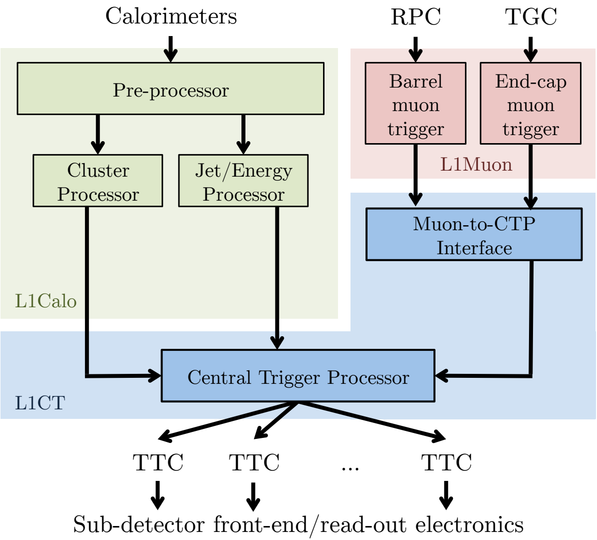
Typical rates for Run I above. Expected in Run II: 100 kHz L1, 1 kHz HLT.

Three levels sequentially refine selection

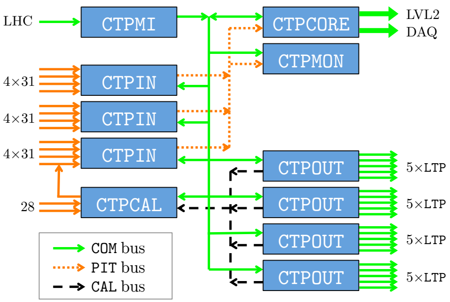
- Level 1 hardware-based, custom electronics modules
  - Synchronized with LHC collisions
  - Reduced-granularity detector data
  - Sends Region-of-Interest (RoI) info to Level 2
- High-Level Trigger (HLT) software-based, runs on PC farm
  - Level 2 uses full-granularity data in RoIs
  - Event Filter uses more sophisticated reconstruction algorithms and full event information

Outline

Overview of the Level-1 Trigger



The Central Trigger Processor (CTP)



Modules (VME, 6U/9U)

- CTPMI: Machine Interface
- CTPIN: Input module
- CTPCORE: Core module
- CTPOUT: Output module
- CTPMON: Monitoring module
- CTPCAL: Calibration module

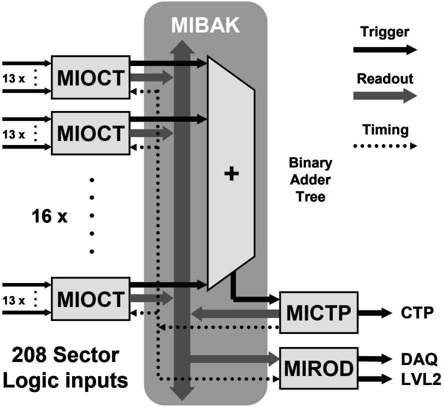
CTP backplanes

- Common (COM): timing and trigger
- Pattern-In-Time (PIT): trigger inputs
- Calibration requests (CAL)

What does the CTP do?

- Receives LHC timing signals and trigger inputs, generates L1 Accept (L1A)
- Sends summary info to L2 & DAQ, and timing signals and L1A to sub-detectors
- Generates dead time to protect sub-detector read-out electronics

The Muon-to-CTP Interface (MUCTPI)



What does the MUCTPI do?

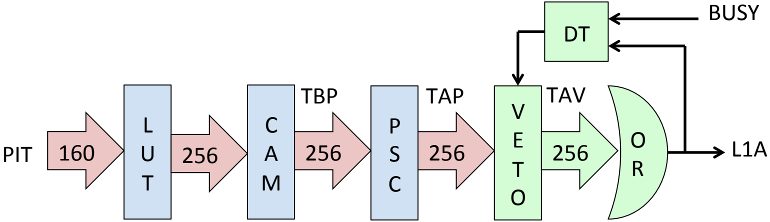
- Summarizes candidates found by muon trigger detector electronics
- Removes double candidates reported by overlapping sectors
- Reports candidate multiplicities for six programmable p_{T} thresholds to the CTP

Three types of modules communicate via the MIBAK backplane:

- MICTP: communicates with the CTP
- MIROD: handles read-out, communicates with data acquisition and Level-2 trigger systems
- MIOCT: processes signals from the muon trigger detectors in each octant

Outline

Motivation for upgrade: CTP resources

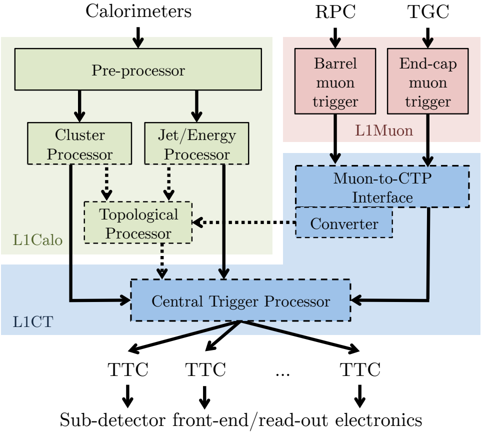


- 160 selected CTPIN signals via PIT bus
- Look-up tables and content-addressable memories form *items* from logical combinations of inputs
- Pre-scales: allows selecting 1 of n triggers, applied per item
- Veto: caused by dead time to protect busy read-out electronics

During a typical run in 2012:

Feature	**Used**	**Available**
CTPIN input cables	9	12
PIT bus lines	160	160
CTPCORE trigger items	241	256
CTPCORE bunch groups	8	8
CTPCORE front inputs	0	0
Max # bits in OR	6	12
Per-bunch item counters	12	12
Output cables to TTC	20	20

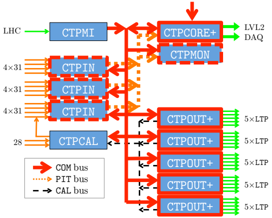
Motivation for upgrade: topological algorithms at Level 1



- Same L1A rate at higher luminosities ⇒ more intelligent selection
  ⇒ exploit difference in event topology for signal and background
- Requires modifications of the CTP and MUCTPI systems

Hardware upgrade of the CTP

- Upgraded COM backplane to allow multiple partitions and a fifth CTPOUT+ (and PIT operated with DDR)
- Redesigned core module, CTPCORE+ ⇒
  - Increased inputs, items and monitoring resources
  - 192 optical/low-latency electrical front-panel inputs
  - Up to three simultaneous L1A partitions (useful e.g. for concurrent commissioning and calibration runs)
- New CTPOUT+: supports multiple partitions and per-bunch monitoring
- Firmware upgrades to CTPIN and CTPMON modules

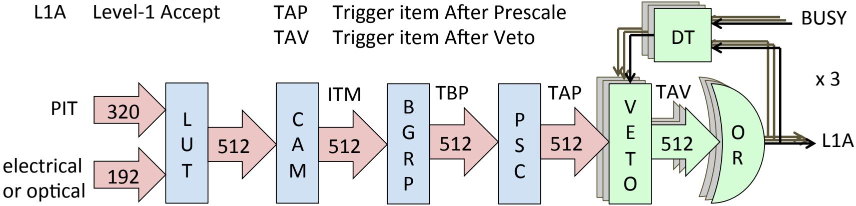


(thick lines highlight changes, dashed for firmware-only)

Feature	Used (2012)	Available	Upgrade
CTPIN input cables	9	12	12
PIT bus lines	160	160	320
CTPCORE trigger items	241	256	512
CTPCORE bunch groups	8	8	16
CTPCORE front inputs	0	0	192
Max # bits in OR	6	12	15
Per-bunch item counters	12	12	256
Output cables to TTC	20	20	25

Trigger path in post-LS1 CTP & parallel partitions

LUT	Look-Up Tables	CAM	Content Addressable Memory
BGRP	Bunch GRouP	PSC	PreSCaling
DT	DeadTime	PIT	Pattern In Time
ITM	Trigger ITeM	TBP	Trigger item Before Prescale
L1A	Level-1 Accept	TAP	Trigger item After Prescale
		TAV	Trigger item After Veto

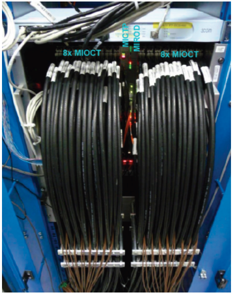


- One primary “physics” partition
- Up to two secondary partitions for parallel calibration and commissioning runs
- Trigger menu shared by all partitions, in each partition only a sub-set of items yield a L1A, and dead-time generation is treated separately
- Only the primary partition sends information to DAQ/Level-2

Firmware upgrade of the MUCTPI

Provide new topological processor with muon candidate information:

- MIOCT firmware upgrade (and new electrical-to-optical converter board)
  $\Rightarrow$ 8x over-clocking two local electrical outputs
  $\Rightarrow$ 16 bits per octant board (256 bits per event)
- How should these bits be used? What physics processes depend on topological triggers involving muons at Level 1? E.g. B-physics ($B_s \to \mu^+\mu^-$), LFV τ decays ($\tau \to 3\mu$, $\tau \to 3\mu\gamma$), ...
- Limited logic resources left in FPGAs of existing MIOCT module $\Rightarrow$ keep it simple



Will send info about up to two muon candidates per octant:

0	1	1	1	0	0	1	0	0	1	0	1	1	1	0	1
η			ϕ			p_{T}		η			ϕ			p_{T}	
Candidate 1								Candidate 2							

$\Rightarrow$ angular resolution $\Delta\eta \times \Delta\phi \sim 0.35 \times 0.1$, three p_{T} thresholds

Outline

Summary & conclusions

Central Trigger Processor (CTP) system

- New CTPCORE+ and CTPOUT+ modules and COM bus, PIT bus at DDR
  - more resources in terms of trigger inputs and monitoring, etc.
  - new features, most importantly the capability to run several parallel L1A partitions

Muon-to-CTP Interface (MUCTPI) system

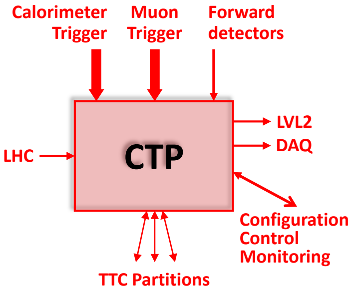
- Hardware of MUCTPI remains unchanged in Long Shutdown 1
- Firmware upgrade of MIOCT module allows sending reduced granularity muon data to topological trigger processor (complete MUCTPI redesign for Phase-I Upgrade in 2018, providing full-granularity data)

Outlook

- On schedule to start commissioning from mid-2014
- Lots of work on testing of hardware and developing firmware and software for the upgraded systems

Back-up slides

Functionality of current CTP system



Trigger:

- Combine triggers from L1Calo, L1Muon (via MuCTPI) & other detectors
- Flexible logical combinations defined in trigger menu
- BG masking, pre-scaling, deadtime generation
- Generate L1A and trigger-type word

Timing:

- Receive bunch clock and orbit signals from LHC
- Add L1A, trigger-type word and event-counter reset (ECR)
- Distribute to TTC partitions, receive busy and calibration requests

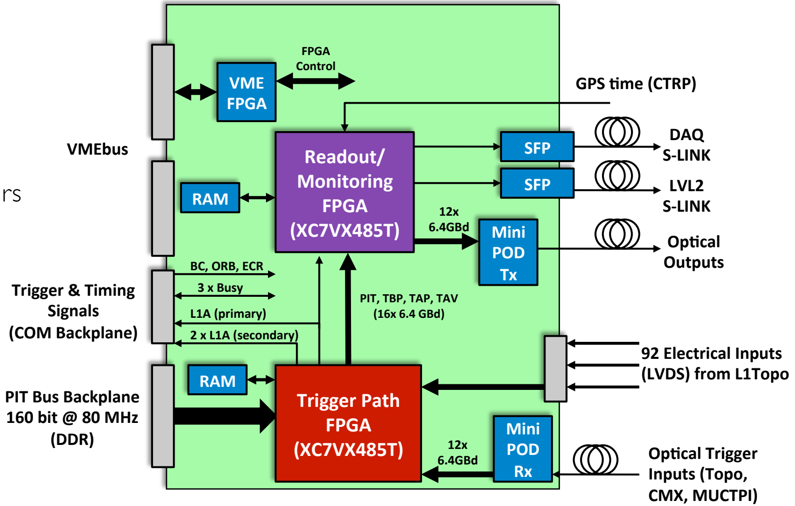
Read-out:

- Send RoI to L2 and read-out data to DAQ

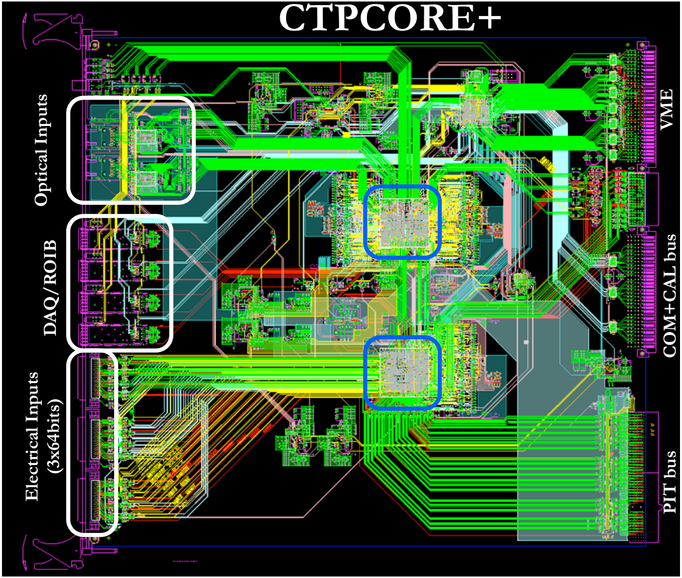
Control:

- Configuration stored in trigger and

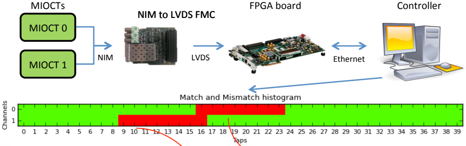
Design of the new CTPCORE+ module



Layout of the new CTPCORE+ module

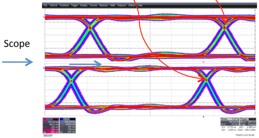


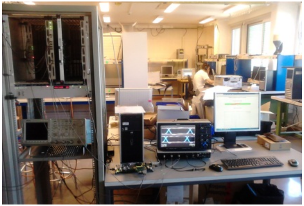
Tests of over-clocking of MIOCT modules



Bit Pattern:
STABLE
UNSTABLE

Data rate: 320Mb/s
PRBS length: 2^{31} - 1

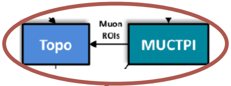




- Initial tests results: zero errors during 24 hours for phases marked in green, suggesting bit-error rate $< 10^{-12}$
- Shows that 8x over-clocking, i.e. running at 320 MHz, is possible

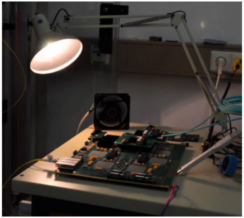
The MuCTPiToTopo electrical-to-optical converter board

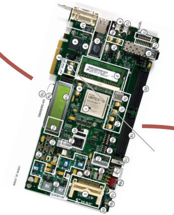
Details in:
ATL-DAQ-INT-2012-003
O.Igonkina, J.Vermeulen



32 LEMO cables from MuCTPi

Prototype of L1Topo





FPGA development kit

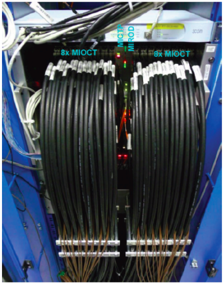


Figure 2: The final MUCTPI as it is installed in the ATLAS experiment.

Can deliver 256 bits from MuCTPi per event to L1Topo

What's the best way of using this information?

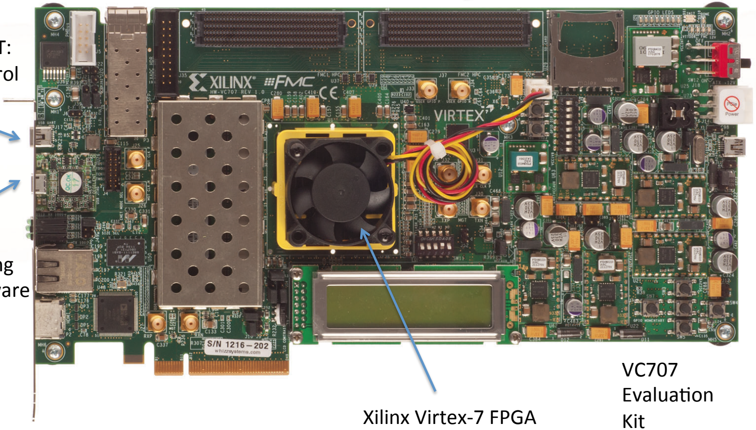
The MuCTPiToTopo electrical-to-optical converter board

FMC board with LEMO connectors goes here

FMC board with 2 QSFP+ transceivers goes here

USB i/f to UART: -> control

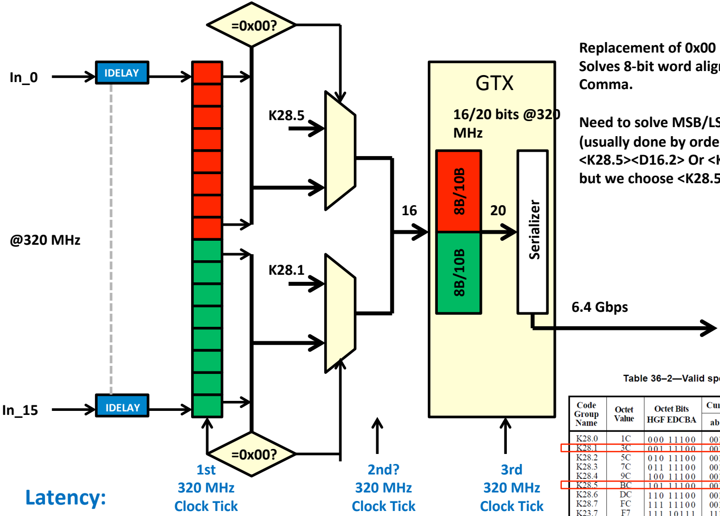
USB JTAG i/f -> loading of firmware



Xilinx Virtex-7 FPGA

VC707 Evaluation Kit

The MuCTPiToTopo electrical-to-optical converter board



Replacement of 0x00 into <K28.5> / <K28.1> Solves 8-bit word alignment. Both contain Comma.

Need to solve MSB/LSB alignment at Topo (usually done by ordered set <K28.5><D16.2> Or <K28.5><D5.6> but we choose <K28.5><K28.1>)

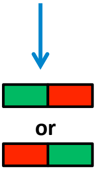


Table 36–2—Valid special code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD – abcdei fghj	Current RD + abcdei fghj	Notes
K28.0	1C	000 11100	001111 0100	110000 1011	1
K28.1	3C	001 11100	001111 1001	110000 0110	1,2
K28.2	5C	010 11100	001111 0101	110000 1010	1
K28.3	7C	011 11100	001111 0011	110000 1100	1
K28.4	9C	100 11100	001111 0010	110000 1101	1
K28.5	BC	101 11100	001111 1010	110000 0101	2
K28.6	DC	110 11100	001111 0110	110000 1001	1
K28.7	FC	111 11100	001111 1000	110000 0111	1,2
K23.7	F7	111 10111	111010 1000	000101 0111	
K27.7	FB	111 11011	110110 1000	001001 0111	
K29.7	FD	111 11101	101110 1000	010001 0111	
K30.7	FE	111 11110	011110 1000	100001 0111	

NOTE 1—Reserved.

NOTE 2—Contains a comma.