Migration from WorldFIP to a Low-Cost Ethernet Fieldbus for Power Converter Control at CERN

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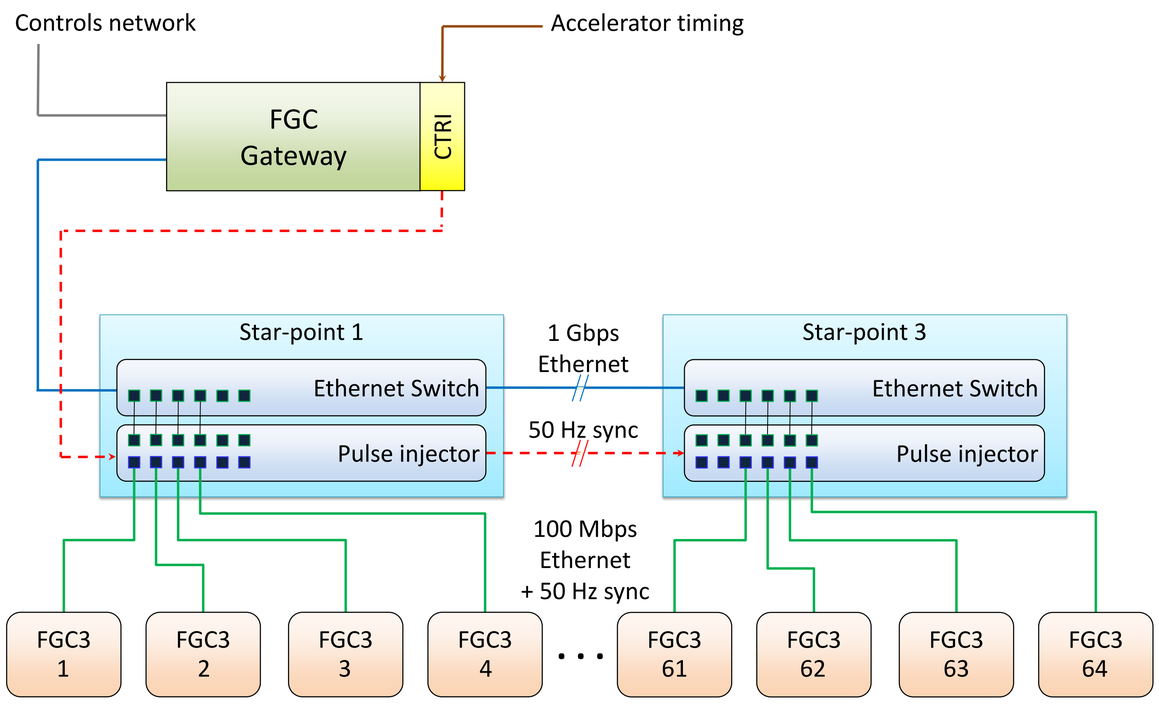
Introduction

Power converter control in the LHC uses embedded computers called Function Generator/Controllers (FGCs) which are connected to WorldFIP fieldbuses around the accelerator ring. The FGCs are integrated into the accelerator control system by x86 gateway front-end systems running Linux. With the LHC now operational, attention has turned to the renovation of older control systems as well as a new installation for Linac 4. A new generation of FGC is being deployed to meet the needs of these cycling accelerators. As WorldFIP is very limited in data rate and is unlikely to undergo further development, it was decided to base future installations upon an Ethernet fieldbus with standard switches and interface chipsets in both the FGCs and gateways. The FGC communications protocol that runs over WorldFIP in the LHC was adapted to work over raw Ethernet, with the aim to have a simple solution that will easily allow the same devices to operate with either type of interface.

FGC_Ether Architecture



A gateway computer includes a CERN-designed CTRI timing receiver, which is configured to provide interrupts for the software and the 50 Hz sync signal for the FGCs. This is transmitted on a coax cable in parallel with the 1 Gbps Ethernet backbone that links the gateway to the switches. Each switch is mounted above a pulse injector to form a star point supporting up to 22 FGCs. Up to 64 FGCs can be connected to one FGC_Ether fieldbus, requiring a minimum of three star points. More than three can be used if the geographical distribution of converters favours such a topology.

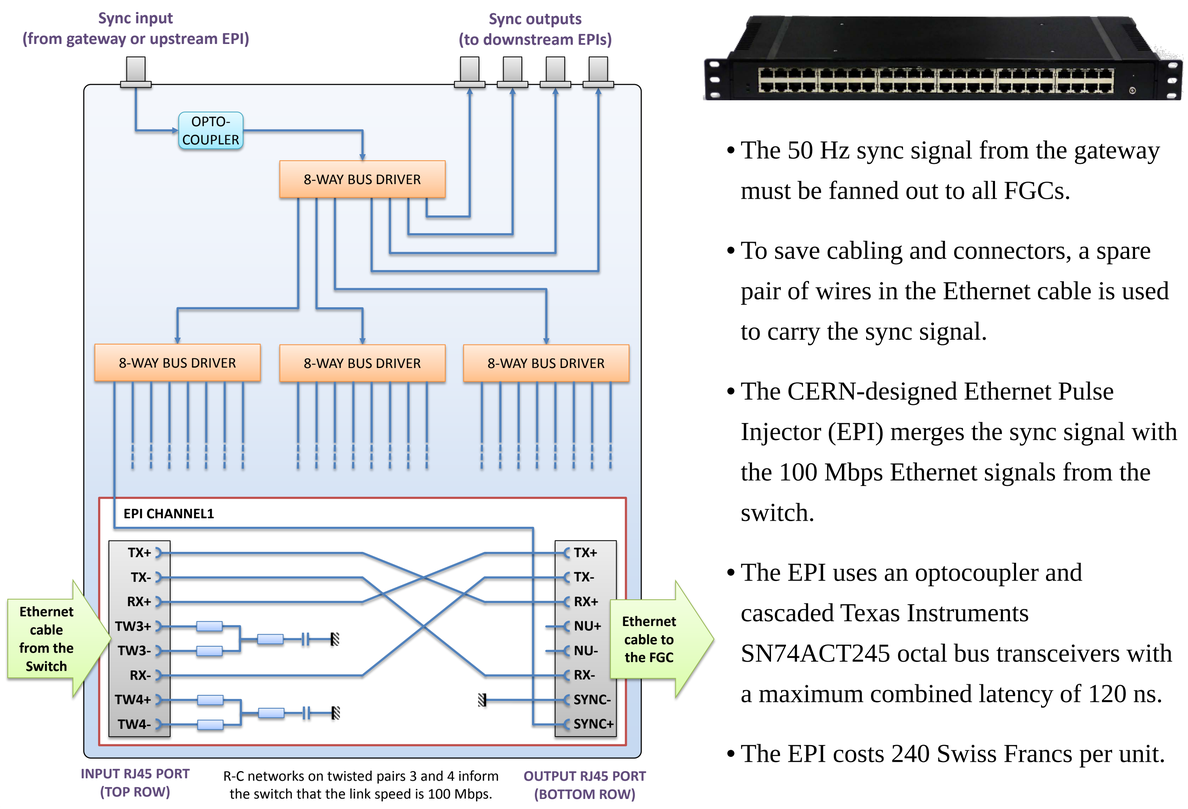
Gateway Computer

- Kontron PCI760 2U industrial PC.
- CERN-designed CTRI PCI timing receiver.
- 64-bit Scientific Linux CERN 6 (SLC6) operating system.
- MRG real-time kernel.
- Function Generator/Controller Daemon (FGCD) software framework.

FGC3

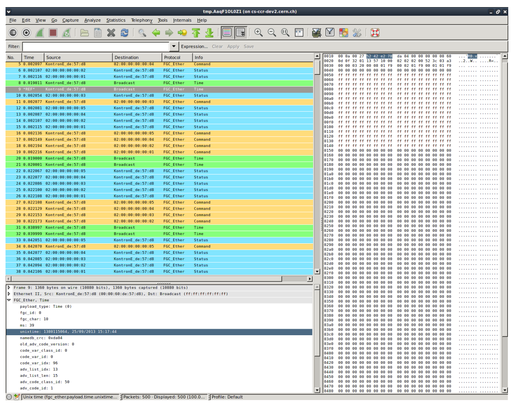
- CERN-designed power converter Function Generator / Controller.
- Renesas RX610 100 MHz microcontroller.
- Texas Instruments TMS320C6727 300 MHz DSP.
- 65 MB RAM, 2 MB flash, 512 KB MRAM.
- SMSC LAN9221 100 Mbps LAN controller.

Ethernet Pulse Injector (EPI)



- The 50 Hz sync signal from the gateway must be fanned out to all FGCs.
- To save cabling and connectors, a spare pair of wires in the Ethernet cable is used to carry the sync signal.
- The CERN-designed Ethernet Pulse Injector (EPI) merges the sync signal with the 100 Mbps Ethernet signals from the switch.
- The EPI uses an optocoupler and cascaded Texas Instruments SN74ACT245 octal bus transceivers with a maximum combined latency of 120 ns.
- The EPI costs 240 Swiss Francs per unit.

Diagnostic Tools



- Tcpdump captures frames on the gateway computer.
- The Wireshark network protocol analyser is used for traffic analysis.
- A CERN-written Wireshark plugin for FGC_Ether decodes all frames.
- A script provides integration with the power converter expert application allowing filtering of data at the time of capture.
- Frames can be captured remotely from any fieldbus while it is in operation.

Ethernet Switch

- Cisco SF 102-24 standard Ethernet switch.
- Unmanaged.
- Two 1 Gbps ports.
- Twenty four 100 Mbps ports.

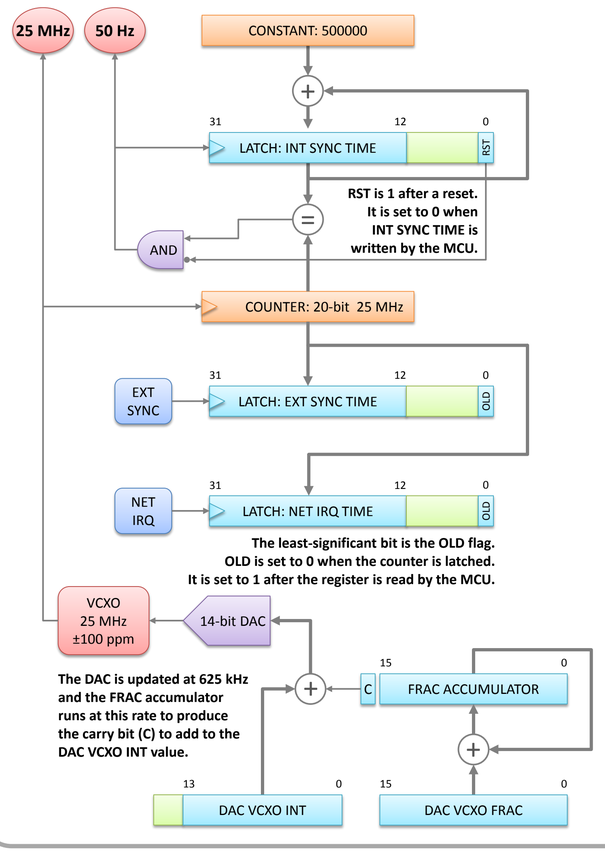
Addressing

- The fieldbus address for each circuit is encoded within a dongle with a DE-9 connector, plugged into the front of each FGC.
- For power converters with replaceable modules, the dongle is fixed to the Ethernet cable.
- For power converters with operational spares, the dongle can be moved to the FGC in the spare converter so that it can assume the correct identity within the control system.

Star-Point

- An FGC_Ether star-point consists of a switch and an Ethernet Pulse Injector.
- Up to 22 FGCs can be connected to each star-point, so a minimum of 3 star points are required for a fully populated bus of 64 FGCs.

Phase-Locked Loop (PLL)



- Power converter controls require a low-jitter synchronised clock in the FGC with 1µs accuracy in the worst case (1 ms is often sufficient).
- This is generated with a 25 MHz voltage-controlled crystal oscillator (VCXO) driven by an over-sampled 14-bit DAC (more than 18-bit effective resolution).
- The DAC is set by a traditional proportional-integral PLL algorithm running in the MCU at 5 Hz using floating-point calculations.
- The PLL is normally disciplined by the external 50 Hz sync pulse (EXT SYNC), received on the spare pair in the Ethernet cable. This has a jitter of much less than one 40 ns clock period.
- If this is not available then the PLL can be disciplined by network interrupts (NET IRQ) for the time packets broadcast by the gateway, however the jitter can be up to 20 µs.
- This provides a useful degraded operating mode.

Conclusions

Early experience from operational use of FGC_Ether is encouraging. Up to 3000 nodes are expected to be deployed over the next decade, so the fact that FGC_Ether is based upon standard low-cost COTS components will provide significant savings and provide security against component obsolescence.
The compatibility with the FGC protocols used with WorldFIP allowed significant code reuse, accelerating development and reducing maintenance costs for the future.