Control, Safety, and Diagnostics for future ATLAS Pixel Detectors

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The ATLAS Pixel detector completed successfully the data-taking period during run 1 of the LHC. To ensure its excellent performance during next run periods with increasing demands two upgrades of the Pixel detector are foreseen. One takes place in the first long shutdown of the LHC, which is currently on-going: an additional most inner layer will be installed, the Insertable B-Layer (IBL). The second upgrade will replace the entire inner detector of the ATLAS experiment by the Inner Tracker (ITK) and is planned for 2020, when the LHC will be upgraded to HL-LHC. We present a concept for the control of the pixel detector at the HL-LHC. While this requires completely new strategies, the control system of the IBL includes only single new components, which can further be developed for the long-term upgrade.

Requirements

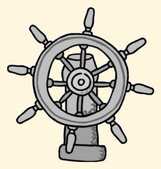
Tasks:
- Ensure the safety of the detector at all times
- Provide the operator with tools for operation
- Provide the expert with additional information to debug the detector and DCS

Design constraints:
- High power density inside the tracker volume
- Reduce material inside the tracker volume
- Radiation hardness of components inside the tracker volume
- no access after the installation

DCS subjects:
- Detector modules (sensor and frontend chips)
- opto-electrical transceivers
- further on- and off-detector electronics
- detector environment

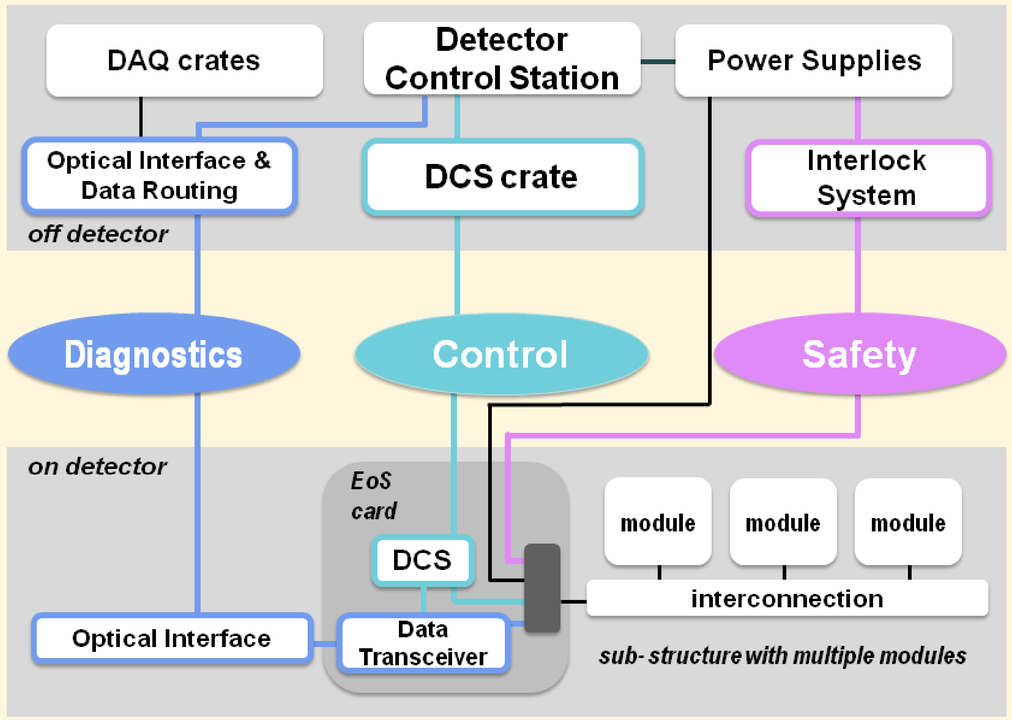
DCS concept: three independent paths

Diagnostics
- On request
- fine segmentation
- Merged into DAQ data stream

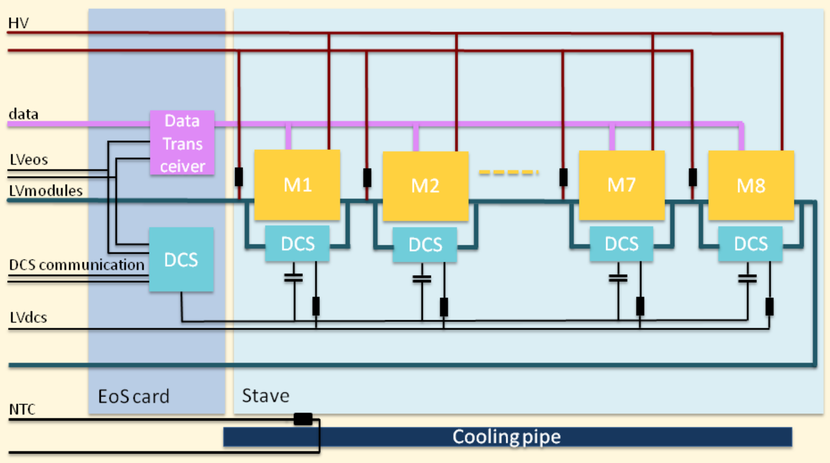


Control & Feedback
- For all use cases
- High reliability
- Steering and monitoring of modules, EoS card, optical interface

Safety
- Permanent availability
- Highest reliability
- Hardwired interlock system

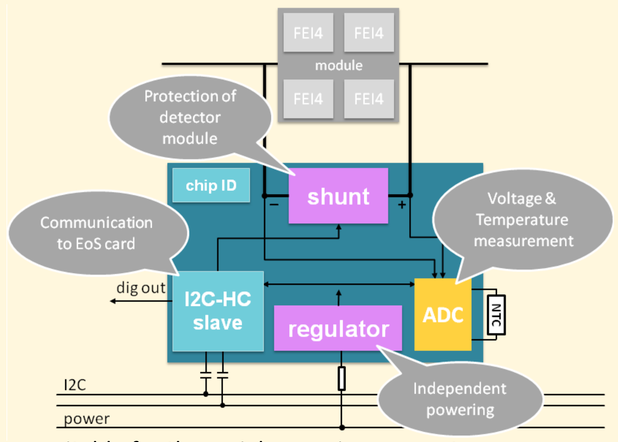


Serial Powering for ITK



- modules of one support structure (half stave) share one low voltage line
- serial powering reduces services significantly
- requires a local control to disable individual modules

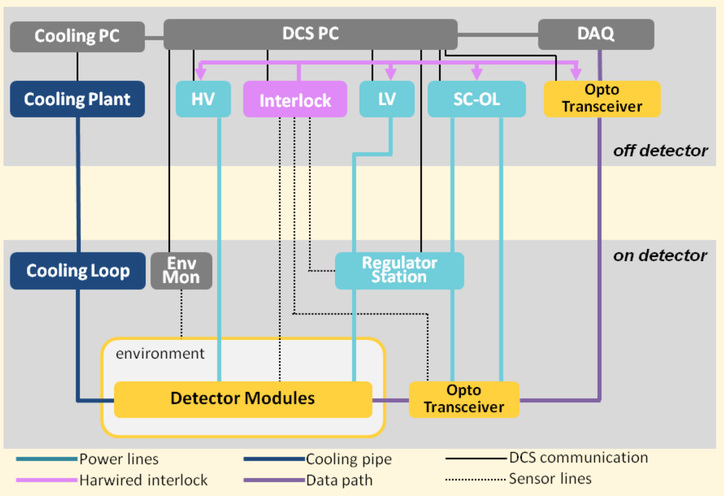
DCS chip



- suitable for the serial powering concept
- protection and control of modules
- local measurements

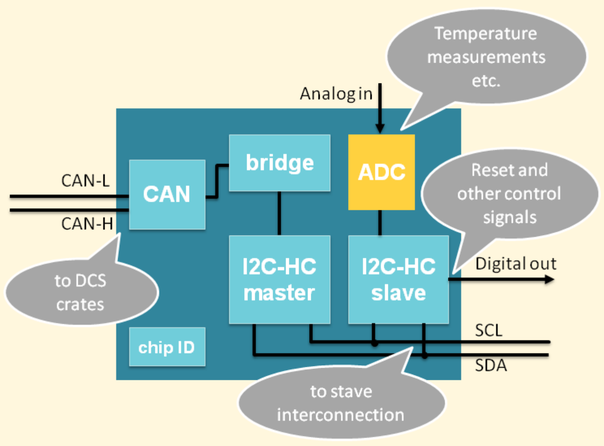
Status:
- communication via modified I2C-bus (Hamming protected) implemented and tested
- ADC from FEI4 and shunt from SPP
  - details see conference proceedings TUPPCO50
- to be submitted in 130 nm CMOS

IBL DCS Overview



- Main components: power supplies, monitoring units, CO_2 evaporative cooling, interlock system
- Production of hardware ongoing
- Installation beginning of 2014

DCS controller

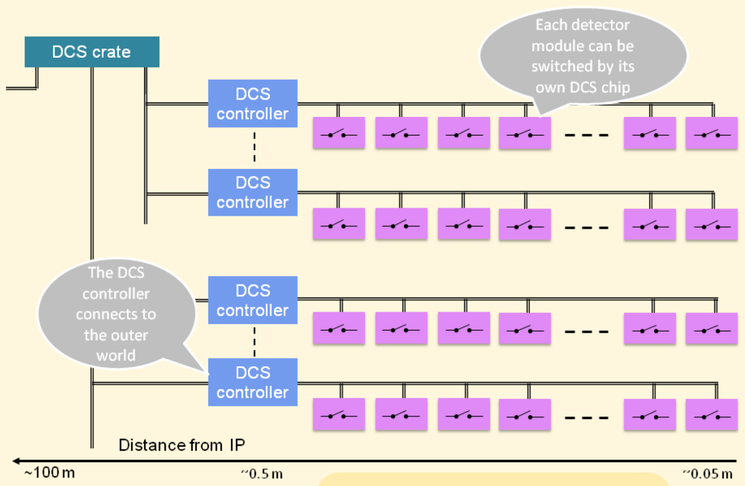


- CAN node
- Master of DCS chip interface
- Bridge between both interfaces (CAN and I2C-HC)
- Triple Modular Redundancy

Status:
- prototypes developed in 130 nm CMOS
- communication tests and
- first irradiation tests performed

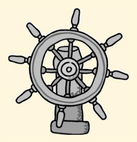
DCS network for ITK

DCS chip and DCS controller are the main ingredients to realize the control and feedback path for the pixel ITK



common design constraints
- Reduction of services
- Radiation hardness
- High reliability

Diagnostics, Control & Safety for IBL



Control
- Mainly on the level of the power supplies
- Parallel services allow for control of individual modules
- Regulator station protects against transients and steers individual modules

Safety
- Hardwired interlock system
- Protection against heat-ups

Diagnostics
- FEI4 contains ADC
- ADC measures temperature, leakage current, voltages of FEI4 Data are sent via data path

under development:
- off-detector decoder extracts DCS data
- OPC-UA server on DCS as receiver