EVALUATION AND IMPLEMENTATION OF ADVANCED PROCESS CONTROL WITH COMPACTCRIO MATERIAL

PH-DT Detector Technologies

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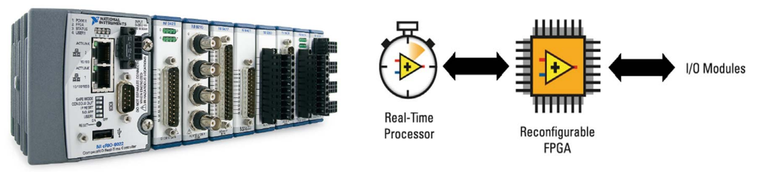
MOTIVATION & STUDY

Programmable Logic Controller (PLC) is commonly used in industries and research applications for process control. However a very complex process control may require algorithms and performances beyond the capability of PLC's, very high-speed or precision controls may also require other solutions.

cRIO has been used at CERN in a recent research conducted to implement advanced process controls (decoupling of Muti Input Multi Output process control, steady state feedback, Kalman filter) with the compactRIO (cRIO) material from National Instruments.

Compact RIO

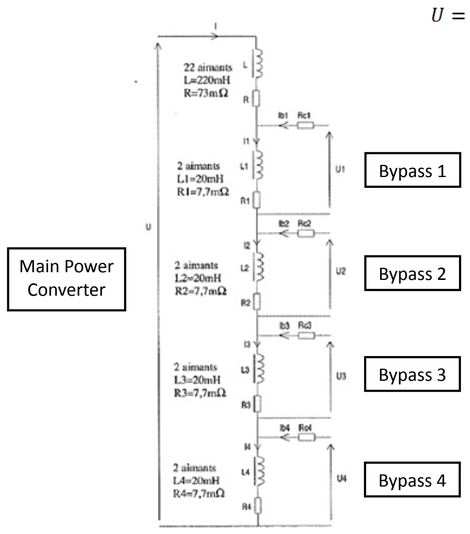
cRIO is a reconfigurable embedded control and acquisition system developed by National Instruments, integrating a real-time controller, a reconfigurable FPGA and I/O modules. The real-time controller consists of a powerful processor for performing autonomous and deterministic applications. The FPGA is a programmable logic circuit, comparable to the hardwired logic.



MULTIPLE INPUT MULTIPLE OUTPUT

Performance assessment of the cRIO for advanced control systems: the CERN SPS beam transfer lines (several magnets in series supplied by one power converter and correction by bypass).

PROCESS



PROCESS MODEL

$$U = L\frac{dI}{dt} + RI + L_1\frac{dI_1}{dt} + R_1I_1 + L_2\frac{dI_2}{dt} + R_2I_2 + L_3\frac{dI_3}{dt} + R_3I_3 + L_4\frac{dI_4}{dt} + R_4I_4$$

$$U_1 = L_1\frac{dI_1}{dt} + R_1I_1 + R_{C1}(I_1 - I) \qquad I_{b1} = I_1 - I$$
$$U_2 = L_2\frac{dI_2}{dt} + R_2I_2 + R_{C2}(I_2 - I) \qquad I_{b2} = I_2 - I$$
$$U_3 = L_3\frac{dI_3}{dt} + R_3I_3 + R_{C3}(I_3 - I) \qquad I_{b3} = I_3 - I$$
$$U_4 = L_4\frac{dI_4}{dt} + R_4I_4 + R_{C4}(I_4 - I) \qquad I_{b4} = I_4 - I$$

STATE-SPACE MODEL

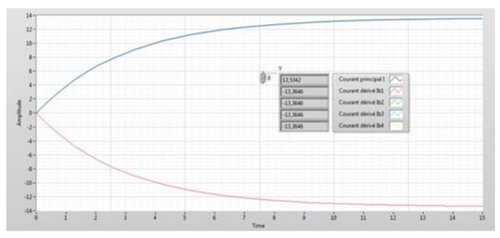
$$\dot{x}(t) = Ax(t) + Bu(t)$$
$$y(t) = Cx(t) + Du(t)$$

$$\begin{bmatrix} \frac{dI}{dt} \\ \frac{dI_1}{dt} \\ \frac{dI_2}{dt} \\ \frac{dI_3}{dt} \\ \frac{dI_4}{dt} \end{bmatrix} = \begin{bmatrix} \frac{(-R-R_{C1}-R_{C2}-R_{C3}-R_{C4}}{L} & \frac{R_{C1}}{L} & \frac{R_{C2}}{L} & \frac{R_{C3}}{L} & \frac{R_{C4}}{L} \\ \frac{R_{C1}}{L_1} & \frac{(-R_{C1}-R_1)}{L_1} & 0 & 0 & 0 \\ \frac{R_{C2}}{L_2} & 0 & \frac{(-R_{C2}-R_2)}{L_2} & 0 & 0 \\ \frac{R_{C3}}{L_3} & 0 & 0 & \frac{(-R_{C3}-R_3)}{L_3} & 0 \\ \frac{R_{C4}}{L_4} & 0 & 0 & 0 & \frac{(-R_{C4}-R_4)}{L_4} \end{bmatrix} \begin{bmatrix} I \\ I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} & -\frac{1}{L} & -\frac{1}{L} & -\frac{1}{L} \\ 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_3} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_4} \end{bmatrix} \begin{bmatrix} U \\ U_1 \\ U_2 \\ U_3 \\ U_4 \end{bmatrix}$$

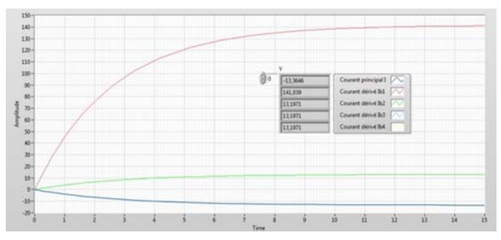
$$\begin{bmatrix} I \\ I_{b1} \\ I_{b2} \\ I_{b3} \\ I_{b4} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 \\ -1 & 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 \\ -1 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I \\ I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}$$

PROCESS SIMULATION

Step response of the main power converter



Step response of the bypass 1



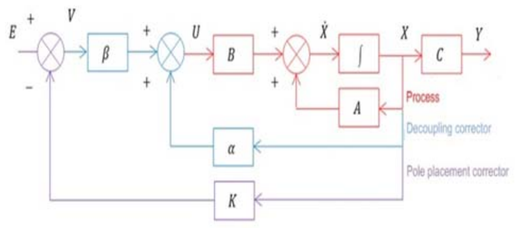
The MIMO process is coupled, the step response to an input affects all outputs.

MIMO DECOUPLING & POLE PLACEMENT CORRECTOR

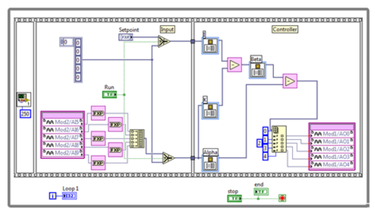
The goal of decoupling corrector is to limit the response of an input to an output with the state feedback $U - \beta V + \alpha X$

In order to adjust the dynamic in close loop by pole placement, we add an additional corrector with the state feedback $V = E - KX$

Process, decoupling corrector and pole placement feedback

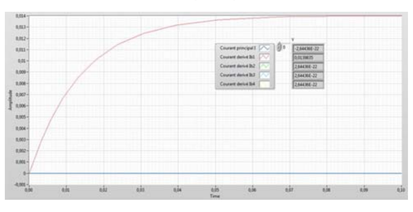


Corrector implementation in the FPGA



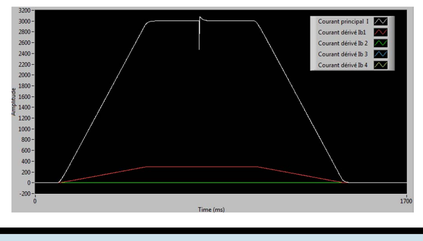
RESULTS

Step response



With the advanced process control (MIMO decoupling), the inputs are decoupled of the outputs and the process reacts as several independent subsystems. The dynamic of each subsystem can be adjusted (here with pole at -70, time constant is 14ms).

Robustness



The robustness of the system is also insured, a perturbation on an output does not affects other subsystems.

The acquisition time of the I/O modules and the treatment for the MIMO advanced control is 10µs.

KALMAN FILTER

To study and evaluate the performance of the cRIO FPGA for signal processing, it is necessary to implement more complex algorithms.

KALMAN FILTER THEORY

The Kalman filter is a powerful and useful mathematical tool in the embedded system. It allows to estimate the state of a system, depending on its previous state, controls applied and noisy measurement.

Equations of a discrete Kalman filter are divided into two stages (prediction and correction):

Step of prediction

$$\hat{x}_{k+1/k} = A_k\hat{x}_{k/k} + B_ku_k$$
$$P_{k+1/k} = A_kP_{k/k}{A_k}^T + G_kQ_k{G_k}^T$$

Step of correction

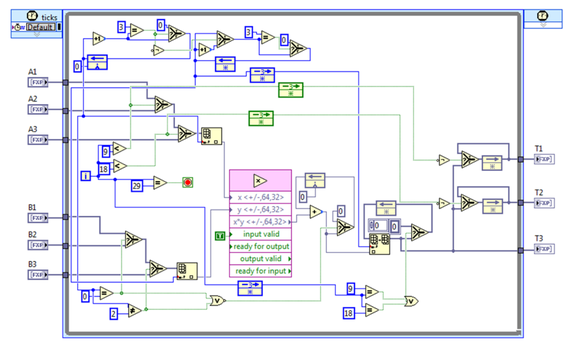
$$\hat{x}_{k/k} = \hat{x}_{k/k-1} + K_k(y_k - C_k\hat{x}_{k/k-1})$$
$$P_{k/k} = (I - K_kC_k)P_{k/k-1}$$

And K_k is the optimal gain of the filter $\quad K_k = P_{k/k-1}{C_k}^T\left(C_kP_{k/k-1}{C_k}^T + R_k\right)^{-1}$

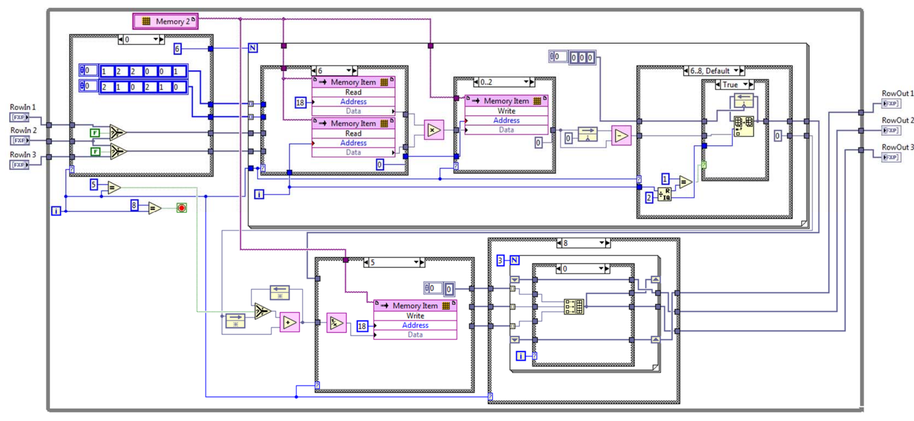
$\hat{x}$ is the estimation of the state correction
P is the estimation error
G_k is the matrix specifying the noise vector involved in the model of evolution
H_k is the matrix specifying the noise vector involved in the model of observation

KALMAN FILTER IMPLEMENTATION

The toolbox of FPGA LabVIEW provides a single tool to multiply a matrix with constant coefficients with a vector. For Kalman filter, it is necessary to perform matrix multiplication with variable coefficients with vector and also matrix multiplication by matrix (matrix being variable coefficients).



The calculation of the inverse matrix has been implemented in the FPGA with the Laplace formula $A^{-1} = \frac{1}{det\ A}{}^t com\ A$

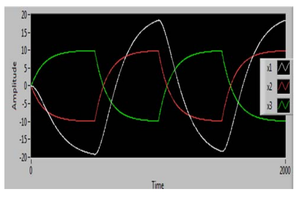


RESULTS

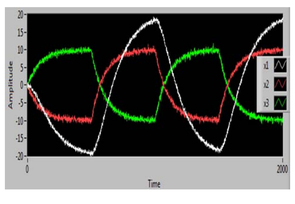
In order to test Kalman filter implemented in the FPGA, the test was realized on a process with the following state-space representation

$$\dot{X} = \begin{bmatrix} -1 & 1 & -1 \\ 0 & -1 & 0 \\ 0 & 1 & 0 \end{bmatrix}X + \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix}u \qquad Y = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}X$$

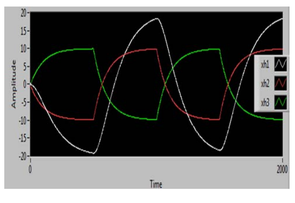
Process simulation



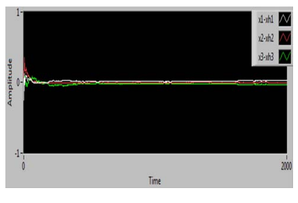
Noisy state



Estimated state with Kalman Filter



Error estimation



The algorithm performs in 2020 cycles, or 50µs with a clock rate of 40 MHz.

SUMMARY

The speed of the FPGA in the cRIO and the toolbox from Labview allows the implementation of complex calculations in order to achieve the advanced control process command and the signal processing.

The cRIO technology is a very good solution in comparison to the PLC for a fast and advanced control process, the computation time is about few 10µs against 20ms to 50ms for the PLC (depending on the complexity of the process and the number of I/O modules).