



Status of the TPS Timing System

C. Y. Wu*, Jenny Chen, Y. S. Cheng, K. T. Hsu

National Synchrotron Radiation Research Center, Hsinchu 30076, Taiwan



Abstract

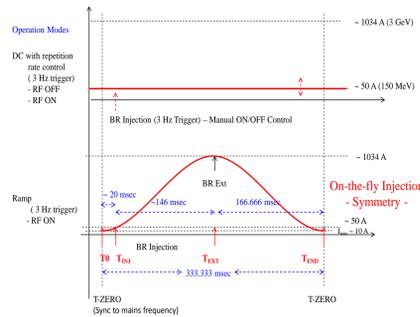
Implementation of timing system of the Taiwan Photon Source (TPS) is underway. Timing system provides synchronization for electron gun, modulators of linac, pulse magnet power supplies, booster power supply ramp trigger, bucket addressing of storage ring, diagnostic equipment, beamline gating signal for top-up injection, synchronize for the time-resolved experiments. The system is based on event distribution system that broadcasts the timing events over optic fibre network, and decodes and processes them at the timing event receivers. The system also supports uplink functionality which will be used for the fast interlock system to distribute signals like beam dump and post-mortem trigger with less than 5 msec response time. Software support is in preceded. Time sequencer to support various injection modes has been developed. Timing solutions for the TPS project will be summarized in the following paragraphs.

Event Based System for TPS Project

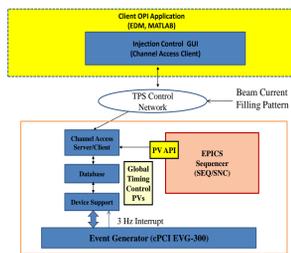
- The TPS timing system is an event based system.
- A central EVG generates events and are distributed over optic fiber links to multiple event receivers (EVRs) located in the control system interface layer, decoding the events referred to as hardware triggers or software interrupts.
- The event clock is derived from the 499.654 MHz master oscillator so that it is locked to the RF frequency.
- TPS timing modules with 6U CompactPCI form factor modules include cPCI-EVG-300, cPCI-EVR-300, cPCI-EVRTG-300 and linac gun trigger receiver.

Accelerator Timing

- The timing sequence control is based on state machine and used to manipulate several PVs to define the transition among different states and communication with the other IOCs.
- The TPS accelerators will be operated in 3 Hz repetition rate.
- The booster power supply could be operated in DC mode or ramping mode with on the fly injection.
- The on the fly injection mode provide flexibility for the booster tuning ramping performed just active ramp trigger as shown in the right figure.
- The sequence is started at T-ZERO which is the trigger time of the sequence RAM.
- Energy ramping time of the booster synchrotron is about 150 msec and there are more than 100 msec time window available for change contents of the sequence RAM.
- All parameters for the machine operation modes will be designed as specific EPICS PV.
- Timing sequencer structure is presented in the right figure.



Booster synchrotron power supply waveform plans.



Timing sequencer structure.

Sequence RAM Entry and Timestamp Management

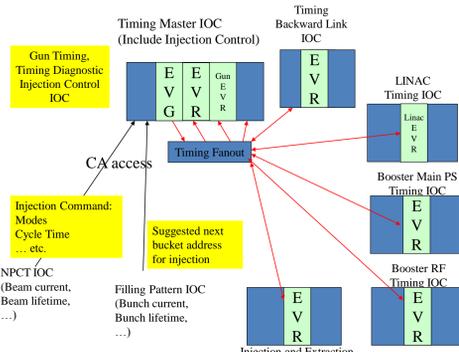
- All sequence will be stored at the sequence RAM. There is a timestamp associated each entry.
- The event can be active when load the desired timestamp. The event can be de-active and re-active by replace the event code.
- The timestamp value can be change for budget address requirements.
- The example of sequence RAM management is presented in the right figure.

Timestamp	Event Code	Timestamp	Event Code	Timestamp	Event Code
-----	-----	-----	-----	-----	-----
xxxxxxxx	0x21	xxxxxxxx	0x21	xxxxxxxx	0x21
xxxxxxxx	0x22	xxxxxxxx	0x20	xxxxxxxx	0x22
xxxxxxxx	0x23	xxxxxxxx	0x23	xxxxxxxx	0x23
-----	-----	-----	-----	-----	-----

Sequence RAM management.

Injection Control

- Injection control is the main theme of the timing system. Timing events related to the operation of all devices will be defined and associated to a timestamp.
- To provide bucket addressing, the timestamp of some trigger events should be adjusted cycle-by-cycle dynamically.
- The timing sequence is stored at the sequence RAM in the EVG.
- The RAM stop-interrupt of the EVG is enabled to wake up an EPICS sequencer.
- The relationship of injection control related IOCs is shown in the right figure.
- The linear accelerator and e-gun triggers will be connected to the timing master and installed at the equipment area (Control Instrument Area, CIA in TPS location name convention) above the linear accelerator system.



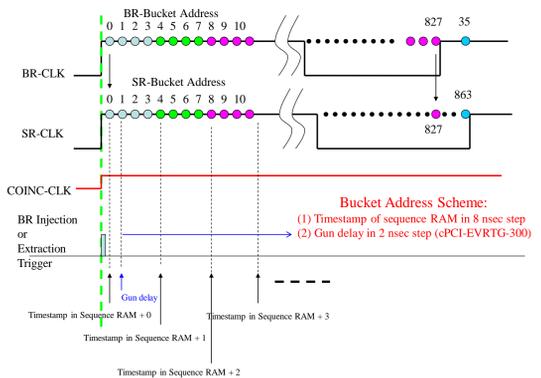
Relationship of injection control related IOCs.

Operation Mode

- The programmable sequence RAM provides a flexibility to change the operation mode.
- Basic operation will be ready for commissioning. Sophisticated modes may be delivered later.
- A simple configuration tool should be available for sequence RAM management. The operation modes may be:
 - Individual subsystem trigger enable/isable.
 - Single bunch and multi-bunch selection.
 - Continuous injection.
 - Repetitive rate decimation for specific trigger.
 - Warm up trigger before injection.
 - Top-up for desired filling pattern.
 - Top-up with filling pattern feedback.

Bucket Addressing

- The bucket addressing is performed by changing the value of timestamp in sequence RAM at every cycle. Bucket addressing scheme is shown in the right figure. The cPCI-EVRTG-300 provides the fine delay for gun trigger and digital delay generator for the storage ring injection kicker trigger with 2ns resolution.



Bucket addressing scheme for TPS.

Top-up injection with Bucket Addressing

- The top-up injection scheme might adopt multi-bunch mode to inject beam to desired target current, after reaching the target current the mode is switched into the single bunch mode. According to the filling pattern, the minimum bunch will be filled in next injection.

Filling Pattern Feedback

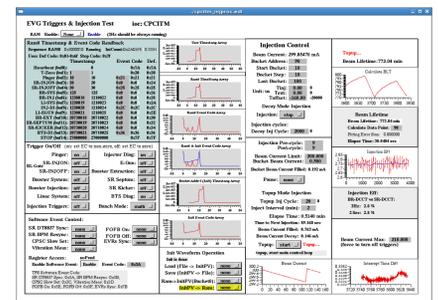
- In order to minimize filling pattern correlated orbit oscillations due to uneven bunch patterns, filling pattern control and/or feedback is planned to minimize bunch-to-bunch variation. Therefore there will be an EPICS sequencer running on the filling pattern IOC that measures bunch structure of storage ring and provides the next injection bucket address to timing master IOC via PV channel access.

Miscellaneous Considerations

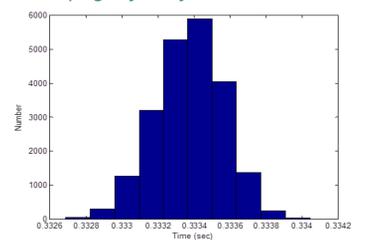
- Some devices might need a few cycles for warm-up before reaching stable working condition for beam injection, for example the injection septum of the storage ring. This is reported by several light sources. The timing sequencer can program the septum fire one or more cycles before real injection cycle take place. The booster power supplies may be the same. This mechanism may ensure accelerator working in a proper condition before injecting beam.

Implementation

- A few timing control related programs are developed by using state notation language (SNL) of the EPICS sequencer.
- The main timing control program provides continuous and top-up injection control.
- Another sequence program calculates the injection efficiency and beam lifetime.
- The beam current of booster and storage ring are averaged by a sequence program running on another IOC which connects booster DCCT and storage ring DCCT.
- The EDM page for injection control related programs testing is presented in the right figure.
- The time difference between consecutive sequence is shown in the right figure. Maximum jitter is about 1.5 ms peak-to-peak and the CPU loading of the EPUCS IOC is less than 20%.



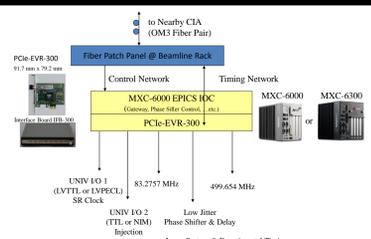
EDM pages for injection control test.



Histogram of time difference between consecutive sequence.

Timing for Beamline Users

- Time resolved experiments need machine revolution clock or its sub-harmonics or harmonics to synchronize synchrotron light pulse produced by isolated bunch(s).
- Event system can provide these functionalities with jitter in 5 ~ 20 psec dependent upon EVR module usage.
- The Basic hardware configuration for beamline timing interface in TPS is presented in the right figure.



Current Status & Summary

- The implementation of the timing system and timing sequencer is ongoing. Various operation scenarios are analysis thoroughly. Prototype test by Matlab scripts was tested in 2011. Change to EPICS sequencer by program using SNL is on-going. Timing fibre network installation will complete in October 2013. Set up of all event system modules equipped EPICS IOCs are scheduled in the first quarter of 2014.
- Implementation of the TPS control system is on-going. Implement various application programs are underway. All components are ready for installation. The timing system will be ready for integrated system test when the TPS installation done.

*E-mail: chunyiwu@nsrrc.org.tw