COMPARISON OF SYNCHRONIZATION LAYERS FOR DESIGN OF TIMING SYSTEMS

Conclusion

- It is possible to implement similar timing system functionality using either an event-based synchronization layer or White Rabbit.
- The different synchronization facilities (interfaces) inside the FPGA firmware will have important implications on the timing system firmware architecture.
- The White Rabbit architecture will revolve around absolute time scheduling, whereas an event-based architecture will revolve around downstreaming precisely scheduled event triggers.

Introduction

- The timing system provides **timing critical services** to the control system, as shown in Fig. 1.
- Commercial off-the-shelf products typically require **customization**, which adapts them to the **machines unique requirements**.
- The **synchronization layer** is a commercial off-the-shelf product together with the fully or partially supplied firmware, see Fig. 2.
- The synchronization facilities (FPGA firmware interfaces) of two different synchronization layers, **White Rabbit** [1] and **Micro-Research Finland** [5], were reviewed, as it has direct implications on how the timing system can be implemented.
- As proof-of-concept a set of timing system services was implemented, interfacing the White Rabbit firmware. Fig. 3 provides a simplified architecture describing the implementation.
- Other timing systems studied were REDNET [2], SINAP [3] and GMT [4]. REDNET and SINAP are both event based timing systems, the former using MRF. GMT is based on White Rabbit.

Timing System Services

- First, there are the **fundamental services**, e.g., coordinated actions of devices throughout the facility and time stamping of events, i.e. triggers of actions and acquisitions of data samples.
- In addition, there are the **machine specific services**, e.g., the Virtual Accelerators concept given in [2] and real-time communication channels.
- Typical requirements for any timing system are the **accuracy** and **precision** of synchronized outputs. Each syncronization layer has its own characteristics, stemming directly from its conceptual design and implementation.
- The synchronization layer that gives the lowest timing system implementation complexity is recommended.

Synchronization Layer

- The synchronization layer is an **abstraction layer** that conceals the synchronization **below** the timing system.
- Synchronization can be made in **two** conceptually different ways: either
  a) ensure that there is **equal propagation delay** to all the receivers and let actions be executed immediately upon reception, or
  b) **synchronize time** (as in 12:00 o'clock) of all network nodes and distribute schedules in advance with actions and exact time of execution.
- All synchronization layers implement network-wide **clock** (as in digital oscillator) **synchronization** (frequency and phase) to ensure alignment of output signals on the recievers.
- Performance measurements available cannot be compared in a fair manner. In the future a dedicated test bed will be set-up for comparison.
- One major difference is the network latency. In MRF the downlink fan-out latency is insignificant, since there is no routing, and the uplink is in the 100 - 200 ns range per concentrator [6]. In White rabbit the latency per fan-out layer in both directions is in the 10 - 20 µs range [7].

Results

- The implemented proof-of-concept timing system provides a set of fundamental services, e.g., delivering synchronized pulses at multiple timing receivers.
- The result of the comparison is that, even though the interfaces are widely different, similar services can be realized, although through different architectural approaches.
- All White Rabbit based timing systems must have output queues in the receivers since actions are received in advance, not immediately executed, like in event-based timing systems.
- Strict requirements for low latency and deterministic loop-back latency can exclude White Rabbit as a viable option.

Authors

Alexander Aulin Söderqvist, Niklas Claesson, Joachim Neves Rodrigues, Department of Electrical and Information Technology, Faculty of Engineering, Lund University, Lund, Sweden.

Rok Tavčar, Rok Štefanič, Jože Dedič, Cosylab, Ljubljana, Slovenia.

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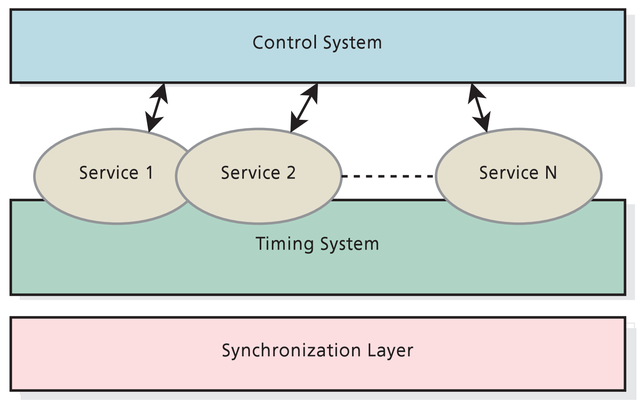

Figure 1: The control system needs several timing critical services, which are provided by the timing system. The timing system itself is constructed on a synchronization layer which provides the basic capabilites to enable implementation of such services.

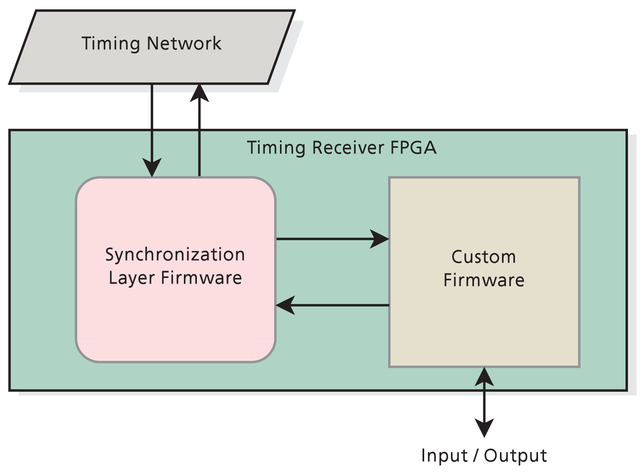

Figure 2: The timing receiver firmware can be seen as two separate modules. The synchronization layer, which is given by the vendor (MRF/WR), and the custom part, which is implemented as part of the timing system.

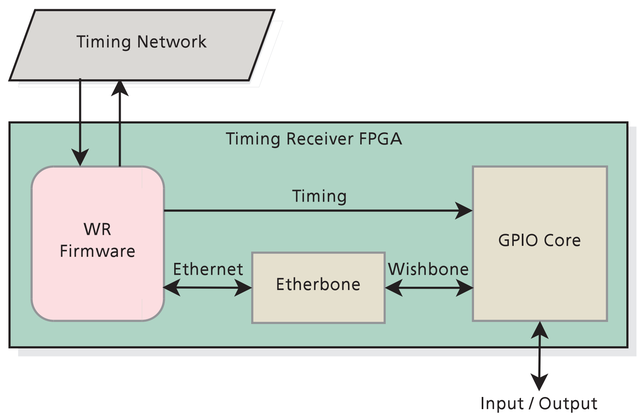

Figure 3: This is a simplification of the designed timing receiver architecture. It shows how the White Rabbit firmware interfaces are connected and what kind of data is being exchanged. Everything except the WR firmware is considered to be custom. The wishbone bus is used for accessing registers in the GPIO Core.

References

[1] P. Moreira, J. Serrano, T. Włostowski, P. Loschmidt and G. Gaderer, "White Rabbit: Sub-Nanosecond Timing Distribution over Ethernet", *Proceedings of ISPCS2009, Bresia, Italy*, 2009.

[2] R. Tavcar, R. Stefanic, Z. Kroflic, J. Dedic and J. Gutleber, "Timing system for Medaustron based on off-the-shelf MRF transport layer", *Proceedings of IPAC2011, San Sebastián, Spain*, 2011.

[3] M. Liu, C. X. Yin, L. Y. Zhao, D. K. Liu, "Development Status of Sinap Timing System", *Proceedings of IPAC2013, Shanghai, China*, 2013.

[4] D. Beck, R. Bar, M. Kreider, C. Prados, S. Rauch, W. Terpstra and M. Zweig, "The new White Rabbit based timing system for the FAIR facility", *Proceedings of PCaPAC2012, Kolkata, India*, 2012.

[5] J. Pietarinen, "MRF Timing System", *Timing Workshop CERN*, February 2008.

[6] J. Pietarinen, "Timing System with Two-Way Signalling", *EPICS Meeting Padova*, October 2008.

[7] M. Kreider, "The FAIR Timing master: A discussion of performance requirements and architectures for a high-precision timing system", *Proceedings of ICALEPCS2011, Grenoble, France*, 2011.

[8] M. Lipinski, T. Włostowski, J. Serrano, P. Alvarez, J. D. G. Cobas, A. Rubini and P. Moreira, "Performance results of the first White Rabbit installation for CNGS time transfer", *Proceedings of ISPCS2012, San Francisco, USA*, 2012.

[9] "Open Hardware Repository", 2009. [Online]. Available: http://www.ohwr.org.