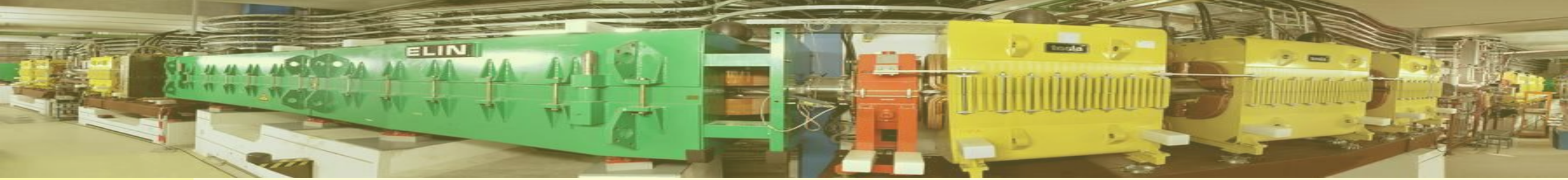

Timing System Developments Based on White Rabbit

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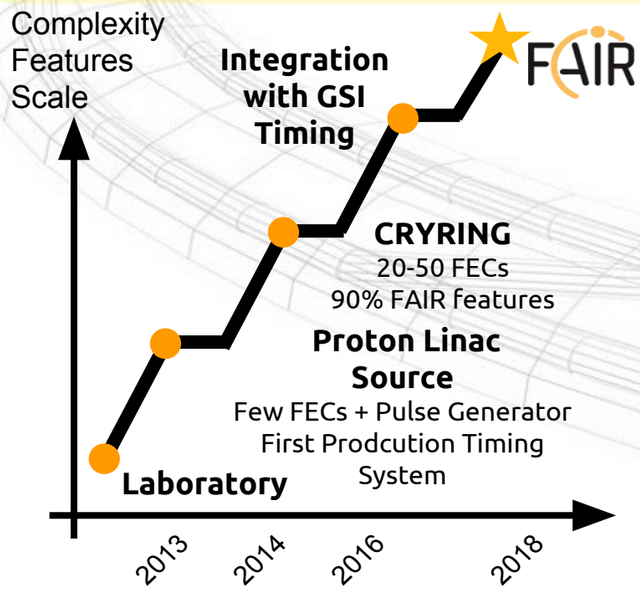
Requirements

- Clock, events and timestamp distribution
- Upper-bound latency of event distribution
- Timing events 1ns resolution
- Machine Cycle from 20ms up to hours
- 2000 Front End Controllers (FEC)
- True parallel operation
- Reliable and robust

Development Plan

Iteration cycles releasing production Timing Systems



Design

White Rabbit

Timing Master

Timing is distributed in the network from a WR switch configured as master. The master uses the 10 Mhz and PPS signal from a GPS for synthonization and the UTC Time for the synchronization of the network

Mngmt Master

It runs network mngt and monitoring software. it configures the network parameters.

Timing Network

WR switches

Timing

Timing and Data resilience against network failures is achieved using redundant connections.
Upper-bound delivery latency guaranteed using a QoS and Cut-through switching.

Data

Etherbone

Data Master

Take machine commands from LSA and convert into sequence of programs, the beam production machine. Run this programs in parallel generating events datagrams sent to the timing network.
It's a Etherbone master sending etherbone msg.

CPU - API Bloc
LSA to Programs

FPGA - SoftCPU Cluster
Pairs execution time, events and FECs

FPGA- Event Concentrator
Aggregates and schedules de transmission of events.

Timing Receivers

Timing Interface of FECs
Tightly synchronized to the TM
Design centered around WB combines the standard func. with specific bus interfaces.

Form Factors
PCIe
VME
SCU
Stand-alone

I/O
Lemo
LVDS
HDMI

FPGA-SoC

Event-Condition-Action Scheduler Unit
Generates control signals at pre-programmed times.

Timestamp Latch Unit
Generates timestamps triggered by signals

Timing Network ⇦ White Rabbit IP Core ⇔ Etherbone Slave ⇒ Wishbone