SIRIUS CONTROL SYSTEM: CONCEPTUAL DESIGN

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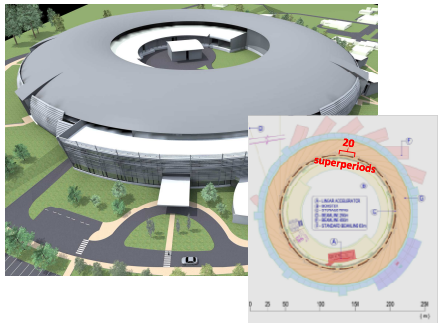
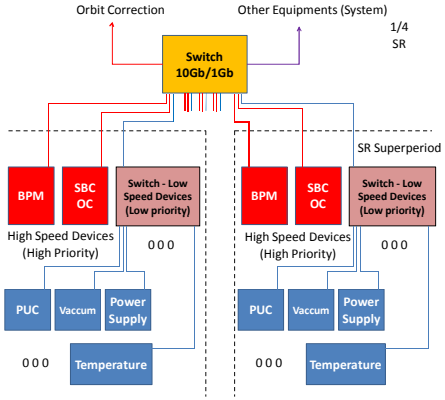
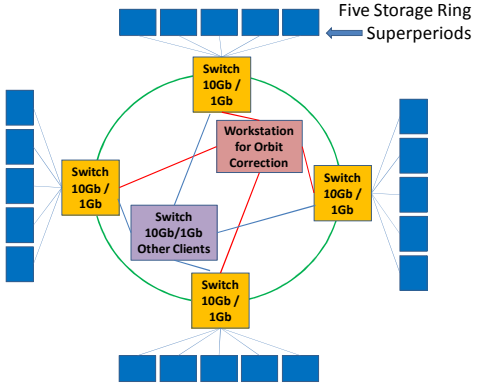


Sirius is a new 3 GeV synchrotron light source currently being designed at the Brazilian Synchrotron Light Laboratory (LNLS) in Campinas, Brazil



Storage Ring Network Detail



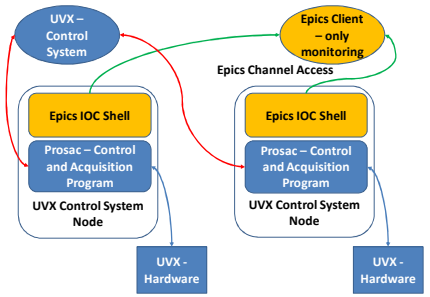
The network topology adopted for the storage ring middle and equipment layer will have double star extended architecture, with the first star connecting the high priority equipment (HPE) and the other one the low priority equipment (LPE).

Round Trip Time for SBC, plus latency time of unmanaged and managed switches

Processor	Average Time (uS) @100B payload TCP Protocol (60 S test)		
	Direct	Unmanaged	Managed
Intel Core 2 Duo SL9400 #2cores @1.9GHz - 2GB	80.42	101.69	105.41
(b) AMD Geode LX800 #1core @500MHz - 0.5GB	143.00	150.46	158.89
Intel Celeron 847 #2cores @1.1GHz - 2GB	229.12	231.61	245.45

Round Trip Time for SBC

Processor	Network	Average Time (uS) @100B payload (60 S test)	
		UDP	TCP
(a) AMD Geode LX800 #1core @500MHz - 0.5GB	82551ER @0.1 Gbps	148.42	158.84
Intel Atom 530 #1core @1.6GHz - 1GB	82574IT @1.0 Gbps	161.71	161.84
(b) AMD Geode LX800 #1core @500MHz - 0.5GB	RTL8100 CL @0.1 Gbps	132.98	143.00
Intel Celeron 847 #2cores @1.1GHz - 2GB	RTL8111 F @1.0 Gbps	227.61	229.12
(c) AMD Geode LX800 #1core @500MHz - 0.5GB	82551ER @0.1 Gbps	153.21	164.64
Intel Core 2 Duo SL9400 #2cores @1.9GHz - 2GB	82574IT @1.0 Gbps	61.60	80.42



Epics Training in UVX Control System