

## DIGITAL CONTROL SYSTEM OF HIGH EXTENSIBILITY FOR KAGRA

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### Abstract

KAGRA is the large scale cryogenic gravitational wave telescope project in Japan which is developed and constructed by ICRR of The University of Tokyo. Hitachi Zosen Corporation (after called Hitz) was in charge of PCI Express input/output (PCIe I/O) chassis and the anti-aliasing (AA) and anti-imaging (AI) filter board of KAGRA digital control system. Hitz contribute to low noise operation for KAGRA interferometer control. This paper reports these products performance.

### KAGRA PROJECT

According to Albert Einstein's theory, which predicts the existence of gravitational wave, asymmetrical mass changing is the distortional time-space transferring at light velocity. Currently, gravitational wave detection is tested with laser interferometer of large scale. In Japan, Large-scale Cryogenic Gravitational wave Telescope, that poplar name is KAGRA, has been constructing at 1000m underground (in maximum) the mountain in Kamioka, Gifu-prefecture.

A laser interferometer observes the distortional space to detect gravitational wave. It measures difference of passed time of irradiated in-phase lasers that are reflected from mirrors located each optical cavity of 2 directions crossing at right angles. Practically, we realize the arrival time lag by measuring the change of the interference article of the laser beam. However, detected gravitational wave signal is very small. Therefore, observing interference fringes of gravitational wave has to be larger facility and circuit of higher accuracy. [1]

Currently, as the large laser interferometer, there are Hanford and Livingstone sites of LIGO (Laser Interferometer Gravitational Wave Observatory) in USA and EGO/VIRGO (European Gravitational Observatory and VIRGO) that are operating gravitational wave detection. LIGO's each site has 4km scale optical cavity. VIRGO is 3km. KAGRA under construction is 3km scale optical cavities located all under the ground. Such underground construction has the advantage of using very hard bedrock in Kamioka, Gifu-prefecture, which reduces effect of vibration on ground surface. Therefore, high accuracy of observation can be expected.

And furthermore, to achieve higher accuracy of observation, we have various plans, making longer the optical cavity by Fabry-Perot Interferometer, cooling mirrors to -253 degrees Celsius by cryostat for preventing thermal noise, providing suspension system for preventing vibration mirrors, using high power and high coherency laser and low noise electrical circuit. Therefore, KAGRA achieves target of accuracy of  $10^{-19}$  m/ $\sqrt{\text{Hz}}$ .

The digital control system of KAGRA controls KAGRA components to realize high precision observation. This system consists of real-time front-end (RTFE) computers and servers to manage RTFE computers. Each RTFE computer is connected to 18 slots PCIe I/O chassis to extent. Differential 32 channels analog to digital converter (ADC) module or differential 16 channels digital to analog converter (DAC) module or 32 channels digital output (DO) module will be equipped into the PCIe I/O chassis. Gentoo Linux OS is installed into RTEF and servers. All RTFE are connected to servers and operate computers through the four type networks. The operating computers are implemented EPICS [2] that is often used as particle accelerator system. If you want to know the KAGRA control system exactly, you can browse title of "Real Time Control for KAGRA 3km Cryogenic Gravitational Wave Detector" at status project session in this conference [3].

### DIGITAL SYSTEM DESIGN

KAGRA digital system is described in Figure 1. The digital system, RTFE consists of the ADC, the DAC, the digital output (DO) and digital input output (DIO) and the computer. The ADC inputs a signal from interferometer (IFO) to a computer. The DAC outputs the processed signals. The DO selects to handle some signal from switch module. The DIO inputs such as trigger signal and outputs the selection signal for the 1PPS signal from timing system. The computer processes the inputted signal by such as PID algorithm, filtering and trigger control.

The input signals are such as light-path-length control signals and angle control signals from various sensors like photo detector and the interferometer used as a gravitational wave detector. The output signals are such as an actuator signal which controls the mirror hung by the pendulum. Figure 1 shows the conception design of KAGRA digital system. In the feedback loop, the signals from various sensors of the interferometer are fed back to the actuators of the interferometer through the ADC, the DAC, several signal filters and the computer. Frequency of the feedback loop is 16384 Hz.

Noises, except the quantization noise, do not theoretically exist in the computer. Therefore a design of the feedback becomes very effective if noise mixture at the input and output part to a computer is settled.

Observed signal level is low in the DC domain and high in the high frequency domain. The signal level depends on the frequency characteristic of ADC. If the signal handled without changing, the signal is covered with a noise of the high frequency domain. Therefore, we can avoid a noise of the DAC by adding the signal level

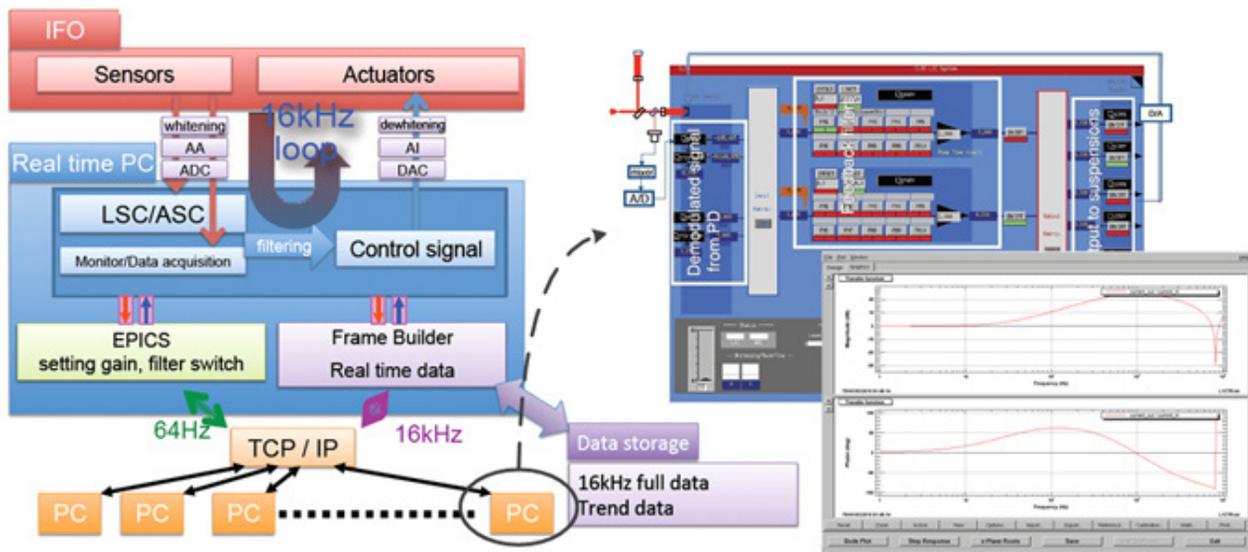


Figure 1: The Concept Design of KAGRA Digital System.

of the high frequency domain and flattening a signal beforehand. Also, we can avoid a noise of the DAC by reproducing signal level of the all frequency domain. The former is implemented by the whitening filter, and the latter is implemented by the dewhitening filter.

Further, The Alias, down-converting caused by a noise higher than the sampling frequency appears by producing to digital system. The ADC and DAC sampling frequency are 65536Hz. Therefore, the Anti-aliasing (AA) and the Anti-imaging (AI) filter are used for excluding the alias from the ADC and DAC noise. That is the AA/AI filter board we produced. These are analog filters installed on the outside of the RTFE. The computer of the RTFE and IFO are connected by fast transfer network. These are installed in each section of the optical cavities.

### AA/AI Filter Board

The AA/AI filter board is a notch filter (passive filter) and third-order low-pass filter (active filter) to prevent quantization effect (Aliasing) of analog to digital conversion. The frequency of analog to digital conversion is  $2^{16}$  (65536) multiplied from 1PPS signal. A combination of Butter-worth low-pass filter (BLPF) and single notch filter (SNF) achieves 10kHz cut-off frequency for BLPF and 65536Hz elimination band for SNF.

The AI filter prevents digital to analog conversion noise from affecting high frequency domain. Both the filter boards have different purpose, but have the same circuit and the same bandwidth. AA/AI filter board implements 8 channels. Hitz produced 320 boards enough to KAGRA's control channels. AA/AI filter board specification is described in Table 1.

### PCIe I/O Chassis

PCIe I/O Chassis performs high-speed data transmission (input/output of the analog and digital signal) between I/O boards and the computer for digital real-time

Table 1: Specification of AA/AI Filter Board

Item	Description
Number of filter circuit	8 circuits/board
Input signal character	Less +or- 10V, differential
Output signal character	Less +or- 10V, differential
Connector type	D-sub 9
LED	Power indicator
Circuit gain	1
Notch filter character	Signal attenuation: Less -75db @65536Hz
Low-pass filter character	Order: Third Cutoff frequency: 10kHz (-3dB)

control. PCIe IO Chassis consists of a PCIe backplane, a PCIe chassis interface board, ADC adapter boards, DAC adapter boards and a timing slave module. We adopted BPX6806-EPS of Trenton Technology as a PCIe backplane that is same as LIGO. It is 20-slot wide motherboard based on PICMG1.3 standard and has one slot for system host board (SHB) and 18 slots slaves. PCIMG1.3 supports USB and Ethernet interface, however, that aren't used in this system. PCIe chassis interface board sends external sampling trigger signal to ADC and DAC and selects slot which provides the trigger signal. The  $2^{16}$  multiplied sampling trigger is synchronized with 1PPS signal from the timing slave board. In these signal switching mechanism, DIO board takes it. The ADC and the DAC adapter board are intended to connect a sampling trigger signal to ADC and DAC. Hitz produced the PCIe chassis interface board and the ADC, the DAC adapter board.

In addition, PCIe I/O chassis can be inputted not only from a normal AC power but also direct DC from a stabi-

lization power supply. PCIe I/O Chassis specification is described in Table 2.

Table 2: Specification of PCIe I/O Chassis

Item	Description
Enclosure	4U, 19 inch rack mount type (EIA)
Max expansion slot number	18 x16PCIe cards
Power supply	ATX silence power supply (natural cooling type)
Cooling	Fan, installed front panel
Dimension	483(W)×177.0(H)×772.0(D)
Material	Electro galvanized zinc plated steel (SPCC)
Weight	17kg

### INSPECTION OF PERFORMANCE

#### AA/AI Filter Board

We evaluated performance of filtering circuit 10 kHz cutoff frequency about BLPF and SNF. Figure 2 shows the measurement of AA/AI filter board transfer function. The power supply unit for performance inspection is a low noise transistor type. The transfer function (gain, phase) of the AA/AI filter board is measured by oscillator sweeping from 10 Hz to 100 kHz.

Figure 3 shows the measurement of equivalent input noise. Output voltage signal is measured level depending on input noise.

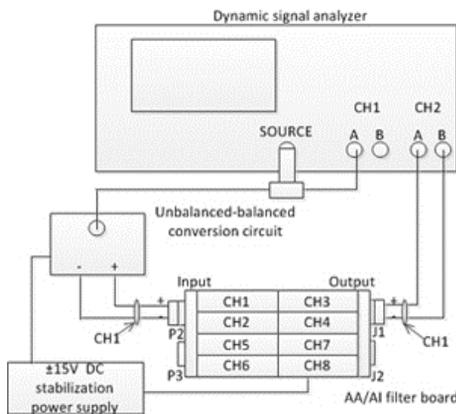


Figure 2: Block diagram of evaluation of the transfer function of LPF and SNF filter signal performance.

The point of the evaluation of the transfer function of the filter circuit is filter performance of BLPF and SNF. The tolerance was decided in reference to a judgment level of transfer function of LIGO. Figure 4 is a gain characteristic evaluation. Figure 5 is a phase properties. In the phase characteristic graph, a wave pattern turns

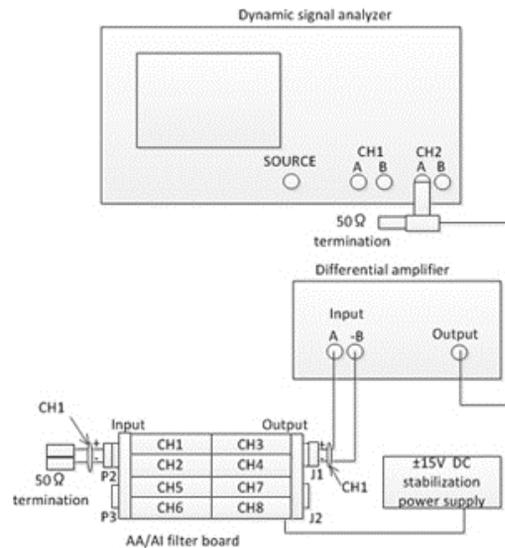


Figure 3: Block diagram of measurement of equivalent input noise.

around from plus 180 degrees to minus 180 degrees. Both gain/phase = 0 dB/165 at 1 kHz and gain/phase = 4.8 dB/25 at 10 kHz meet evaluation judgment value enough together. In addition, the evaluation of the eliminative performance meets -75 dB at 65,536 Hz enough.

Then, we measured the equivalent input noise of the filter circuit. The result is shown in Figure 6 and Figure 7. It is less than 50 nV/rHz at 125 Hz to 100 kHz and 80 nV/rHz at 10 Hz to 700 Hz. Both the results satisfy the judgment level. Some channels of measured boards did not meet the judgment level of the equivalent input noise. It is thought that the individual difference of an implemented differential amplifier produced a burst noise. Therefore, we changed differential amplifier from LT1492 to AD8622 has a few burst noises. However, defectiveness was even found in the board implementing AD8622 by the equivalent input noise measurement. As a result of analysing it, we thought about the possibility that a similar burst noise occurred in op-amp THS4131D which we used in BLPF. And as a result of changing it, the remaining channels satisfy the judgment level.

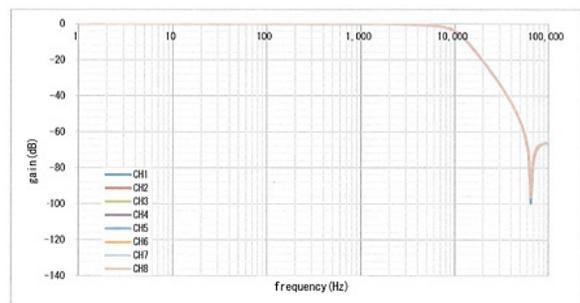


Figure 4: Graph charts of measurement of gain characteristic of LPF and SNF functions. This shown data is channel 1, serial No. 001.

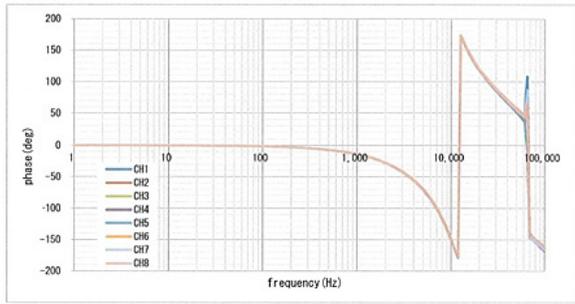


Figure 5: Graph charts of measurement of phase characteristic of LPF and SNF functions. This shown data is channel 1, serial No. 001.

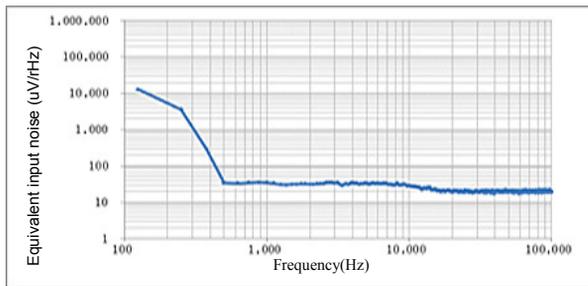


Figure 6: Graph charts of measurement of equivalent input noise. ( scope of 0~10kHz). This shown data is channel 1, serial No. 001.

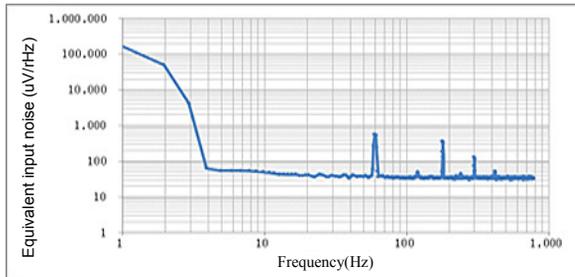


Figure 7: Graph charts of measurement of equivalent input noise (scope of 0~1kHz). This shown data is channel 1, serial No. 001.

### PCIe I/O Chassis

As an evaluation of the simple substance of RTFE, we carried out a connection examination between the PCIe I/O chassis and a computer. We implemented PCIe4 host cable adapter board into a computer and implemented expansion link board (ELB) for SHB slot into PCIe I/O chassis. Two types of cable length at 50cm and 2m are tested. We used lspci command and the application for detection systems (x1x14, x1vex) [4] to determine whether the computer recognized PCIe I/O boards.

In KAGRA digital system, the distance between the computer and the PCIe I/O chassis will be more than two or three meter length. Therefore, some meters length is necessary even if the least cable length. Furthermore, we cannot transmit it with the PCIe metal cable when using the cables more than 10m. Therefore, at the places far

more than 10m, we should connect by an optical fiber cable.

In the examination of the metal cable, when a 2m metal cable was used, it resulted that the normally reorganization with the lspci command and application will be about 1 time per ten times in starting processes. Since the transfer speed of GEN2 is 5.0 Gbps per one lane (double transfer speed of GEN1), this surmises that the construction state of the metal cable had influenced the transmission signal.

In the examination of the optical fiber cable, the 100m length optical cable connects between SHB and host cable adapter board. It resulted in failure. Although the plan was made on the board of the old model, GEN1 at the beginning, that of production discontinuous will estimate by a current model. Current model performs auto negotiation of GEN1 and GEN2. Nevertheless, since it did not operate, it converted about ELB by the result that there are some improvement items as a result of discussion with a vendor.

Next, it examined by the 10m cable of the modified version. Although it was used in the environment of auto negotiation, since there was much frequency where starting was poor, it has been recognized as fixing to GEN1 and examining by the basic input output system (BIOS) of a computer, with the optical cable.

### CONCLUSION

Hitz gave high precision, the treatment for the low noise in the production of electronic circuits in charge of KAGRA digital system. In the future plan, we will perform RTFE system and the loopback through the AA/AI filter and are going to examine the performance evaluation. In addition, in PCIe I/O chassis and the optical fiber cable connection between the host and it, stability can start only when we fix setting of GEN1 by the present conditions, the BIOS setting on the computer. Even if GEN1 fixed setting uses the computer which is not done, it is stable and thinks about working by optical fiber cable connection. Furthermore, it seems to be recognizable, and examination is going to take measures stable input and output board to implement against PCIe I/O Chassis in the future in GEN2.

### REFERENCES

- [1] <http://gwcenter.icrr.u-tokyo.ac.jp/>
- [2] <http://www.aps.anl.gov/epics/>
- [3] Osamu Miyakawa, "Real Time Control for KAGRA 3km Cryogenic Gravitational Wave Detector", ICALEPCS13, MOCOAB07, to be published.
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