HIGH PERFORMANCE AND LOW LATENCY SINGLE CAVITY RF CONTROL BASED ON MTCA.4

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Abstract

The European XFEL project at DESY requires a very precise RF control, fulfilling the objectives of high performance FEL generation. Within the MTCA.4 based hardware framework a LLRF system has been designed to control multi-cavity applications, require large processing capabilities. A generic software structure allows to apply the same design also for single-cavity applications, reducing efforts for maintenance. It has be demonstrated that the MTCA.4 based LLRF controller development achieves XFEL requirement in terms of amplitude and phase control. Due to the complexity of the signal part, which is not essential for a single cavity regulation an alternative framework has been developed, to minimize processing latency which is especially for high bandwidth applications very important. This setup is based on a fast processing advanced mezzanine card (AMC) combined with a down-converter and vector-modulator rear transition module (RTM). Within this paper the system layout and first measurement results are presented, demonstrating capabilities not only for LLRF specific applications.

INTRODUCTION

The European Free Electron Laser XFEL generates X-Ray laser light of tunable wavelength by the SASE process, using an electron beam accelerated to about 17.5 GeV, in a pulsed operation mode. Providing its users stable and reproducible photons, requires a very precise control of acceleration fields. The latest renovation of the LLRF system is a change of the controller hardware to an uTCA based technology standard, [1]. This hardware platform allows to fulfill the requirements for fast, high performance and reliable data processing within a modular framework. Regulation concepts and hardware developments can be shared and extended to operate at different locations or facilities, e.g REGAE [2].

The linear accelerator REGAE (Relativistic Electron Gun for Atomic Exploration) at DESY delivers electron bunches with a few femtosecond duration for time-resolved investigation of material structures, in a pump-probe configuration. The electrons of a pC bunch charge are emitted by impinging picosecond laser pulses onto a photo-cathode mounted in a 1.5-cell S-band RF-gun, [3].

Regulation aspects like system bandwidth, pulse duration and number of channels to be processed strongly vary in between both applications. Therefore a special setup has been developed dedicated for normal conducting (nc) acceleration structures, which is optimized in low latency processing and costs. Usually these applications process only a few channels, which aims to optimize the crate size to this hardware setup.

In this paper, first measurements of this single cavity LLRF controller is presented. The system has been setup at REGAE for a digital feedback loop, controlling a 6 us RF pulse at a sampling rate of 125 MHz. Internal loop delays have been measured. Further the amplitude and phase stability, mainly determined by imbalances of the high power amplifier has been measured as function of the proportional feedback gain. Finally extension to further facilities is outlined.

LLRF SYSTEM BASED ON MTCA.4

For high performance regulation of high frequency fields, fast processing capabilities are essential. One can distinguish between two types of applications currently being operated at DESY. For super conducting (sc) application usually many RF channels are combined to a so called VS which is used to control one high power klystron. Parallel processing of more then 100 channels is done within a LLRF crate. All signals have to be transferred to a central controller using low latency links. This is a well suited setup for this type of application and can be applied also to single cavity, NC systems.

Figure 2: XFEL GUN mTCA.4 LLRF system in 2U crate.

However while processing single channels, this setup is over-determined in terms of cost per RF station. In addition the strategy of data preprocessing and collecting at a central controller introduces latency in the control loop which prevents from operating in closed loop mode with reasonable gain margins. An example for a cost and space optimized LLRF version can be found in Fig. 2.

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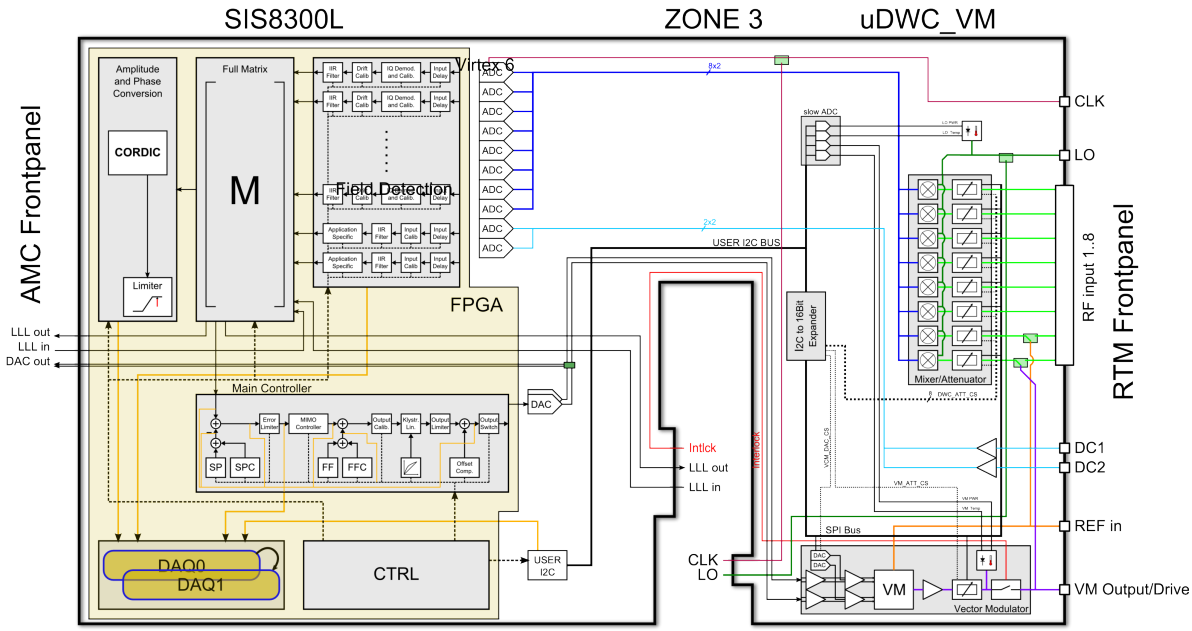

Figure 1: Schematic block diagram of signal flow within firmware.

This dedicated setup will be used for example at the XFEL RF Gun. The high bandwidth compared to SC applications of this regulation loop demands a very fast digital processing to cope with limited gain margin due to phase lags. Therefore the existing control loop architecture has been optimized to reduce the overall processing delay. Fast internal processing is achieved by lowering the data throughput, shortening pipe-lining length, and increasing the operating frequency of individual blocks. An outline of the control loop is given in Fig. 1. A detailed description of the individual processing steps can be found in [4].

The overall processing delay has been estimated to be about 500 ns. Basis for processing tasks is a field programmable gate array (FPGA) controller board used in SC applications for preprocessing tasks.

Hardware

The setup for the single cavity LLRF control system is based on the following two boards.

The SIS8300L [5] AMC is a FPGA-based (Xilinx Virtex6 series) digitizer / signal generator card. Maximum 10 input channels digitized by ADCs and 2 output signals generated by a dual DAC can be used. Converters and the FPGA are operating synchronously at 125 MHz frequency. Data acquisition and control are performed by an in-crate CPU which communicates with the controller card using a PCI Express bus.

The DRTM-DWC8VM1 is a analog front-end board performing a down- and up-conversion of measured and drive signals, respectively (see Fig. 3). Input RF signals are detected at an intermediate frequency (e.g. here 25 MHz), and output signal is a modified reference signal. The frequency band of RF signals is $0.7 - 4$ GHz and can be upgraded to 6 GHz

This system can be substituted to a direct sampling version, using a fast ADC sampling board in the uTCA standard and the special DWC version DRTM-DS8VM1, having 8 analog input channel of $5 - 400$ MHz and one upconverter $0.05 - 6$ GHz

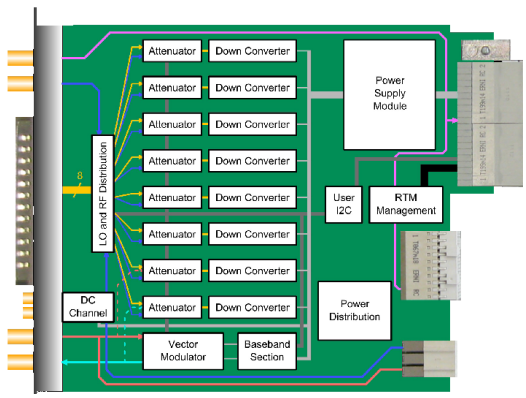

Figure 3: Schematic view of DRTMDWC8VM1 board.

Software

The corresponding firmware and software was designed to be comparable modular like the mTCA hardware. Functional block are shared in between systems which reduces maintenance effort and test setups for upgrades. Essential blocks like limiters, adjustable delays and scaling processes are equal. Fast processing controller blocks like filters and

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signal detection have been adapted to the higher sampling frequency and tuned for low latency processing.

Iterative algorithms running on the server level stabilizing the operation even if no direct feedback is turned on. This applications running in a pulsed mode, e.g. having pulse to pulse feedback reducing repetitive control errors and compensates for drifts. An example can be seen in Fig. 4.

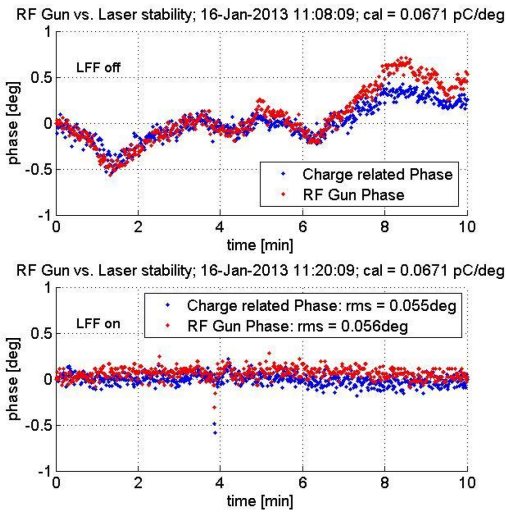

Figure 4: Output drift compensation using an iterative learning control algorithm.

Waveforms gathered by the controller during RF pulses are sent to the CPU module. The data is initially preprocessed and transmitted to the display and storage servers.

The combination of pulse to pulse feedbacks and in pulse output feedback schemes have been successfully operated for SC applications. With this low latency framework, it is possible to extend this strategy also for NC short pulse applications.

MEASUREMENT RESULTS IN CLOSED LOOP OPERATION

The presented measurement results are recently derived from REGAE. The previous measured loop delay 1 us has been reduced to about 600 ns as it can shown in Fig. 5, where also individual delays to dedicated points within the loop are presented. The main contribution is due to reduction of board communication links compared to the previous setup.

For the first measurement in close loop operation, a combination of a proportional feedback plus IIR lowpass filter has been used. The field stability as function of feedback gain and filter corner frequency is shown for the field phase in Fig. 6. The minimum can be found already for low gain settings where high frequency distortions are still suppressed by the controller. The given phase lag reduces the gain margin, and must be further optimized.

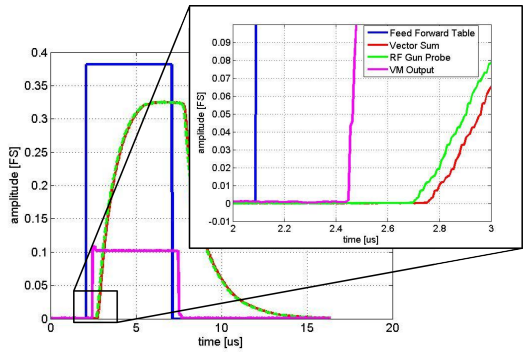

Figure 5: Integral loop delay measurement with new hardware setup.

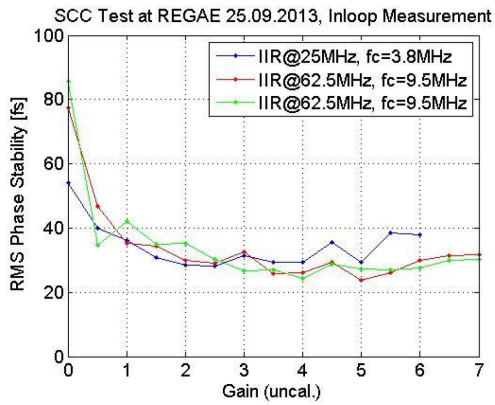

Figure 6: Phase stability gain scan for different filter settings.

OUTLOOK

A permanent system integration is currently being setup for REGAE and the XFEL RF gun. Long term stability and experience are to be gained during regular operation conditions. Further this setup will be used in different facilities outside of DESY, which requires a generic software design for integration in different control system frameworks. Software packages and drivers are going to be supported.

REFERENCES

[1] J. Branlard et al.,"The European XFEL LLRF system," IPAC'12, New Orleans, Louisiana, USA, MOOAC01.

[2] M. Hoffmann, H. Schlarb, C. Schmidt, W. Jalmuzna, A. Piotrowski, "Precision LLRF Controls for the S-Band Accelerator REGAE", IPAC'13, Shanghai, PRoC.

[3] M. Felber, M. Hoffmann, U. Mavric, H. Schlarb, S. Schulz,"Laser synchronization at REGAE using phase detection at an intermediate frequency," IPAC'12, New Orleans, Louisiana, USA, WEPPD048.

[4] I. Rutkowski, L. Butkowski, M. Hoffman, H. Schlarb, C. Schmidt, "REGAE LLRF control system overview", IPAC'13, Shanghai, PRoC.

[5] Struck innovative systems, "www.struck.de"

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