

# A PXI-BASED LOW-LEVEL CONTROL SYSTEM FOR THE FAST PULSED MAGNETS IN THE CERN PS COMPLEX

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## Abstract

Fast pulsed magnet (kicker) systems are used for beam injection and extraction in the CERN PS complex. A novel approach, based on off-the-shelf PXI components, has been used for the consolidation of the low-level part of their control system. Typical functions required like interlocking, equipment state control, thyatron drift stabilisation and protection, short circuit detection in magnets and transmission lines, pulsed signal acquisition and fine timing have been successfully integrated within a PXI controller. It comprises a National Instruments NI PXI-810x RT real time processor, a multifunctional RIO module including a Virtex-5 LX30 FPGA, a 1 GS/s digitiser and a digital delay module with 1 ns resolution. National Instruments LabVIEW development tools have been used to develop the embedded real time software as well as FPGA configuration and expert application programs. The integration within the CERN controls environment is performed using the Rapid Application Development Environment (RADE) software tools, developed at CERN.

## INTRODUCTION

A typical PS kicker magnet installation comprises a number of individual pulse generator modules grouped together. The generator modules are completely independent of each other and are individually controllable from the top layer or the Frontend Controller (FEC) as shown in Fig. 1. The FEC groups the generators together to perform a single function or a number of different functions, for example extraction over multiple turns or multiple batch operations. See layout, Fig. 2.

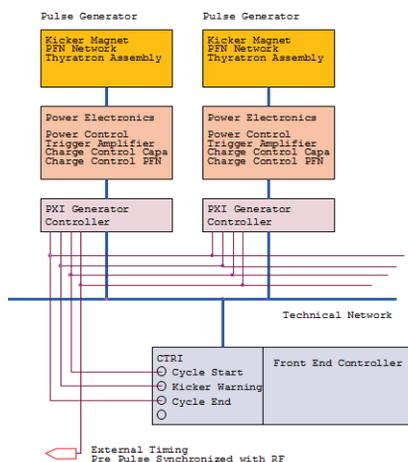


Figure 1: Block diagram of a typical kicker system layout.

The FEC acts as the master and data concentrator for all generators and provides a uniform interface to the hardware equipment as seen from the application layer. Communication with the generators is done via Ethernet.



Figure 2: Kicker system layout.

The CERN PS complex kicker control system is fully multi-user compatible allowing a dynamic management of different operational settings per machine cycle with a minimum machine cycle length of 1.2 sec.

The timing signals are generated at the FEC level and distributed to the different generator module(s) for synchronisation with the different machine cycles (cycle start, cycle end and cycle warning) or for synchronisation with the current beam process (pre-pulse).

## GENERATOR MODULE

A generator module can be seen as three different subcomponents:

- The kicker magnet with its pulse forming network and fast thyatron switches;
- The power electronics for power distribution, triggering and charge control;
- The generator electronics, for state control, interlocking logic, fast protection, signals acquisition and data monitoring.

A typical kicker system module (Fig. 3) consists of a cable Pulse Forming Line (PFL), resonantly charged to a given high voltage with the so-called Resonant Charging Power Supply (RCPS), connected via a high-voltage switch to a magnet load. Due to the very fast rise-time requirements, and relatively short pulse lengths, in the PS a cable PFL is preferred to a lumped element in most of the systems. The PFL is discharged by a Main Switch thyatron (MS) into the magnet. Some systems have a terminated magnet for faster rise times, others have a shorted magnet for larger deflections. The other end of the PFL is connected to a terminating resistor and a Dump

Switch thyatron (DS) that allows for kicker pulse length adjustment and added security in case of magnet breakdowns.

As a rule of thumb a kicker magnet can be pulsed as many times per cycle as its RCPS has primary capacitor banks, generally two per generator. Pre-pulse is the signal from which the MS trigger and DS trigger are derived.

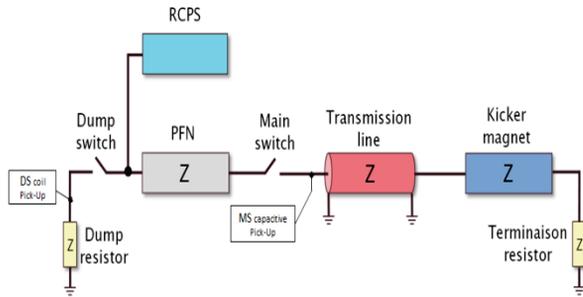


Figure 3: Typical kicker generator layout.

### PXI ARCHITECTURE

The former PS kicker magnet control system was built up using conventional electronic modules, one module for every individual function, forming a substantial and rigid system. All these functions have now been integrated into one PXI system (Fig. 4) resulting in a flexible system that can be ‘software’ tailored to the different needs of the variety of existing kicker installations.

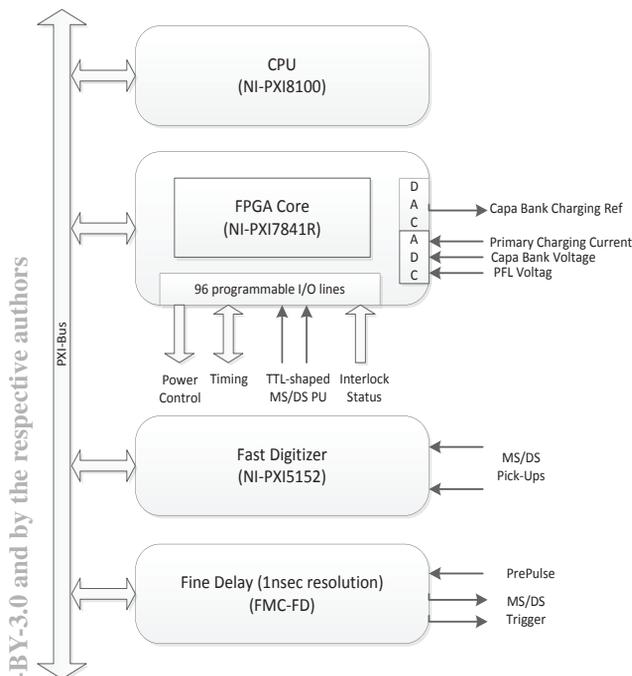


Figure 4: PXI Architecture.

### PXI HARDWARE

The following parts form the PXI controller:

- NI PXI-8100 RT, 2 GHz real time processor for cycle management, state control and integration within the accelerator complex control architecture;
- NI-PXI-7841R multifunctional RIO module includes a FPGA, 96 I/O channels, 8 channels 16 bit 200 kHz ADC, 8 channels 16 bit 1 MHz DAC for interlocking logic and fast protection;
- NI-PXI5152 300 MHz high-speed 1GS/s digitizer for pulsed signal acquisition and fast protection;
- 4 channel PXI-FMC 1 ns resolution delay generator for fine synchronisation with beam processes [1].

### PXI SOFTWARE

All PXI software development is realized with the LabVIEW software framework from National Instruments. The programming language used in LabVIEW, also referred to as ‘G’, is a dataflow programming language. The dataflow nature makes it very suitable for multicore processors.

The PXI systems control blocks are divided into three categories:

- RT program running on the CPU;
- FPGA program connected to the hardware;
- Specialist access for debugging and maintenance.

#### RT Program

The RT program is an event driven program that receives every machine cycle the operational kicker settings for the next cycle from the FEC. These settings contain the kick strength, the kick state and the fine synchronisation delays. Upon reception it passes the settings to the FPGA and sets the programmable fine delays for the kicker pulse start (MS trigger) and stop (DS trigger) timing signals by using the pre-pulse as the reference.

Communication with the FEC is done by means of the LabWindows/CVI Network Variable Library, using the so-called shared variables and the National Instruments Publish-Subscribe protocol (NI-PSP) [2], see Fig. 5.

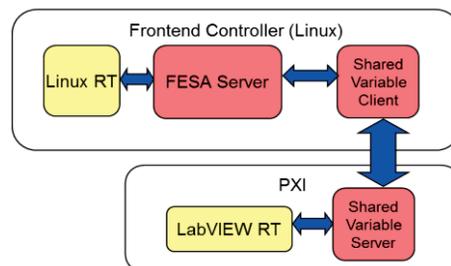


Figure 5: PXI – FEC communication.

At the upper level, the Rapid Application Development Environment toolkit (RADE) [3], developed at CERN, allows integration into the CERN controls environment, amongst a variety of other tools, via the Java API for

Parameter Control (JAPC) or the Controls Middleware (CMW) layer.

With the help of these tools and IEPLC [2], a PXI system can be accessed and controlled via the FEC and its standardized Frontend Software Architecture (FESA).

### FPGA Program

The FPGA receives the dynamic settings from the RT program and then performs the following task list:

- Timing gating, analysis and measurement;
- RCPS control, monitoring and protection;
- Maskable interlock and status handling;
- Generator state control (ON, OFF, STANDBY, FAULTY);
- Thyatron monitoring and protection;
- Short circuit detection in transmission line and magnet;
- Thyatron drift stabilisation.

### Specialist Access

There are several application tools available for the expert, either by directly accessing the shared variables containing all the settings (operational and configuration), status and acquisition, or via the FESA framework.

The FESA framework will give a view of the kicker system as seen by the control room whereas direct access of the shared variables will give a more detailed understanding of the system (Fig 6).

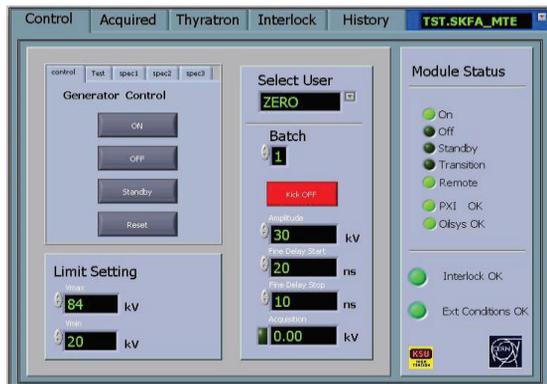


Figure 6: PXI control and status via FESA.

## PXI EMBEDDED FUNCTIONS

### Timing Gating

The kick state (ON or OFF) used for the timing gating is received as operational setting. The timing measurements and timing analysis is in relation to the C-train (in ms) from the start of cycle.

Timing errors are detailed, UTC time stamped and returned to the FEC.

### RCPS Monitoring

The RCPS monitoring measures the PFL voltage, the primary charging current and indicates if abnormalities are detected during the PFL charging process (over-

voltage, under-voltage, over-current & under-current) resulting in interlocking the system.

### Interlock

All interlocks are maskable. Furthermore they can be selected individually to switch off all power equipment via the Power Control Unit (PCU) or only prevent the generator from pulsing by inhibiting the timing.

### State Control and Status

The basic control functions for the generator are ON, OFF, STANDBY and RESET. These controls are hardwired to the PCU.

The PCU returns the status word to the FPGA indicating its current state (ON, OFF, STANDBY, WARMING-UP, FAULTY).

### Thyatron Monitoring and Protection

The function of this unit is to survey and protect the thyatron switches widely used within kicker systems. Monitoring of thyatron firing characteristics is done for security reasons and for optimisation of their lifetime.

The MS and DS have associated current pick-ups in order to measure their switching characteristics, MS-PU and DS-PU respectively (Fig. 7).

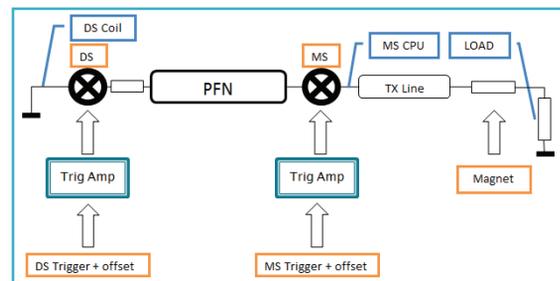


Figure 7: Thyatron protection.

In the FPGA the presence of the MS-PU and DS-PU signals is detected by TTL shaping the pick-up signals and correlated with the presence of trigger pulses. This way faulty shots and missing shots are detected.

Extra protection against negative current in the dump switch is taken when the magnet is shorted. Due to reflections the positive current has to be detected first before a negative current can be accepted. Positive current direction is assumed to flow from dump switch to main switch.

For the detection of short circuits in the transmission line, high voltage connectors or magnet, the ADC on the FPGA card is too slow. The use of a fast digitizer is therefore required.

When the magnet is shorted the time between the rising edge of the first positive MS-PU pulse and the rising edge of the second DS-PU pulse is measured. This distance is fixed and should be equal to the sum of the PFN electrical length and twice the electrical length of the transmission line. If this length is shorter then a short circuit has occurred.

In case the magnet is terminated any reflection measured in MS-PU indicates a short circuit.

Figure 8 shows a Bewley Lattice reflection diagram of a short circuited magnet with the current doubling in the magnet. With the help of this diagram reflection patterns can easily be traced.

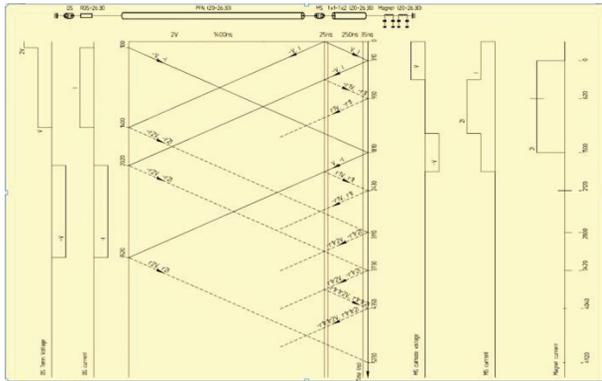


Figure 8: Bewley Lattice diagram.

*Thyratron Drift stabilization*

The drift stabilizer compensates deterministic drift inside the trigger amplifiers and the thyratrons ( $D_{equip}$ ) that will vary depending on equipment characteristics and aging effects. The system makes use of the fast digitizer for precise measurement of thyatron switching characteristics and corrects instabilities by adjusting the high precision fine delays in the triggering chain (Fig. 9).

The delay between MS & DS thyatron triggers and the positive edge of the current pick-up is measured ( $t_{meas}$ ) and, after subtraction of the user controllable delay ( $D_{ms/ds}$ ), fixed at a constant working point called the offset delay ( $D_{offset}$ ).

$$t_{meas} = D_{ms/ds} + D_{comp} + D_{equip}$$

$$D_{offset} = D_{comp} + D_{equip}$$

By correcting the compensation delay ( $D_{comp}$ ) so that the  $D_{offset}$  stays constant, a stable deflection pulse is achieved. Corrections are made after a settable number of consecutive drift in the same direction has been detected. The drift stabilizer generates an interlock when the required drift correction exceeds a settable level.

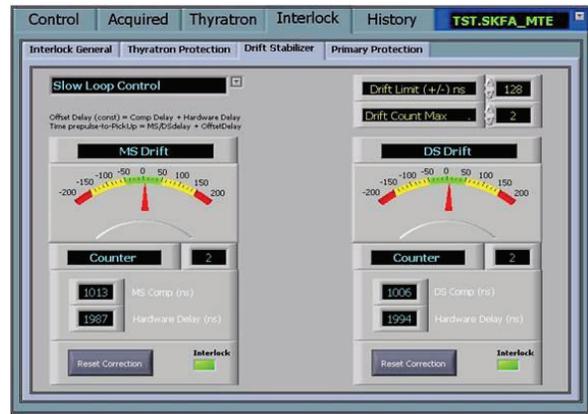


Figure 9: Drift stabilizer display.

**CONCLUSION**

The introduction of PXI in PS complex kicker controls offers an interesting alternative to existing technologies, not only because of its integration into the CERN controls system by means of RADE, but also because of its flexibility and ease of use.

The different types of kicker systems can be fine-tuned by altering the firmware of the system and no hardware changes are required. Parts of the described system will be integrated into other accelerator complexes, for example the RCPS monitoring and protection system will also be used for the LHC injection kickers. Furthermore measured signals like the PFL voltage, the charging current and the fast pick-up signals, used for protection of the generators can also be made available for visual monitoring at no extra cost.

**REFERENCES**

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- [2] F. Locci et al., "IEPLC, Automated Communication in a Heterogeneous Control System Environment," this conference.
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