DISTRIBUTED FEEDBACK LOOP IMPLEMENTATION IN THE RHIC LOW LEVEL PLATFORM *

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Abstract

We present a brief overview of a distributed feedback system based on the RHIC Low Level RF (LLRF) Platform. The general architecture and sub-system components of a complex feedback system are described, emphasizing the techniques and features employed to achieve deterministic and low latency data and timing delivery between local and remote sub-systems: processors, FPGA fabric components and the high level control system. In particular, we will describe how we make use of the platform to implement a widely distributed multi-processor and FPGA based longitudinal damping system, which relies on task sharing, tight synchronization and integration to achieve the desired functionality and performance.

INTRODUCTION

The various feedback loops developed as part of the new RHIC LLRF were implemented in software running in a Xilinx Virtex-5 FPGA embedded PowerPC 440 microprocessor. In general these loops consist of a proportional-integral-derivative (PID) controller in which the derivative term is seldom used. In some cases the PID controller is combined with an open-loop feed-forward controller to achieve better stability and faster response (see Fig. 1).

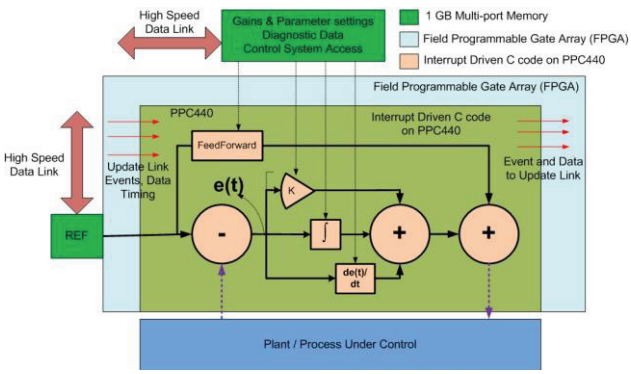

Figure 1: Basic structure of a PID controller developed within the RH IC LLRF Platform.

The loop code is written in the C programming language and is based on a standalone interrupt driven implementation. The Power PC is configured to use an FPGA based double precision floating point unit. High speed digital signal processing functions are defined in the form of hardware definition language and implemented within the FPGA fabric.

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We developed a series of platform based implementations to serve the specific requirements of each subsystem. Various LLRF Platform configurations have been deployed throughout the Collider-Accelerator Complex (C-AD) at BNL, including: the Relativistic Heavy Ion Collider (RHIC), the Alternating Gradient Synchrotron (AGS), the AGS Booster, the Electron Beam Ion Source (EBIS) [1] and the R&D Energy Recovery Linac (ERL). The kinds of loops developed and commissioned so far include cavity tuning loops, cavity IQ (magnitude and phase) control loops, various beam control loops and machine synchronization loops.

THE RHIC LLRF PLATFORM

A brief description of the hardware [2] and the overall system architecture [3] is required to clarify how the loops work and how components and sub-systems interact. Just four custom hardware components comprise the platform: a Carrier Board designed to host up to six XMC daughter cards, a four channel high speed ADC daughter card, a four channel high speed DAC daughter card, and an Update Link Master (ULM) (see Fig. 2).

Controller Chassis

An RF Controller is a 3U, 19 inch rack mount chassis which holds the Carrier Board and can be configured to serve as a Cavity Controller or a System Controller by installing a desired daughter card configuration. RF Controllers are connected to the ULM chassis (and thus to each other) via fiber optic links, forming a complex distributed system [4]. In addition, each controller provides a control system interface that manages remote access to all configuration parameters and diagnostic data via Ethernet [5,6].

Daughter Cards

The RF systems employ two types of daughter cards: a digital to analog converter (DAC) board and an analog to digital converter (ADC) board. The XMC DAC board has four 16 bit DACs with a maximum update rate of 600 Msps [7]. The XMC ADC board has four 16 bit ADCs with a maximum sample rate of 160 Msps [8]. Both the ADC and DAC boards feature a Xilinx FPGA with an embedded, hard core Power PC microprocessor which is used to implement the various feedback loop algorithms.

Update Link Master

An Update Link Master (ULM) chassis provides high speed deterministic event (timing) and data delivery, facilitating scalability, tight integration and synchronization between all sub-systems [4].

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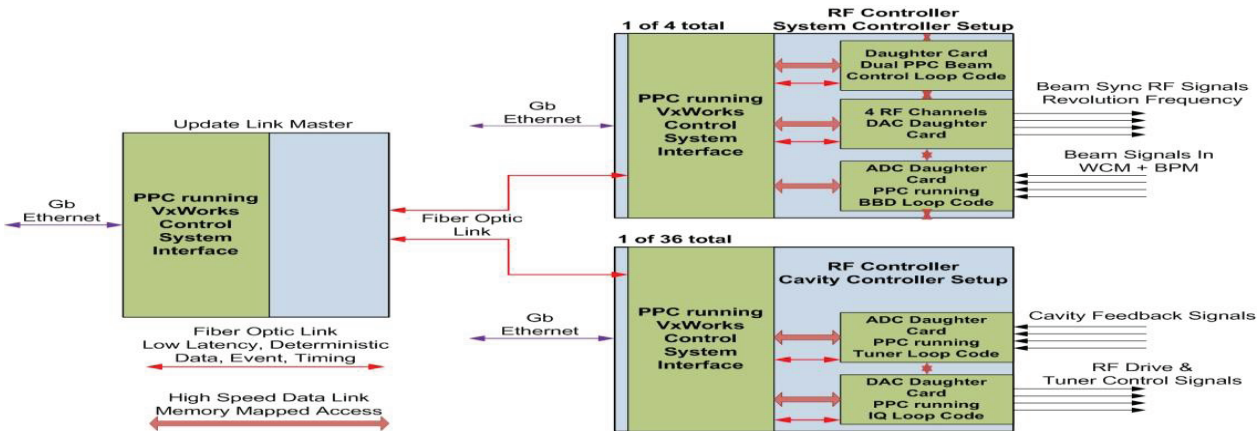

Figure 2: Block diagram of the overall system.

FEEDBACK LOOP IMPLEMENTATION

The first question we asked ourselves is whether these loops needed to be implemented in FPGA fabric or if using an embedded processor would be sufficient. We choose to implement some of the fundamental blocks of the digital signal processing in the FPGA fabric when speed and latency are paramount. The bulk of the loop code is executed in the embedded PPC processor, giving us design flexibility and development speed that come from using software. The processor based implementation has met our loop bandwidth requirements in every case thus far.

In order to ensure a very high level of synchronization between processors we use the Update Link system. The synchronization is critical in cases where we need a subset of processors to act in unison. Examples of this include transition crossing, rebucketing, and fault handling. Another case is where multiple processors contribute to a common loop and need to share information in real-time. A specific example of this is damping longitudinal oscillations.

Damping Longitudinal Oscillations

The new RHIC bunch by bunch longitudinal damper (BBLD) is an example of a loop that involves multiple processors, see Fig. 3.

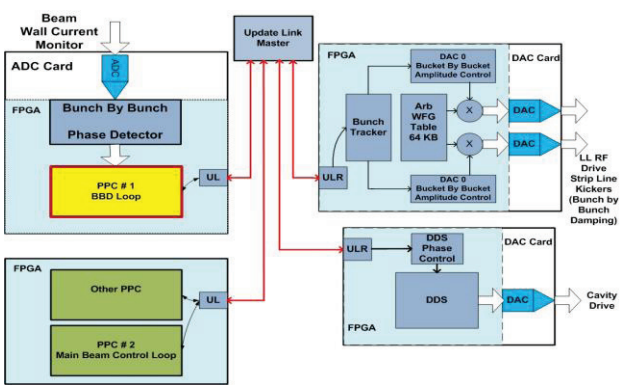

Figure 3: High level diagram showing main components of the longitudinal loop. See Fig. 4 for detail of BBLD loop.

This system was first introduced during RHIC FY13 polarized proton run to increase the threshold for intensity driven longitudinal coupled bunch instabilities, ultimately leading to record peak and average collision luminosities. As an extension to the existing RHIC LLRF system, the BBLD system required the additional integration of a spare embedded processor in a System Controller ADC, along with a new Controller chassis used to drive the broadband kickers used for incoherent coupled bunch damping (located one RHIC sextant away). Power limitations of the new broadband kicker amplifiers required that we continue using the existing bunch to bucket phase loop for damping of the average (coherent) longitudinal dipole motion. A high degree of synchronization was essential to orchestrate these combined damping efforts: the BBLD loop worked on coupled bunch instabilities while the main bunch to bucket phase loop continued damping the average (coherent) bunch motion.

A time domain bunch signal (wall current monitor) is digitized by a high speed ADC. Once digitized, signals are processed using algorithms implemented in the FPGA [8]. The FPGA presents the resulting processed bunch to bucket phase data of each bunch to the embedded PPC via memory mapped registers.

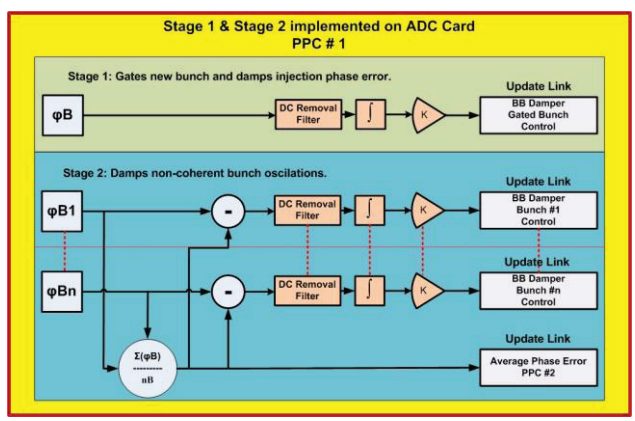

Figure 4: Two stages PPC#1 longitudinal damper.

The phase of each individual bunch is processed by PPC#1 as detailed in Fig. 4. The general signal

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processing consists of removing any average phase offset (DC removal filter), creating a 90 degree phase shifted term of the phase error (via an integrator) and a final gain adjust multiplier. The result of this computation is then transmitted via the update link to the remote BBLD Controller, and used to modulate the amplitude or phase of the RF drive to produce the desired damping.

The implementation sub-divides the task into a two stage process. Stage 1, shown in Fig. 4, consists of damping single bunch oscillations due to injection phase error. Injection phase oscillations are damped using the bunch by bunch damper during the first three to four seconds after a new bunch has been transferred into RHIC, Fig. 5 (bottom). After initial oscillations are completely damped the algorithm hands the bunch data to Stage 2 to continue being processed. Stage 2, illustrated in Fig. 4, is responsible for computing the average phase error of all bunches which have already been processed in Stage 1. This average phase error is then sent to the main bunch to bucket phase loop for damping coherent bunch oscillations [9]. While in this stage, the algorithm computes any phase error of a bunch that is not coherent with the average motion of all bunches and transmits this damping term to the Bunch by Bunch damper. This allows for both dampers to contribute to the common goal, producing the most optimal performance, bottom of Fig. 6.

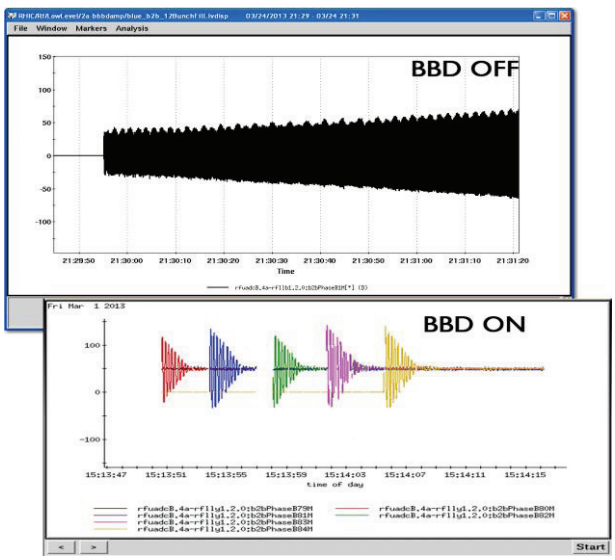

Figure 5: Top shows single bunch injection phase with damper loop turned OFF. Bottom shows the bunch by bunch damper ON acting on newly injected bunches.

Without added landau voltage, injected bunches will oscillate longitudinally due to injection phase mismatch and intrinsic instability, leading to emittance blow-up (Fig. 5, top). The bunch by bunch damper is able to damp these oscillations within 2s (Fig. 5, bottom). Though landau voltage remains necessary for stability at the highest intensities, the damper minimizes the required voltage, which further reduces landau induced emittance blow-up from injection phase errors.

The damper also inhibits longitudinal instabilities along the RHIC energy ramp, which would otherwise cause emittance blow-up and possibly beam aborts. Figure 6 (top) shows such instabilities occurring, as observed in the measured phases from several bunches. Figure 6 (bottom) shows another energy ramp with the damper active and no indication of large amplitude bunch phase oscillations.

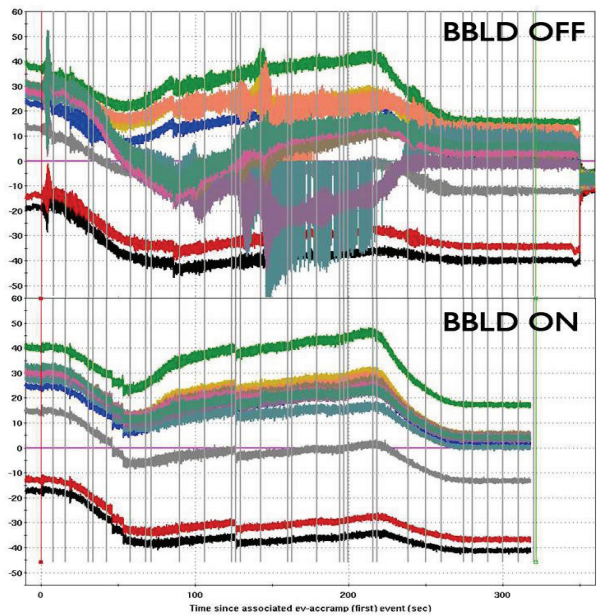

Figure 6: Bunch phase oscillations during two RHIC energy ramps: top shows BBLD OFF, bottom shows ramp with damper ON.

Implementation of Cavity Controller Loops

An RF controller chassis can be configured with one ADC card and one DAC daughter card to perform the task of controlling an RF Cavity. The cavity controller implements two feedback loops: I-Q feedback for control of cavity field amplitude and phase, and cavity tuning (resonance) control.

The cavity IQ-Loop resides in the DAC embedded PPC. It receives measured I and Q data from the ADC card over the Update Link. These values then get compared to the reference I and Q set points entered via the control system. The error terms are processed by a proportional-integral block, as shown in Fig. 7. The result is then passed to the DAC firmware to modulate the cavity RF drive. This processor is also responsible for cavity protection which turns OFF the cavity drive based on a variety of possible fault conditions.

The cavity resonance control loop (tuning loop) is implemented in the ADC embedded PPC. The processor obtains the phase of the digitized cavity forward and field probe signals from the phase detector [8] firmware via memory mapped registers. These phases are compared to find the phase error, which is processed by the PI loop in the ADC PPC and sent via the Update Link to the DAC to control the cavity tuner.

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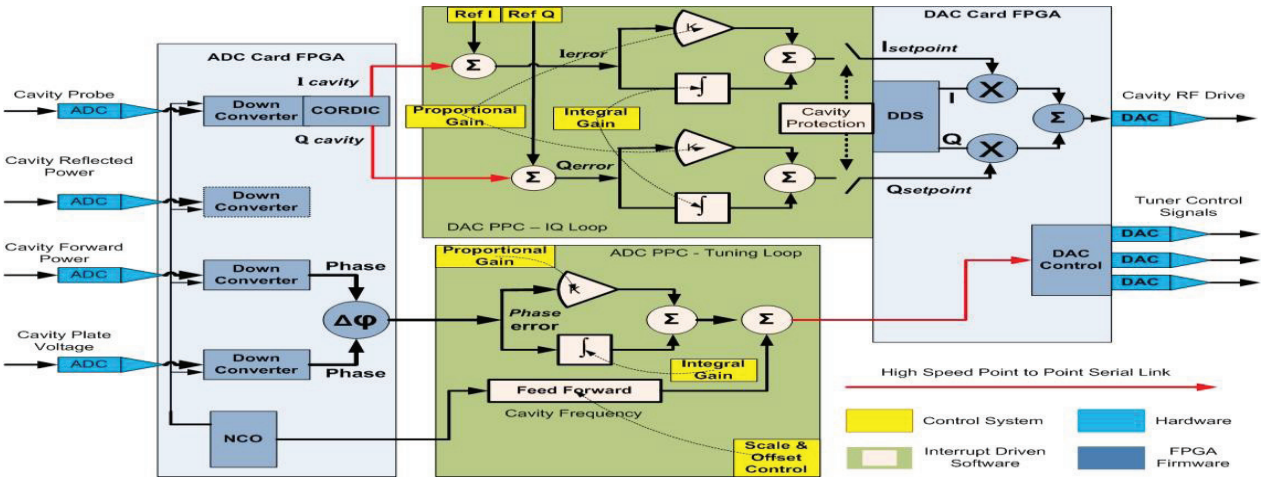

Figure 7: RF cavity controller, implementing a cavity resonance control loop and a cavity IQ-Loop.

Results of an IQ-Loop used to control the R&D ERL 703MHz 5-Cell Cavity are illustrated in Fig. 8. The open loop response of the cavity has significant error, due to strong microphonic detuning. The cavity closed loop response follows the reference very closely.

The closed loop steady state amplitude error is about 0.015% rms, with a phase error of about 0.02 deg rms.

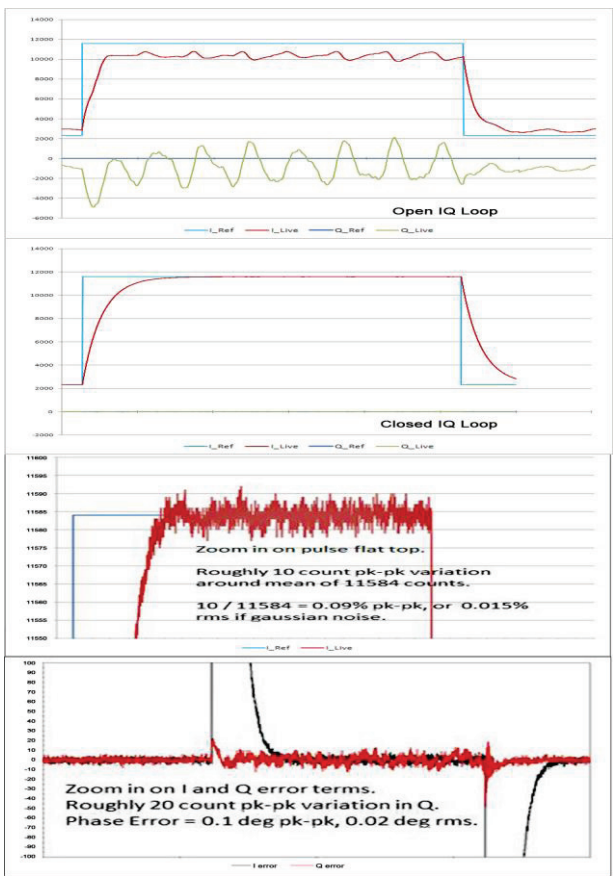

Figure 8: Results of using IQ -Loop of ERL 5-Cell cavity.

CONCLUSION

Various implementations of distributed feedback control loops have been developed using the RHIC LLRF Platform, and deployed throughout the C-AD complex. Over the past three years more than forty controllers have been installed into the various machine LLRF systems. These controllers, tightly integrated and synchronized via the LLRF Update Link have vastly improved RF system performance, flexibility and reliability.

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