Free and Open Source Software at CERN: Integration of Drivers in The Linux Kernel

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CERN Controls System Front End Computers (FECs)

The controls system relies on FECs on several form factors/buses, most of them based on Single-Board Computers (SBCs)

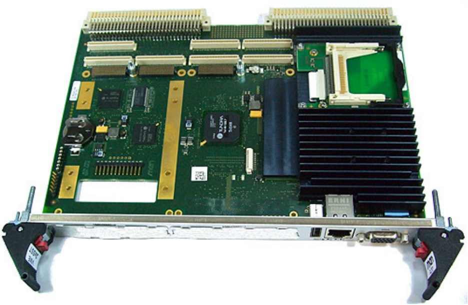
- Number of FECs: 1140
- Number of VME crates: 710

For the VME crates, the ongoing renovation process gives

- CES RIO2/RIO3 SBCs with PowerPC CPUs running LynxOS (around 605 crates by August 2011), to
- MEN-A20 SBCs with Intel CPUs running real-time Linux (around 105 by August 2011).

MEN A20 and the TSI148 chip and driver

The MEN A20 SBC is an Intel Core 2 Duo-based board interfacing to the VME bus via a Tundra TSI148 PCI-X to VME bridge chip.



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Beginning as an in-house and CERN-centric development

Why going upstream? (2010)

By mid-2010, the decision is taken to submit the driver for acceptance in the Linux kernel main tree. Motivation:

- Smoother maintenance in the (frequent) case of kernel API changes (see `Documentation/stable_api_nonsense.txt` in the kernel tree).
- Widespread distribution of the code base, which can then be enhanced and get contributed by researchers
- Contributing back in return to the many benefits the FOSS community gives us.

The original motivations were more ideological than practical

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Lessons learned

- It is hard, LKML and maintainers are tough
- One must be prepared to compromise (design, APIs, tools)
- One must build a reputation slowly
- Requires patience

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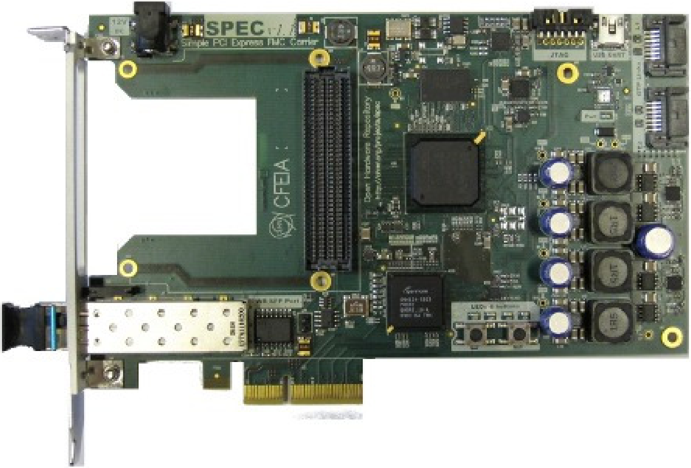
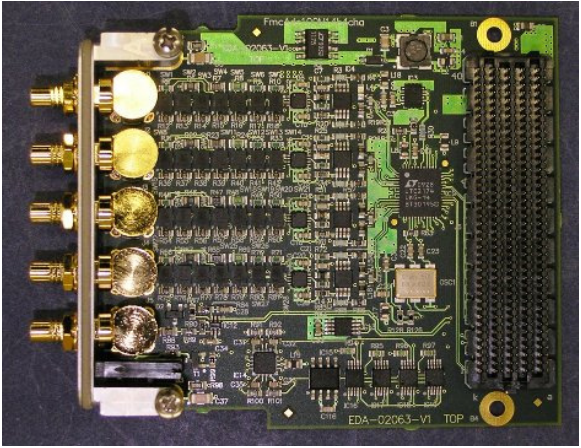
Why?

A typical data acquisition application: carrier



A typical data acquisition application: mezzanine

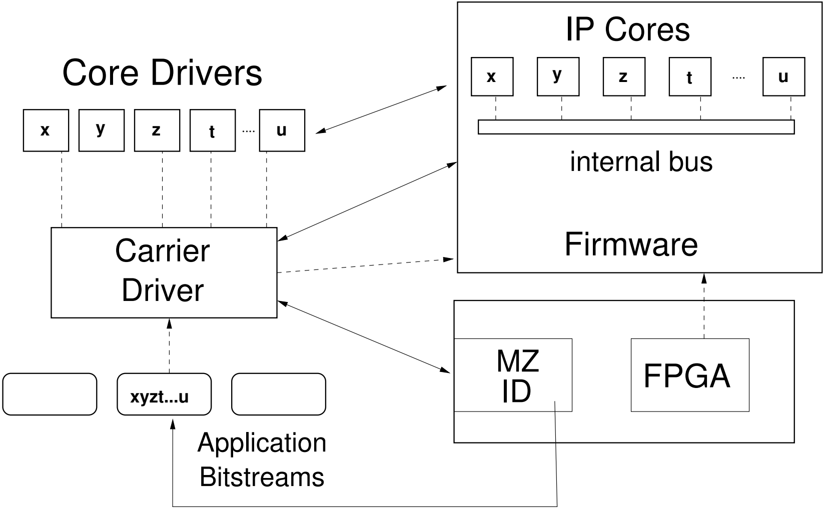


The FMC family of boards

This is a substantial part of our standard HW kit, currently under development (see `http://www.ohwr.org/projects/fmc-projects`).

- carriers in PCIe and VME format
- simple mezzanines with electronics for ADCs, DACs, DIO and endless other applications
- circuitry in the mezzanine
- FPGA application logic in the carrier
- *logic in the FPGA is organized as a set of IP cores interconnected through an internal bus named Wishbone*

Architecture of the FMC drivers



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It will be (we hope) the first Wishbone bus driver in the mainstream kernel ⇒ will to go upstream, timeliness

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Then `zio` comes

- Alessandro Rubini and Federico Vaga, main developers
- Integration mainstream *ab initio*
- See (soon) under `http://www.ohwr.org/`
- Clean design conforming to Linux kernel practice

Next candidates for (zio) integration

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- Tews TPCI200/TVME200 carries plus IPOCTAL serial boards
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- timing receivers, White Rabbit, etc.

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- Use of best practice and bleeding-edge tools selected by experienced programmers, *e.g.* `git`, `sparse` and `coccinelle`.