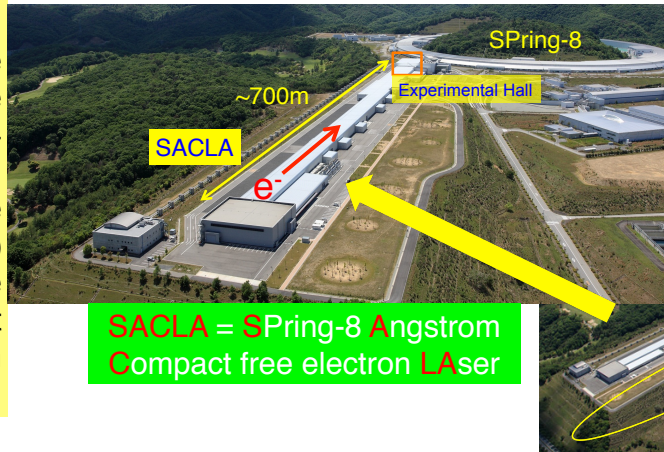icalepcs 2011

SPring·8 / SACLA

Development of Image Data Acquisition System for 2D Detector at SACLA (SPring-8 XFEL)

Akio Kiyomichi*, A. Amselem, T. Hirono, T. Ohata, R. Tanaka, M. Yamaga, JASRI/SPring-8, Sayo, Hyogo, Japan,
T. Hatsui, RIKEN/SPring-8, Sayo, Hyogo, Japan

We have developed a image data acquisition system for the X-ray and optical imaging devices at SACLA (SPring-8 Angstrom Compact free electron LAser). The frontends with the Camera Link interface transfer the data to data-handling servers, which buffer and distribute the data to on-line monitors and a high-speed storage.
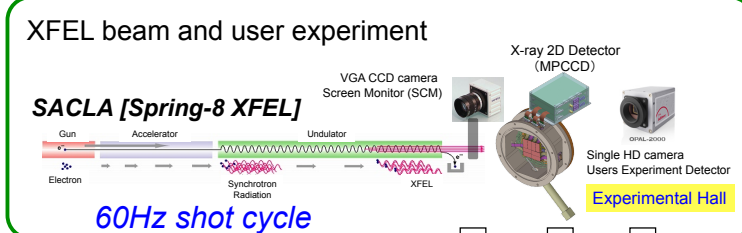In order to meet the requirements of proposed experiments to be performed at SACLA, Multi-Port Charge-Coupled Device (MPCCD) detector has been developed. The MPCCD sensor has 0.5 M pixels. The required bandwidth is 480Mbps each at a 60Hz shot cycle. In the first experimental runs, two arrayed detectors with 8 and 4 sensors in tandem will be the operation with maximum data rate reaching 5.8 Gbps.

SPring-8
~700m
Experimental Hall
SACLA
e⁻

SPring-8/SACLA Site View

SACLA = SPring-8 Angstrom Compact free electron LAser

XFEL FACILITIES

SPring-8

XFEL beam and user experiment

SACLA [Spring-8 XFEL]

Gun / Accelerator / Undulator

Electron / Synchrotron Radiation / XFEL

VGA CCD camera Screen Monitor (SCM)

X-ray 2D Detector (MPCCD)

Single HD camera
Users Experiment Detector

Experimental Hall

60Hz shot cycle

Camera Link Readout

Data-Handling Server
- Data transport from VME to storage
  - Receive the image data from VME Camera Link board via TCP/IP
  - Formatting a data structure
  - TCP/IP data transport service for Storage
- Basic analysis features for online data monitor
  - Averaging
  - Region-of-Interest statistical analysis
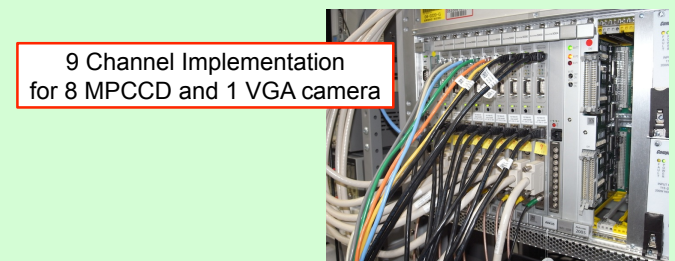 - Line profile calculation
  - Run user own analysis code

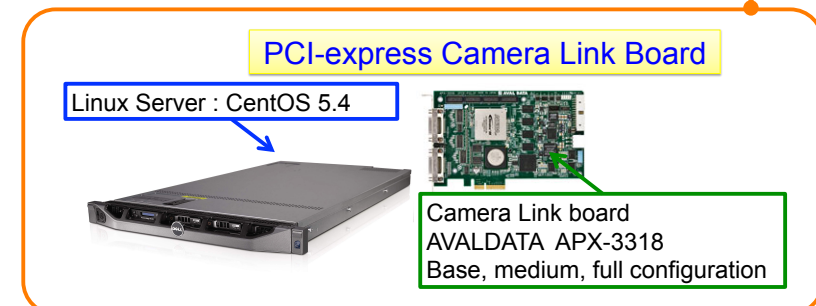## Schematic view and data flow of DAQ for SACLA

Online Data Monitor
DAQ Control

Supercomputer "K Computer"
10 Pflops 2012.4 ~

LiveView

Data-Handling Server

Users Experiment Detectors
Commercial camera

LiveView Control

Control

10 Gbps Ethernet

OPAL-2000

CameraLink

HD camera

To file server

Data stream 4 Gbps

10 Gbps Ethernet

Data file server   Data file server

PC Cluster
for data preprocessing
10 Tflops with high speed I/O

PCI-express Camera Link Board

VME CPU board

To data-handling server

High-Speed Storage

Frontend of Image Data Acquisition
Developed 2 type of Camera Link systems

- **VME CameraLink board**
  - **Custom made device**
  - **LossLess compression**
  - **Max data rate 760Mbps**
  - Flexible and logic-reconfigurable baseboard
  - CameraLink mezzanine card
 - Processor PMC card

9 Channel Implementation for 8 MPCCD and 1 VGA camera

MPCCD Octal sensors
512x1024 pixels 8 set

2048 pixels
2048 pixels

480Mbps/ch

PrPMC   FPGA Lossless compression

VME Camera Link Board

4.8 GB/sec/controller   8 GB/sec/controller

- **PCI-express CameraLink board**
  - **Commercially available device**
  - **Support various cameras**
  - PC Linux Server CentOS 5.4
  - AVALDATA APX-3318

VME CameraLink Board

ARKUS Axvme5000

Processor PMC:
Embedded Linux on PowerPC
Data Transfer via TCP/IP

PC Server

FPGA: Vertex5
LossLess Compression
Counting Frame Number

Detector

CameraLink Card:
Base configuration

Block Diagram of VME baseboard

IF Module
DSW x2   BPI Mode   Flash x2   RSW x2

CN1   TTL
FPGA1
- IF Control
- Calculation
- PPC

FPGA0
- VME IF

DIN Connector
VME A32/16MHz

CN2   PCI   PCI Bridge

Local Bus

Ethernet Controller

JTAG   JTAG

SD Card IF

JTAG Chain

RJ45   Trans   PHY   DDR2

COM   RS232c TR

Debug

Debug JTAG

Flexible and logic-reconfigurable VME board

PCI-express Camera Link Board

Linux Server : CentOS 5.4

Camera Link board
AVALDATA APX-3318
Base, medium, full configuration

Status of VME-based and PC-based Camera Link Data Acquisition

	VME system	PC system
No. of support cameras	2	>100
Supported Camera Link configuration	base only	base, medium, full
Camera clock	< 80MHz	< 85MHz
Loss-less compression	Yes	No
MADOCA control	Yes	Yes
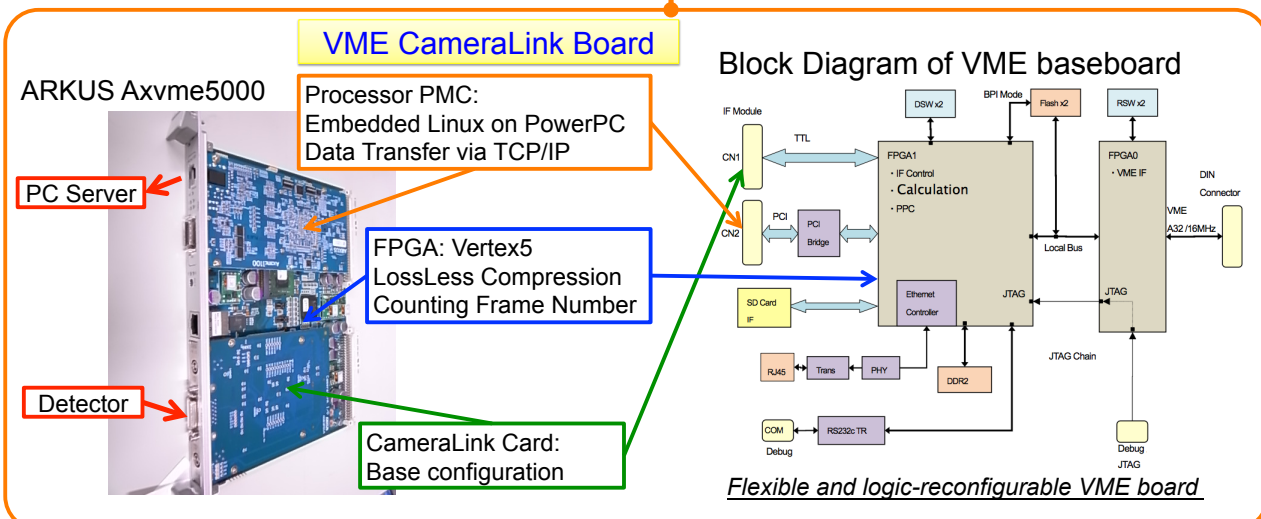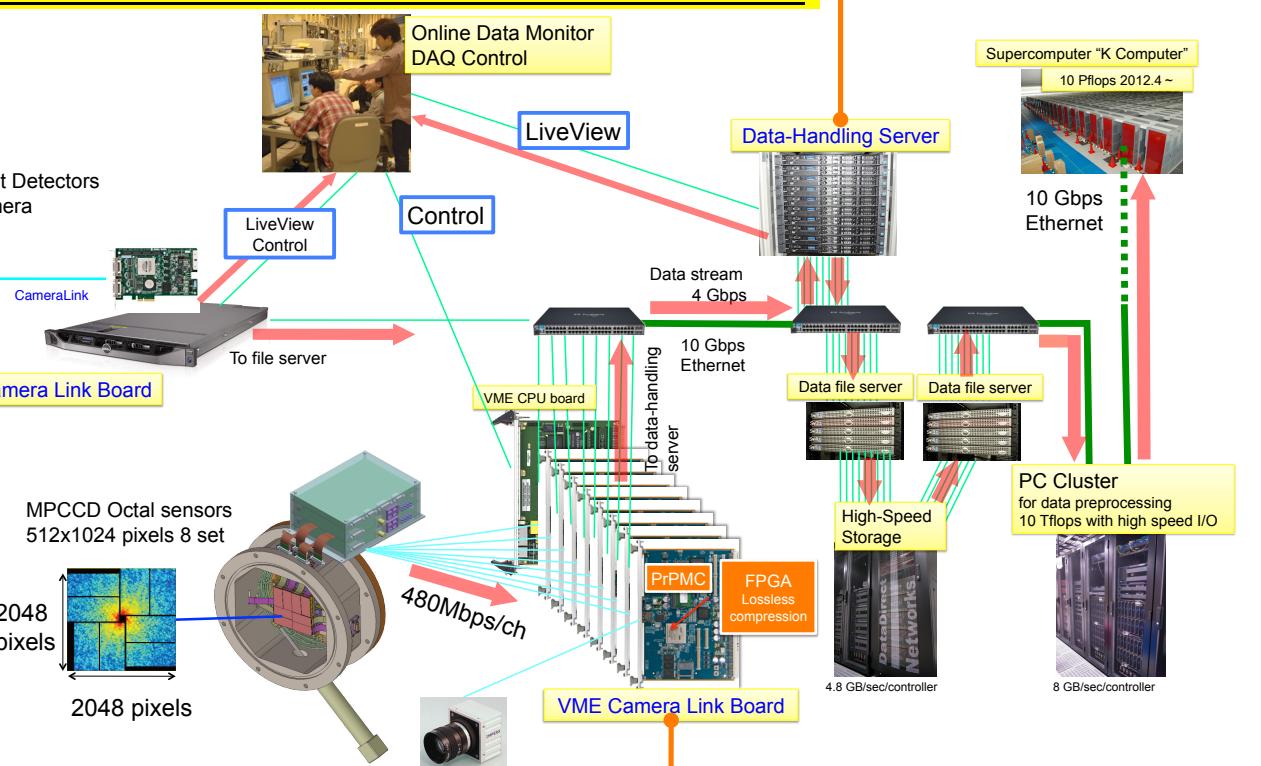
Summary:
 The image data acquisition system has been developed for the X-ray 2D detector and optical cameras at SACLA. We have developed a VME Camera Link board with FPGA. We demonstrated that the data transfer from the MPCCD detectors to the high-speed data storage at a transfer rate of 5.8 Gbps. The off-the-shelf PC-express Camera Link board was also implemented in the system in order to support wider range of camera.