A DIGITAL BASE-BAND RF CONTROL SYSTEM[*]

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Abstract

The analog RF control system of the S-DALINAC has been replaced by a new digital system. The new hardware consists of an RF module and an FPGA board that have been developed in-house. A self-developed CPU implemented in the FPGA executing the control algorithm allows to change the algorithm without time-consuming synthesis. Another micro-controller connects the FPGA board to a standard PC server via CAN bus. This connection is used to adjust control parameters as well as to send commands from the RF control system to the cavity tuner power supplies. The PC runs Linux and an EPICS IOC. The latter is connected to the CAN bus with a device support that uses the SocketCAN network stack included in recent Linux kernels making the IOC independent of the CAN controller hardware. A diagnostic server streams signals from the FPGAs to clients on the network. Clients used for diagnosis include a software oscilloscope as well as a software spectrum analyzer. The parameters of the controllers can be changed with Control System Studio.

We will present the architecture of the RF control system as well as the functionality of its components from a control system developers point of view.

INTRODUCTION

The S-DALINAC is an 130 MeV recirculating electron linac that is operated in CW mode. It uses superconducting niobium cavities at 2 K with a loaded Q of $3 \cdot 10^7$ for acceleration. Their 20 cell design and the high operating frequency of 3 GHz make them very susceptible for microphonics. In addition, superconducting 2 and 5 cell capture cavities, one of them supporting acceleration at velocities $\beta < 1$, are used inside the injector.

Furthermore, room-temperature chopper and buncher cavities are operated. A new polarized electron injector has been assembled in the accelerator hall [1]. Its bunching system consists of a chopper cavity and a 3 GHz as well as a 6 GHz harmonic buncher. Therefore the RF control system has to deal with different loaded quality factors (Q_L) ranging from some 5000 to $3 \cdot 10^7$ as well as with different operating frequencies.

The target specification for the stability of the accelerating field is an error in phase of $0.7°$ rms and a relative error in amplitude of $8 \cdot 10^{-5}$ rms. Since the old analog RF control system never achieved these values and became more and more unreliable it has been replaced by the new digital RF control system last year.

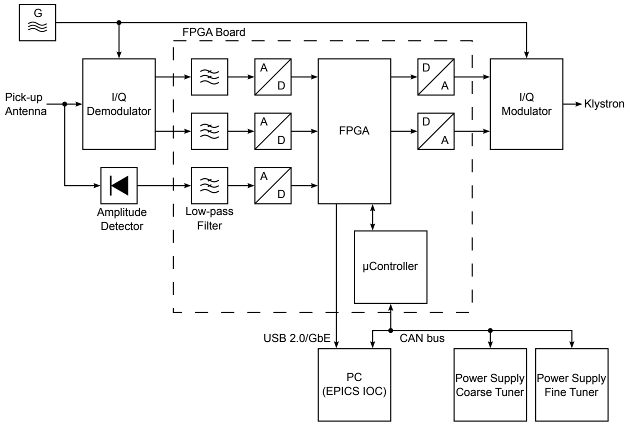

Figure 1: Overview over the hardware components of one channel of the RF control system.

CONTROLLER-BOARD HARDWARE

The RF control system converts the RF signals down to the base band. This allows to split the hardware into two parts: A frequency dependent RF board containing the I/Q (de)modulator and a frequency independent FPGA board processing the signals (see Fig. 1). All hardware components have been developed in-house. A separate power detector located on the RF board improves the accuracy of the magnitude measurement.

The analog signals are low-pass filtered on the FPGA board before they are digitized to avoid aliasing effects. The filters used for this purpose are third-order π filters with an edge frequency of $\approx$ 100 kHz. This filtering step is very important because the $19/20\,\pi$ mode of our 20 cell cavities is only separated by 700 kHz from the π mode used for acceleration. The chosen filter design ensures that the adjacent mode is suppressed by 55 dB while on the other hand the phase shift introduced by the filter is negligible for microphonic frequencies (up to 10 kHz).

High-linearity 18 bit ADCs are used to meet the specification in respect to accuracy. They run at their maximum sampling rate of 1 MS/s to keep the latency low and to allow the system to detect the signal of a detuned cavity operated in self-excited loop mode.

The FPGA used on the controller boards is a Xilinx Spartan 6 (XC6SLX45). Roughly 25% of its resources are used up to now leaving enough room for future extensions of the algorithm.

The requirements concerning the resolution of the DACs are not as high as for the ADCs. The DACs that are used on the FPGA board have a resolution of 16 bits and run with a frequency of 1 MS/s.

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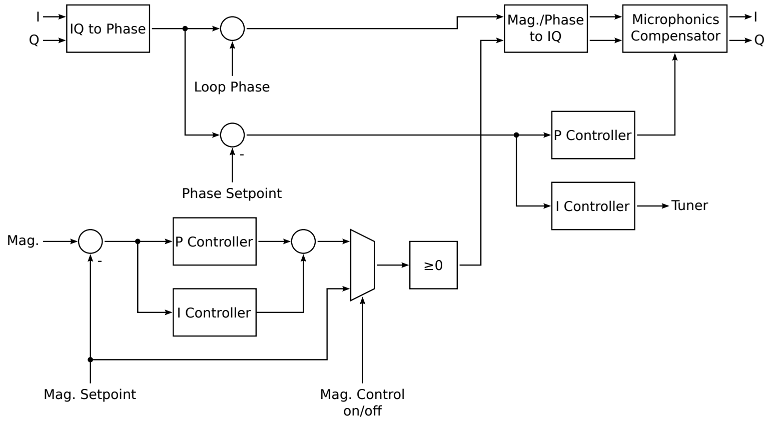


Figure 2: Simplified flow-chart of the self-excited loop control algorithm used with the superconducting cavities.

FPGA AND CONTROL ALGORITHM

The different Q_Ls of our cavities make different control algorithms necessary. The room-temperature copper resonators are operated with a generator-driven resonator (GDR) algorithm whereas for the superconducting cavities a self-excited loop (SEL) algorithm is better suited. Figure 2 shows a simplified flow-chart of the SEL control algorithm. In addition to simple operations like multiplication and adding operations it uses CORDIC blocks to transform from Cartesian coordinates (I and Q) to polar coordinates (magnitude and phase) and back [2]. For a more detailed description of the control algorithms see [3] and [4].

The control algorithm is implemented as a program for a self-developed soft CPU that is placed into the FPGA. The CPU is highly optimized for the implementation of RF control algorithms. Its arithmetic logic unit (ALU) uses 18 bit operands in order to fully exploit the accuracy of the ADCs. To keep things as simple as possible the instruction set is reduced to the operations needed for RF control algorithms. The CPU does not use complex memory access but only variable and parameter registers. Parameter registers are used for control parameters that are adjusted by the operator. They are read-only for the soft CPU but read/write for the micro-controller which connects the controller board to the PC. Variable registers used for intermediary results on the other hand are read-only for the micro-controller but read/write for the soft CPU. This concept together with a two-staged pipeline allows a high clock rate of 80 MHz. Complex operations like the conversion from Cartesian coordinates into polar coordinates and back are based on Xilinx CORDIC IP cores [5] that can be used from the CPU and that are pipelined as well (about 30 stages).

The CPU provides several 36 bit accumulating registers that can be used for the implementation of integral controllers. Only the 18 most significant bits are used for further processing but all 36 bits are considered for the accumulated sum. This allows integral controllers with time constants of roughly 1 s.

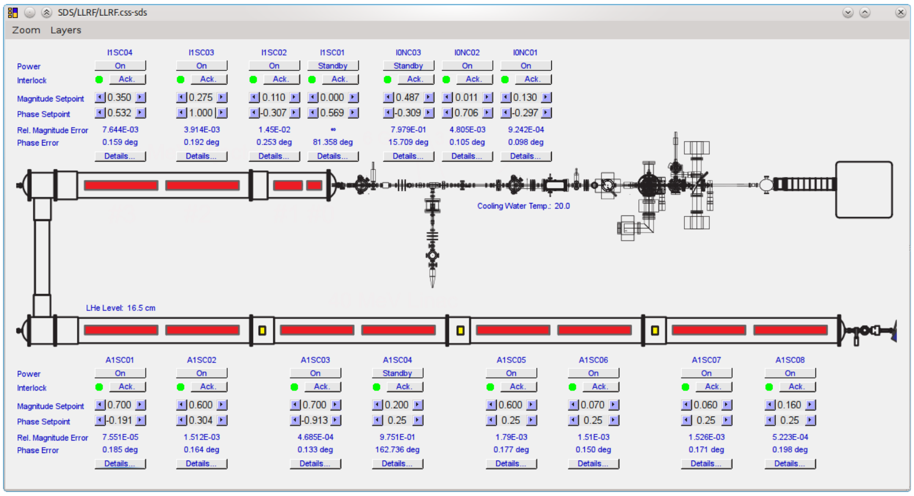
To avoid discontinuities all operations are available in a normal and a clipping variant. The latter clips the signal to the maximum/minimum 18 bit value if the result of an operation exceeds the range. The normal variant of the instructions is typically used for phase operations whereas the clipping variant is used for calculations with magnitude or I/Q values.

Using a soft CPU for the control algorithm has advantages in diagnostics because all variables (and thereby all intermediary results) are stored in fixed registers (block RAMs) where they can be read out easily. In particular there is no need for 18 bit data paths and huge multiplexers throughout the whole FPGA that would consume a great deal of the resources. In addition to this the soft CPU approach speeds up the development of the control algorithms. No time consuming synthesis of the Verilog code is necessary after the control algorithm has been changed. On the other hand the serial processing of the data reduces the performance. It turned out that for most practical purposes this penalty is small since the latency between ADC and DAC is determined mainly by the CORDIC blocks. The latency caused by the complete control algorithm is approximately 1 μs.

SLOW CONTROL

The controller boards are connected to a standard PC server via CAN bus. This interface is used to monitor and adjust all slowly varying (e. g. by user interaction) parameters of the control algorithm and the hardware. The micro-controller that connects the FPGA boards to the CAN bus runs Nut/OS, an open source real-time operating system providing cooperative multi-threading [6]. In addition to communicating with the PC it sends commands directly to the fine and coarse tuner power supplies via CAN bus. A three-step controller implemented in the micro-controller activates the motor tuner if the fine tuner approaches its limits.

The PC runs Linux and an EPICS IOC that is hooked up to the CAN bus via a device support that uses the SocketCAN network stack included in recent Linux kernels (since 2.6.25) [7]. SocketCAN provides access to the CAN bus



	I1SC04	I1SC03	I1SC02	I1SC01	I0NC03	I0NC02	I0NC01
Power	On	On	On	Standby	Standby	On	On
Interlock	● Ack.	● Ack.	● Ack.	● Ack.	● Ack.	● Ack.	● Ack.
Magnitude Setpoint	0.350	0.275	0.110	0.000	0.487	0.011	0.130
Phase Setpoint	0.532	1.000	-0.307	0.569	-0.309	0.706	-0.297
Rel. Magnitude Error	7.644E-03	3.914E-03	1.45E-02	∞	7.979E-01	4.805E-03	9.242E-04
Phase Error	0.159 deg	0.192 deg	0.253 deg	81.358 deg	15.709 deg	0.105 deg	0.098 deg
	Details...	Details...	Details...	Details...	Details...	Details...	Details...

	A1SC01	A1SC02	A1SC03	A1SC04	A1SC05	A1SC06	A1SC07	A1SC08
Power	On	On	On	Standby	On	On	On	On
Interlock	● Ack.	● Ack.	● Ack.	● Ack.	● Ack.	● Ack.	● Ack.	● Ack.
Magnitude Setpoint	0.700	0.600	0.700	0.200	0.600	0.070	0.060	0.160
Phase Setpoint	-0.191	0.304	-0.913	0.25	0.25	0.25	0.25	0.25
Rel. Magnitude Error	7.551E-05	1.512E-03	4.685E-04	9.751E-01	1.79E-03	1.51E-03	1.526E-03	5.223E-04
Phase Error	0.185 deg	0.164 deg	0.133 deg	162.736 deg	0.177 deg	0.150 deg	0.171 deg	0.198 deg
	Details...	Details...	Details...	Details...	Details...	Details...	Details...	Details...

Figure 3: Screenshot of the main display of the RF control system's operator interface. It only provides the most frequently used controls and links to further displays for details.

via network devices (BSD sockets) which can be accessed by multiple applications at the same time (e. g. the IOC and a CAN sniffer). Furthermore it acts as an abstraction layer that makes the device support independent of a specific CAN card or hardware vendor (all CAN cards having a SocketCAN driver are supported).

All together the IOC provides several thousand records for all 16 RF channels. A great deal of them is related to diagnostics.

The operator interface has been implemented with Synoptic Display Studio [8]. Figure 3 shows a screenshot of a display providing an overview over all control loops and their most important controls. Further controls are available on control algorithm specific displays that contain all parameters for the selected controller.

DIAGNOSTICS

The FPGA boards provide fast diagnostic data via USB 2.0. Eight signals with a resolution of 16 bits are continuously transferred into the PC with the full sampling rate of 1 MS/s. The two least significant bits of the full 18 bit result are available as separate channels.

During operation eight controller boards are plugged into a crate together with a concentrator card. The concentrator card uses an FPGA to collect the data from the controller boards and streams the selected signals to the PC over its own USB 2.0 interface (cp. Fig. 4). Two crates can be coupled over a parallel LVDS interface. In this configuration one concentrator module acts as master and the other as slave. Signals from different controller boards and crates can be transferred at the same time.

In addition to the eight channels with full sampling rate the master concentrator card provides a stream of all 64 signals of all 16 controller boards on a second USB 2.0 interface. This data is transferred with a reduced sampling rate of 2 kHz and is intended for monitoring. Both USB data streams end at the PC where the IOC reads the data via a specially developed device support.

The data streams are forwarded by the diagnostic server process to the connected clients via TCP connections. Typical client applications include a software oscilloscope [9] that has been extended with a data source plug-in that reads data over the network from the IOC as well as a software spectrum analyzer [10]. Data recording is possible with standard Unix tools (e. g. netcat).

In addition to forwarding the stream of data the slow data stream is fed into EPICS records by the device support. It provides mean values of all signals every 0.1 s which can be used for monitoring.

Those values can be used to detect if a controller is out of lock but they do not provide precise information about the performance of the cavity and its controller. Even the oscilloscope view of the fast streaming data is not very helpful because it is difficult to see small changes in a noisy signal. A much more meaningful measure for the errors of the field in the cavity are the RMS errors of the magnitude and phase error signals. They could be calculated from the fast streaming data at the PC but this would be possible only for four cavities even if all eight diagnostic channels are sacrificed for this purpose. To cover all cavities while keeping the diagnostic channels free for the operator the RMS calculation has been moved partly into the FPGAs of the controller boards. They have the whole data stream available and can relieve the PC from processing work by carrying out the most time-consuming part of the calculation. The FPGAs calculate the square of the signals for each ADC sample and sum 2^{17} of them up which corresponds to a time of roughly 0.1 s. The result is transferred to the PC via CAN bus. The EPICS IOC calculates the square root of the sums and scales the values to finally get an error in degrees or a relative error in case of the magnitude respectively.

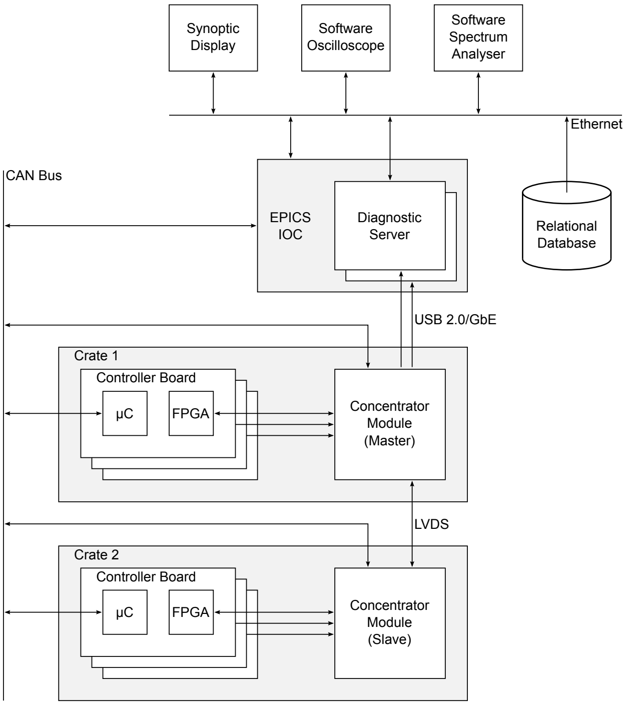


Figure 4: Data flow between controller boards, concentrator modules, diagnostic server and clients.

SOFTWARE AND FIRMWARE DEPLOYMENT

The RF control system has been put into operation as soon as the major components allowed stable operation. A lot of bug fixes and new features have been integrated since then. It turned out that the concept of continuous integration works best for us. It requires to recompile and deploy the software to the PC server and firmware to the micro-controllers and FPGAs frequently and – most important – in a repeatable fashion. This has been achieved by using the Debian Fully Automatic Installation (FAI) [11] to setup the PC server over the network. A virtual machine is used for testing to make sure all packages are installed cleanly before the production machine is reinstalled. To speed up the installation some software components are automatically build by a build server and distributed as Debian packages. This way changes can be deployed to the test or the production system within minutes. A complete installation of the server takes about 10 minutes. This means that downtimes of the accelerator of half an hour can be used to upgrade the complete RF control software. Updates of the IOC are possible even during operation because the controller boards run completely independent of the PC.

The IOC configuration is generated automatically from a relational database and a set of templates during installation. This way we can recover quickly from a broken PC without the need to hold completely installed and configured spare hardware available. Instead one spare machine is sufficient for all PCs running IOCs.

The micro-controller firmware images of the FPGA boards and the tuner power supplies can be updated via CAN bus. A boot loader makes it possible to recover from broken firmware images without physical access to the JTAG chain. The configuration of the FPGAs can be written using the same technique. A multi-boot functionality provides a fall-back to a second “golden” image for the FPGA in case of a broken primary bitstream [12].

These measures together with revision control of all components make a significant contribution to reduce the downtime of the RF control system.

SUMMARY

The digital RF control system is based on in-house developed hardware giving us full control over every detail. The soft CPU that has been implemented in the FPGA allows fast and flexible modification of the control algorithm on one hand and powerful diagnostics on the other hand. The availability of extensive diagnostics has proven to be a considerable precondition for the smooth commissioning of a new RF control system.

A highly automatized deployment of all parts of the software and configuration allows a fast integration of further improvements into the production system.

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