SYSTEM INTEGRATION OF SwissFEL BEAM LOSS MONITORS

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Abstract

Scintillator-based Beam Loss Monitors will be used at SwissFEL for monitoring the losses, for optimizing beam conditioning, beam measurements with the wire-scanner and Undulator protection. The optical signals from the scintillators will be detected by PMTs which are located outside the accelerator tunnel. The PMT control and signal conditioning is done via a front-end based on the PSI Analogue Carrier board (PAC). The PAC board allows for amplification/attenuation, offsetting and single-ended to differential conversion of the analog signal, while the Generic PSI Carrier (GPAC) board provides digitization and FPGA-based post-processing, along with bridging the communication to EPICs controls. A fast algorithm was developed to process the signals and trigger the machine protection system (MPS) at 100Hz. The system integration of the BLMs will be discussed in this paper.

INTRODUCTION

In SwissFEL, scintillator screens and wire scanners will be used to monitor the electron beam in the charge range 10 - 200 pC and in the energy range 0.007 - 5.8 GeV. In particular, wire-scanner will be used to resolve the 28 ns time structure of a 100 Hz, two-bunches train [1, 2]. Losses caused during beam conditioning and wire-scanner insertions can travel for tens of meters in the machine. Loss monitors have been designed to track these losses for emittance measurements and to prevent radiation-induced demagnetization of the Undulators.

The beam loss monitor systems have been developed based on the following system requirements to detect losses before an appreciable loss level is reached.

Table 1: Beam Loss Monitor Specifications

Parameters	Specifications	Purpose
Charge range	10 - 200 pC	Full beam loss
Minimum detection	0.1 pC	Wire-scanner measurements
Repetition rate	100 Hz	2-bunch resolving capability, shot-to-shot
Machine protection system	Yes	Beam synchro-nous DAQ

There are a total of 48 BLMs, which will be located at fixed distances with respect to the wire-scanner for slice emittance measurements, and between Undulator segments to monitor the losses reaching at these locations. The BLMs will be interfaced to the machine protection system (MPS), leading to either a beam suppression in the machine or to immediately act on the laser shutter.

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DETECTORS

The BLMs consist of organic scintillator fibers (BCF12, Saint Gobain), which are then connected to clear duplex plastic optical fibers (POF, Avago Tech) that propagate the scintillator's output light from the accelerator into the technical gallery where the light detectors are located. One of the POFs is optically mated to a PMT (Hamamatsu H10720) [3] and the other to a pulsed light emitting diode (Avago Technologies HFBR-1505AZ/2505AZ) [4]. The LED provides a system-live check and observation of light transmission through the connected fibers for radiation damage, during or outside of beam operation.

DAQ SYSTEM OVERVIEW

The PMTs and preamplifiers, which convert the PMT charge pulse into a time-shaped voltage signal, are mounted on the signal conditioning board called the PSI Analog Carrier (PAC) board. All controls of the PMT, preamplifier and LED voltages, and output signal conditioning is done by the PAC. The output signals are digitized and processed with the Generic PSI Carrier (GPAC) board, which was developed at PSI for application in multiple accelerators (European XFEL, SwissFEL and SLS) [5].

PAC Board

Up to four mezzanine-boards, 2 channels per board may be plugged to the PAC carrier board. Each mezzanine board supports one PMT signal conditioning electronic. This means that a single PAC board can house and control 4 BLMs. All mezzanine boards connectors provides low noise standard linear supply voltages (±12 VDC / ±5 VDC and +3.3 VDC), eight remotely controlled DC voltage supplies, eight general purpose digital controls/status signals and four differential digital I/O signals covering a large spectrum of requests. To avoid digital noise production on sensitive signals, the digital control (Oscillators, FPGA) can be set to standby mode when not in use.

The PAC board communicates with remote systems controls over a serial connection, either through specific user I/O on the VME-P2 connector or over a standard RJ45 network connector located on the front panel for

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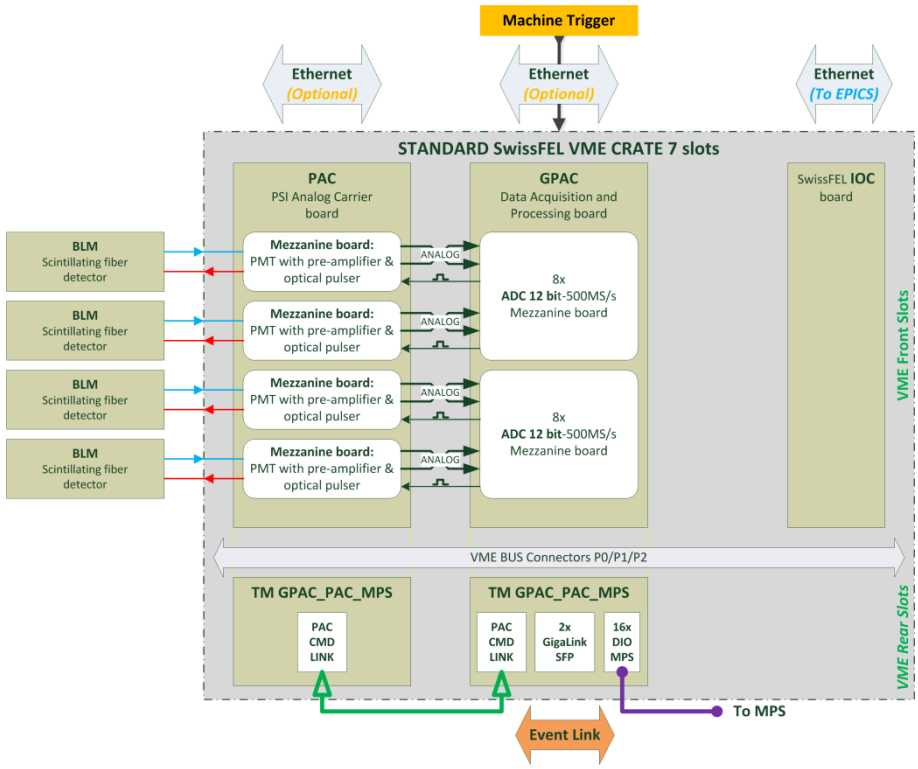

Figure 1: Sketch of the Beam Loss Monitor (BLM) electronic crate overview.

standalone applications. The PAC board supports live insertion.

Analog-to-Digital Conversion

The SwissFEL BLMs use an ADC board originally developed for the European XFEL button BPM system [5]. The ADC board, implemented as mezzanine module for the GPAC, has eight 12-bit 500 MSa/s ADCs (Intersil KAD5512P-50). We plan to interleave up to two/four of such channels for increased resolution, with a 180°/90° degree delay. This delay on the raw signal is introduced digitally with the LMK01020 [6] clock distribution chip on the ADC mezzanine.

The ADC sampling clock is provided externally by the reference distribution system. Differential signalling and coaxial cables are used for the connections to and from the PAC.

Digital Backend

The digital backend consist of one GPAC board and two ADC mezzanine cards as a generic digital platform, as described in [5, 7].

The System (SYS) FPGA handles communication of the GPAC with the machine control system and timing system, via VME bus or SFP fibre optic link. Over VME, the GPAC communicates to the IOC board, responsible for EPICs record processing, as well as linking with the machine network. The digital processing of the ADC signals is done in the two FPGAs (a.k.a. BPM FPGA, Xilinx Virtex-5 [8]), where the signal processing of the mezzanine ADC signals is done in firmware/software (see "Firmware" section). The FPGA provides interfacing via backplane transition modules to the PAC board, over a differential protocol ("FastLink") running at a clock frequency of 12.5 MHz.

In addition, the GPAC has a so-called backplane (BP) FPGA for controlling slower IOs of front-end electronics via user defined IOs, as well as two FPGAs (CONFIG and SEU) for board and power management. Thanks to the generic firmware/software framework, only part of the BPM and BP FPGA firmware on the GPAC is application-dependent, thus reducing the development effort for new applications and monitors.

Transition Modules

The GPAC will connect to the SwissFEL BLM-Electronics, SwissFEL Machine Protection System (MPS) and SwissFEL event recording system via a transition board mounted on the rear side of a SwissFEL standard VME crate. Communication to the event generating system is achieved by GBit/s optical links connected to the GPAC-VME J0/P0 connector via SFP-modules, while MPS and BLM electronics use the user defined pins of the GPAC-J2/P2 for controls [9].

Triggering

The embedded event receiver consists of a generic IP core capable of decoding the SwissFEL event distribution system [7]. This core is located on the GPAC and connected to the main event generator via optical fiber, using a front-end SFP+ connector on the GPAC. This event is routed to the BPM FPGA, where the appropriate samples from the ADCs are captured and processed.

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This solution has been preferred over the VME-EVR-230 card from Micro Research [10]. Even though it has a jitter of 5ps which is adequate for the needs of the BLM, an integrated event decoder has been preferred for cost-saving reasons.

I/O Controller

Data and statistics obtained at 100 Hz are transmitted through EPICS to the IOC, based on an IFC1210 board from IOxOS [11]. There raw digitized signals and processed results are transmitted to the archiver for both short and long term storage. Control consoles access these records over EPICS, although at a much lower refreshing rate (~5Hz).

SIGNAL PROCESSING

Firmware

The BLM-specific part of the firmware was implemented on the BPM (Virtex-5 FX70T) and BP (Spartan3A) FPGA. Another FPGA (Spartan3A) is located on the PAC board, with a serial protocol to the BP FPGA on GPAC for control of PAC board settings like gain, offset, etc.

The data processing on the BPM FPGA consists of data reception, triggering, buffering and relevant parameter extraction (discussed in the next sections). This is done in real time for every SwissFEL bunch, been able to process a full vector of 4k samples at 100Hz. Raw data is not discarded, it is transferred to the IOC for archiving and for off-line analysis.

On the PAC, a System-on-Chip (SoC) design based on a Microblaze processor has been implemented on its Spartan 3 FPGA. The PAC may receive commands from the GPAC over the FastLink connector or work autonomously, accessed over a XT-Nano-XXL chip [12]. This flexible communication component converts TCP/IP packets to a Serial RS232 format, which is then connected to the PLB bus using an UART core as bridge. Another IP Core interfaces with the 8 DAC available on the PAC via an SPI Bus. Voltage values and operating ranges can be set from EPICS or over the XT-Nano interface.

The PAC board has four slots for extension for detector-specific mezzanine cards. Each mezzanine interface includes eight analogue outputs from two DAC devices, generic lines for SPI/I^{2}C communication and power. This configuration allows for expansion and modularity, highly desirable features in projects of such complexity as the Beam Loss Monitors. By means of an I^{2}C access, an identifier can be read for identifying which mezzanine board has been mounted on the PAC.

Firmware/Software Implementation

The digitized waveforms are processed to determine the pulse integral (see Fig. 2). First a number of samples are picked just before the pulse signals and averaged to give the "baseline" value. Baseline is calculated anew for each bunch.

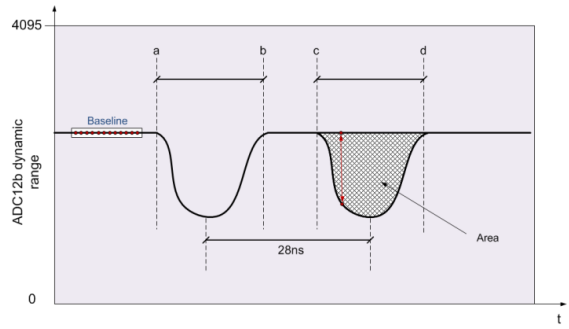

Figure 2: Schematic of the pulse integration.

Then, the regions of interest – sample numbers for the beginning and end of a pulse - are determined by the operator of these monitors. The reason behind this approach is to decouple the two pulses from each other for various locations of the BLMs in the machine, as some variations are to be expected. Region-Of-Interest (ROIs) can be configured over EPICS for double-bunch distinction. The samples in the ROI are summed and the baseline is subtracted. The behaviour of the integral area (shown in Fig. 2) of each pulse is tracked for loss measurements. The value obtained is compared to three thresholds. Two correspond with the MPS alarm levels and a third for device saturation. All three are calculated in <1ms on a per-bunch basis.

Once raw data has been processed, and interrupt to the VME Bust/IOC triggers data fetching from the FIFO on the IP Core to the corresponding waveform record. VME Burst transfers (MBLT, 2eSST) are enabled to support the necessary bandwidth.

MPS Algorithm

The SwissFEL machine protection system (MPS) collects alarms from a variety of monitor systems. Each monitor can generate two types of alarms: level 1 alarm, where no further electron bunches are generated by shifting the radiofrequency (RF) in the gun in order to obtain a timing where no laser is present, and a more severe level 2 alarm, where the RF for the entire machine is turned off.

The calculations are performed at a rate of 100 Hz, independent of the bunch repetition rate of the machine.

1. Determination of monitor reading that enters the calculation (S_0)
2. In case there is no beam measured during the current RF pulse: $S_{calc} = S_0$
3. In case the monitor reading S is saturated: $S_{calc} = S_{sat}$ .S
4. Otherwise: $S_{calc} = S$
5. Filtered error signal is calculated
6. Generation of alarms (level 1 or 2) by comparing the filtered signal to the alarm thresholds

Once an alarm is generated, it remains active until its condition is not fulfilled anymore.

For the FPGA implementation, there are four vectors of interest: the integral values extracted from ADC samples

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(S_n), the previously calculated average (avg_n) and the two threshold vectors (one per alarm level).

The proposed formula for alarm level calculation is:

$$\frac{1}{2K}\left(avg_n \cdot (K-1) + S_n\right) \quad (1)$$

K is a factor for weighted average. A diagram of the algorithm is shown in Fig. 3.

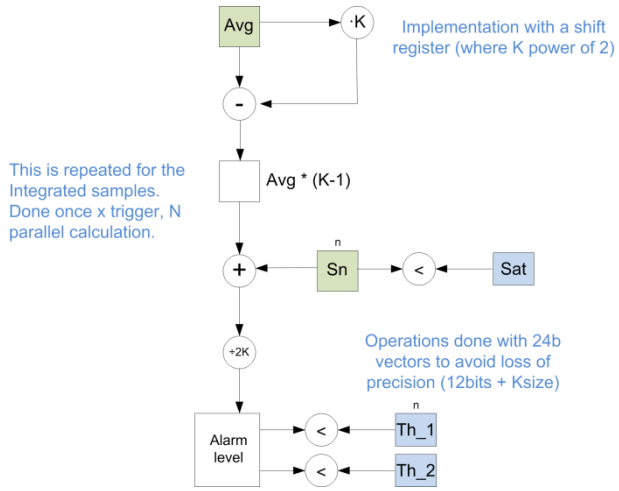

Figure 3: Flow diagram of the MPS algorithm.

This is essentially a low-pass filter which reacts inversely to the number of previous average values calculated (K). This smooths out alarm generation while eliminating spurious alarms (Fig. 4). Divisions and multiplications on the FPGA are implemented with shift registers, which speeds processing while reducing resource use. Hence, K must be a power of two.

Automatic Gain Adjustment

This is where the PMT gain voltage is changed on the PAC board to avoid saturating both the ADC input and the PMT. Each digitized pulse is compared to the saturation threshold. The GPAC issues a command to reduce the PMT control voltage to avoid saturation effect and hence, inaccurate loss measurements. If despite gain reduction the PMTs and/or ADCs are saturated, the machine protection system will trigger Alarm level 2 and prevent beam travelling through the machine.

CONCLUSION

We have presented the DAQ system for the SwissFEL Beam Loss Monitors, which has been designed profiting to a large extent from a generic diagnostics hardware concept. All in all, 48 BLMs will be installed, making it one of the critical instruments for the protections of the accelerator.

Signals obtained from the scintillator fibers are sent to a modular analog front end for signal conditioning before being digitized with 12 bit, 500 MSa/s ADCs. Data is processed in real time on a FPGA, where a specific algorithm compares loss levels to a set threshold and raises the corresponding alarms in case machine protection must be triggered. The DAQ system enables processing at 100 Hz rate and thus, generating an interlock which is fast enough to prevent machine damages.

The firmware for the PAC and GPAC boards have been implemented and tested with realistic input, obtaining satisfactory results. PAC has proven to successfully communicate with the GPAC and the EPICS control system via an IFC1210 IOC.

Further tests of the complete system are ongoing to verify the stable function of the instrument, together with the feasibility of using BLMs as readout for wire-scanner beam profile measurements. This is imperative for accurate emittance measurements. Moreover,

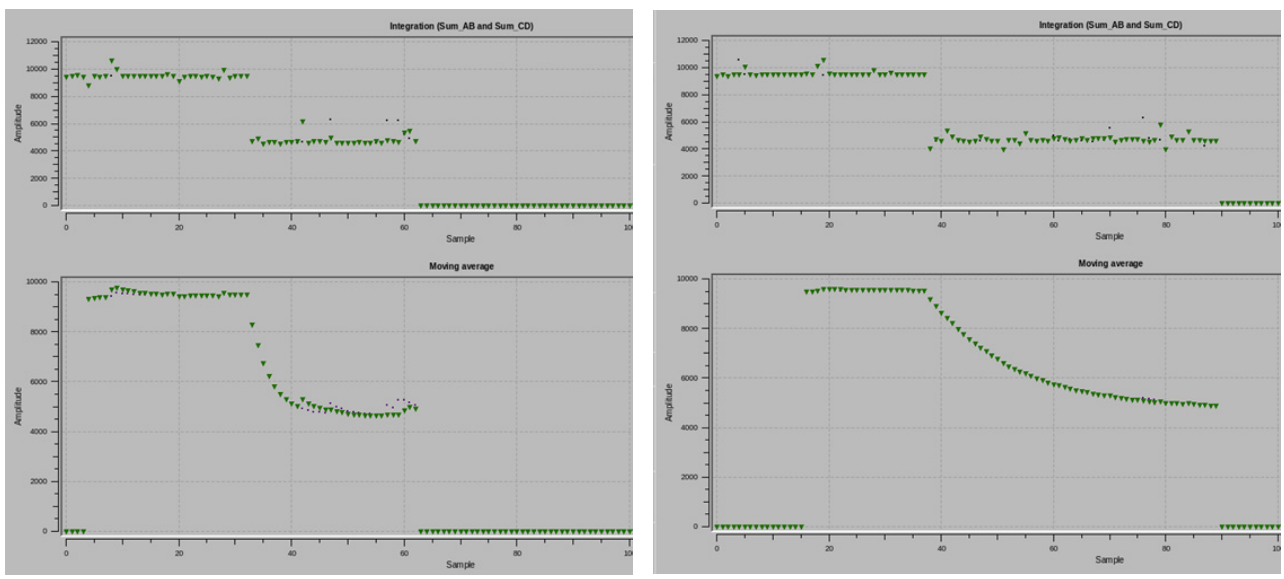

Figure 4: Results of the algorithm implementation shown for two values of K. The algorithm acts as a low pass filter (bottom plot) and removes noise from the shot-to-shot changes of the integrated signals (top plot). The filtered signal is used for triggering the MPS.

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implementation has been successfully completed for the Longitudinal Loss Monitors, where the position of the losses can be determined to within 1 m. Each sample of the digitized output is information relevant for the MPS computation, which means about 2000 computations at 100 Hz.

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REFERENCES

[1] R. Ischebeck et. al., "Overview of beam instrumentation activites for SwissFEL", MOPF31, Proceedings of IBIC2014, Monterey, USA (2014)
[2] G.L. Orlandi et. al., "Design and test of wire-scanners for SwissFEL", THP091, Proceedings of FEL2014 Basel, Switzerland (2014).
[3] Hamamatsu photonics, Solothurn, Switzerland.
[4] Acal Bfi, Groebenzell, Germany.
[5] B. Keil et. al. "A generic BPM electronic platform for European XFEL, SwissFEL and SLS", MOCB02, Proceedings of IBIC2012, Tsukuba, Japan (2012)
[6] Texas Instruments: http://www.ti.com/product/lmk01020
[7] W. Koprek et. al. "Overview of Applications and Synergies of a Generic FPGA-Based Beam Diagnostics Electronics Platform at SwissFEL", these proceedings, IBIC 2015, Melbourne, Australia (2015).
[8] Xilinx/Avnet website: http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
[9] P. Pollet, Transition modules, Private communication
[10] IOXOS website: http://www.ioxos.ch/index.php?option=com_content&view=article&id=136&Itemid=113
[11] Micro Research website: http://www.mrf.fi/index.php/vme-products/76-vme-event-receiver-wo-rf-vme-evr-230
[12] AK-NORD, XT-Nano-XXL website: http://www.ak-nord.de/ak/product_info.php?products_id=33&language=en

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