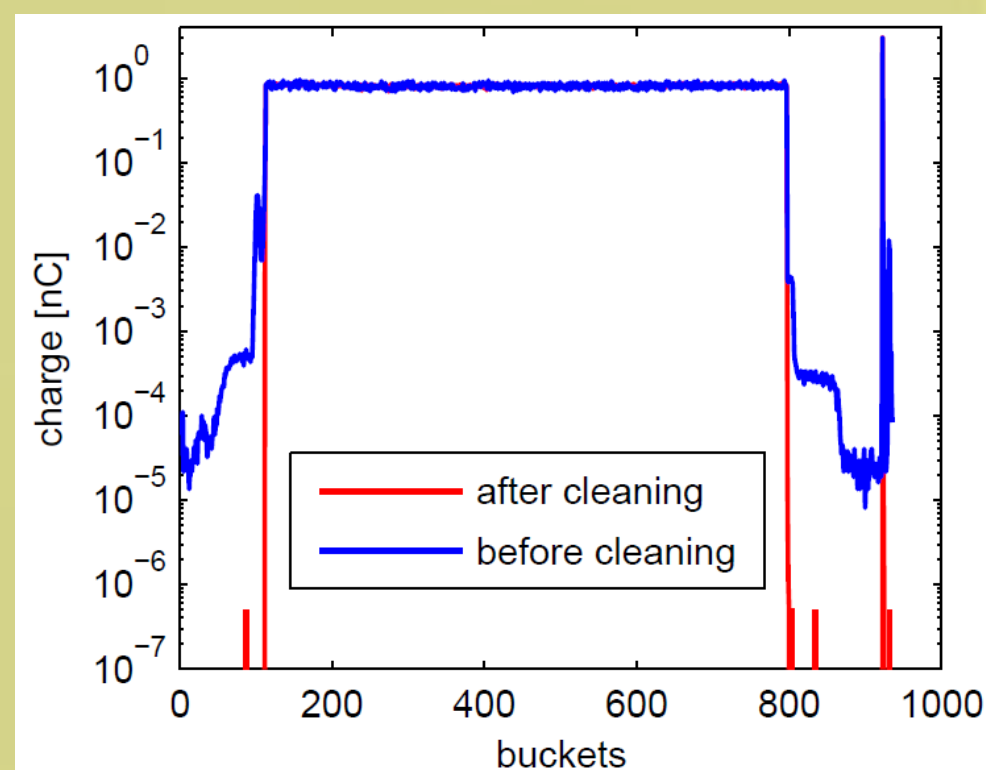
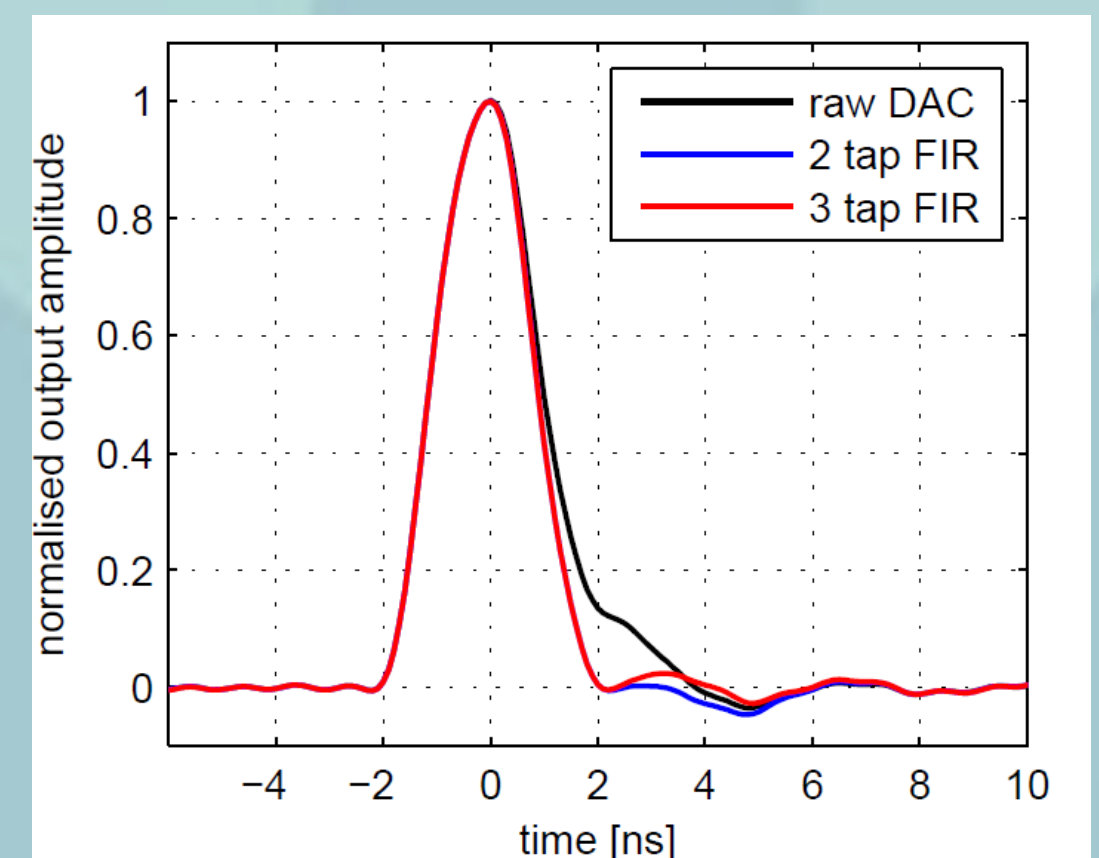


G. Rehm, M. Abbott, A.F.D. Morgan, Diamond Light Source, Oxfordshire, U.K.

[illegible]

DAC pre-emphasis to adjust impulse response using scope



ADC data statistics (on CS03R-CS-SERV-02.pri.diamond.ac.uk)

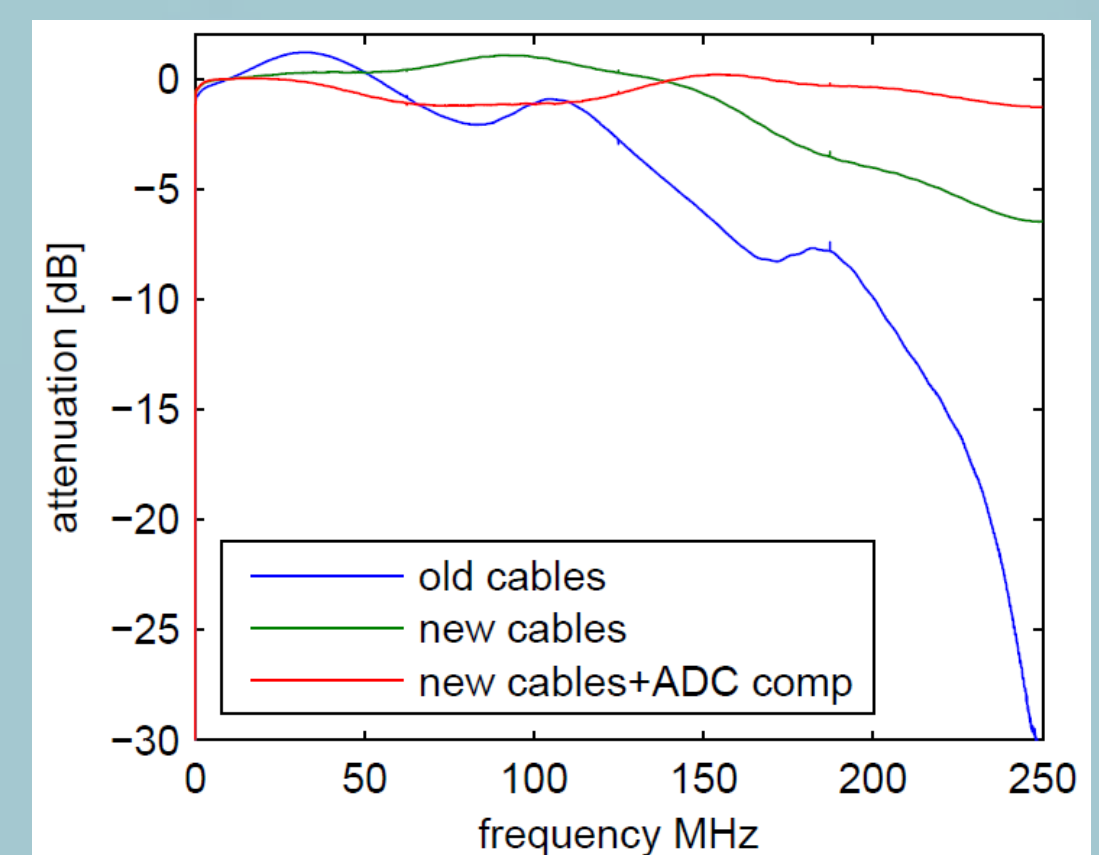
SR23C-DI-TMBF-01 ADC Setup

ADC Compensation Filter

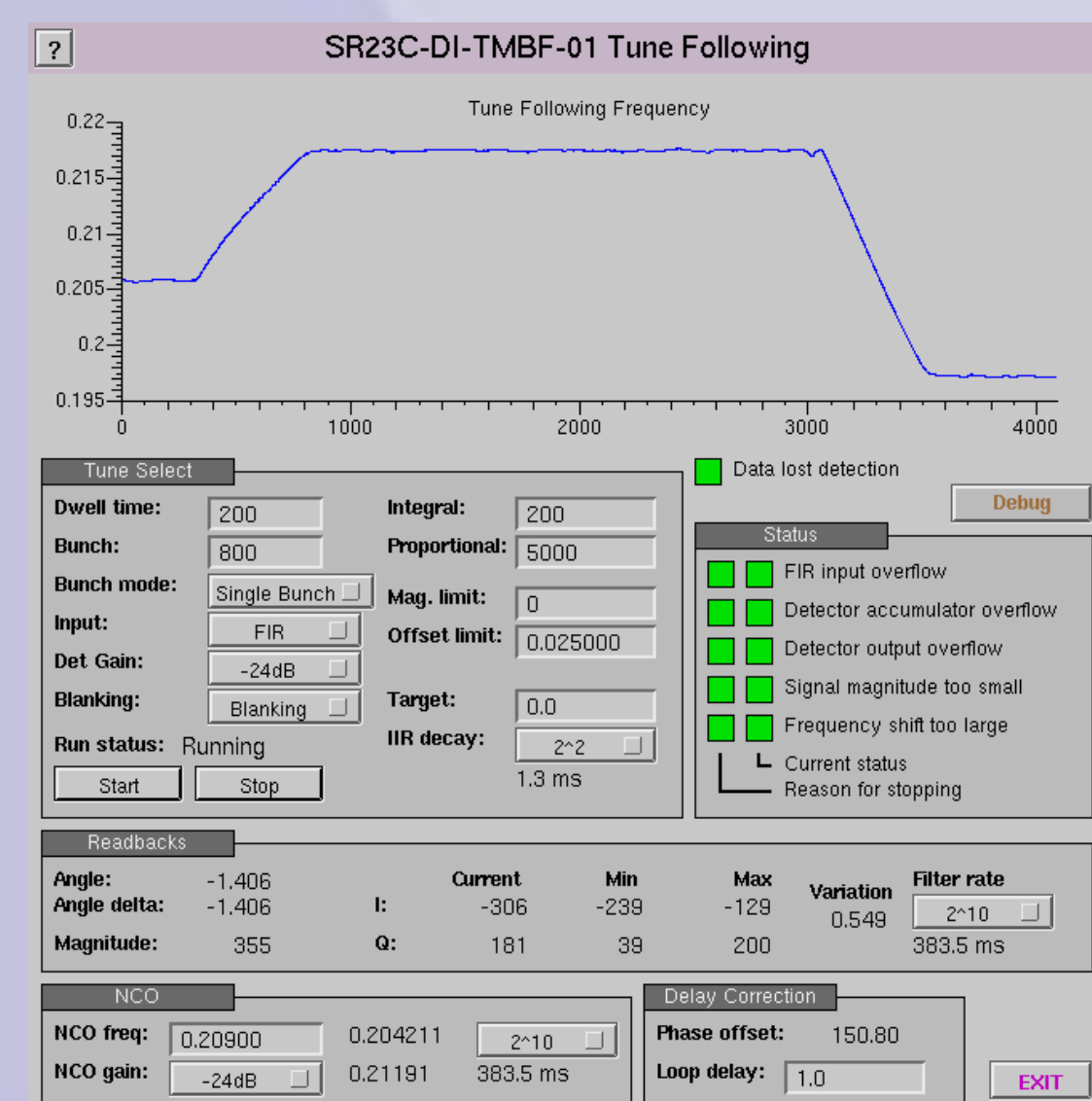
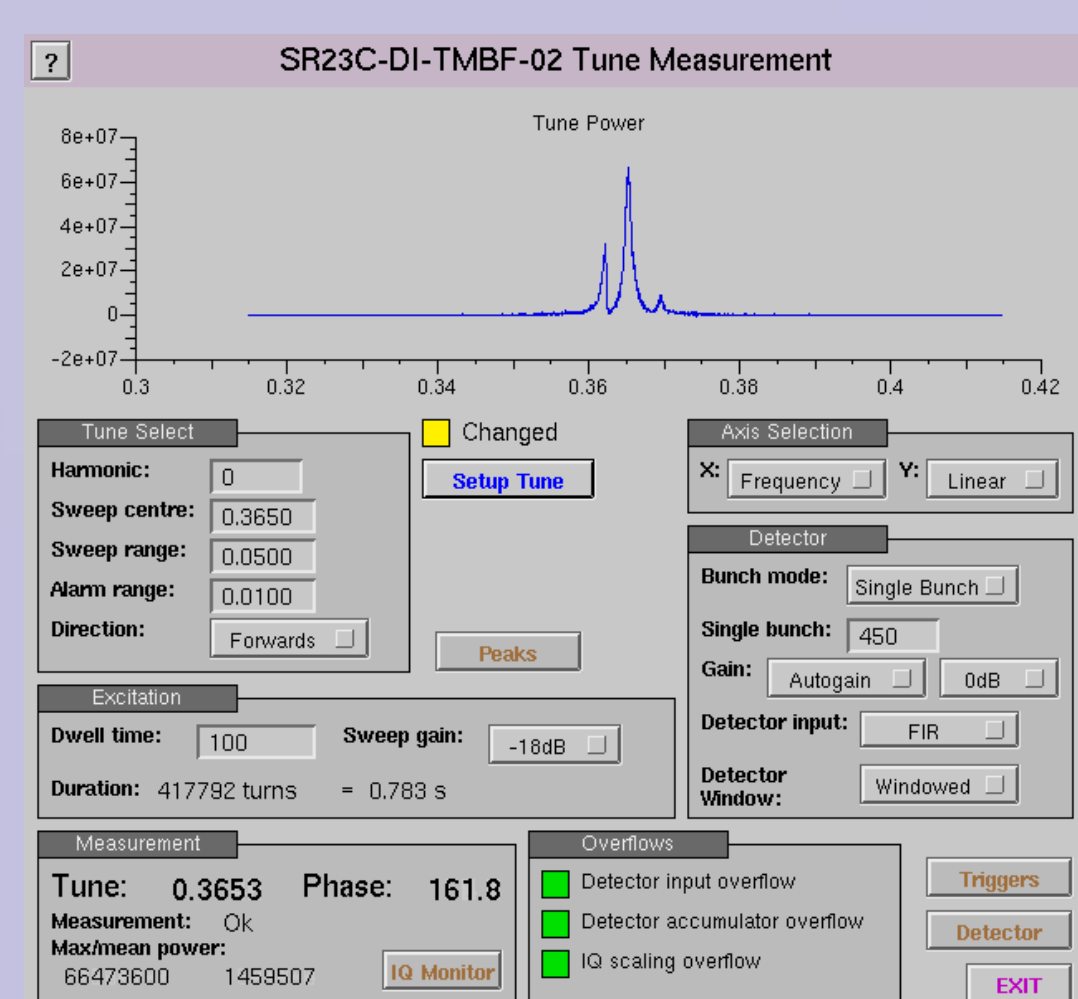
Group delay: 0 ns

ADC Offsets

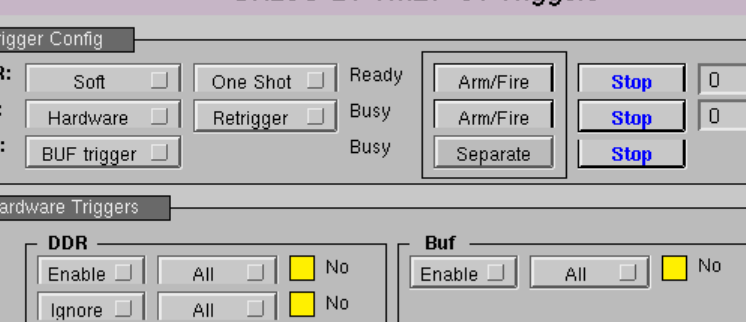
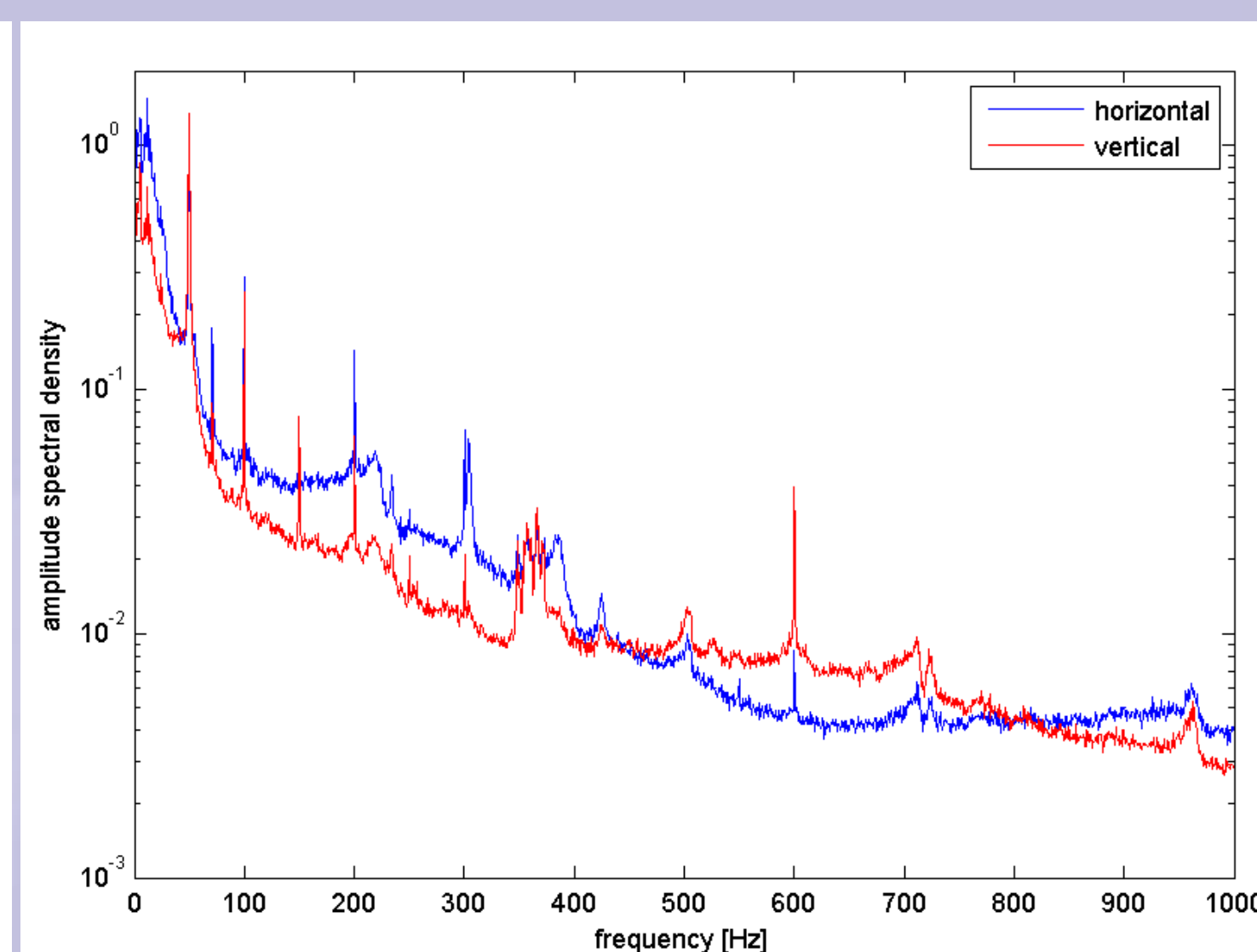
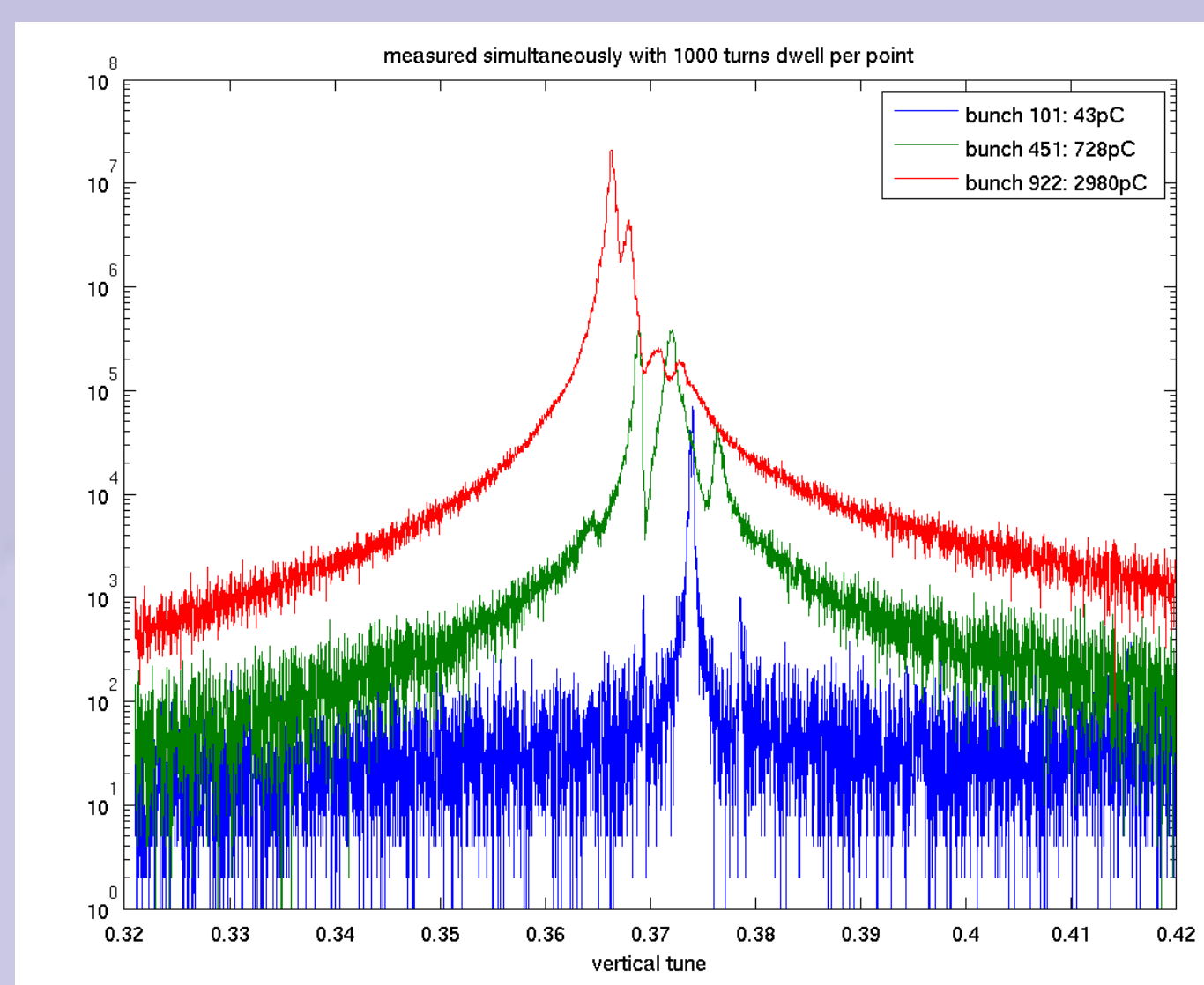
Set ADC Offsets EXIT



Phase Locked Loop Tune Tracking



One tune reading every
100 turns or 187us



Trigger Configuration (on CSR32C5-5EM-02 pin diamond.ac.uk)

SR32C5-TMBF-01 Triggers

DOR: ☐ CPU ☐ One shot ☐ Ready ☐ Arm ☐ Stop ☐ 0 ☐ turn

Buf: ☐ Hardware ☐ Register ☐ Busy ☐ Arm/Fire ☐ Stop ☐ turn

Set: ☐ SHF trigger ☐ Busy ☐ Separate ☐ Stop ☐ turn

Advanced Triggers

Trg	Enable	All	No
T0	<input type="checkbox"/> Ignore	<input type="checkbox"/> All	<input type="checkbox"/> No
T1	<input type="checkbox"/> Ignore	<input type="checkbox"/> All	<input type="checkbox"/> No
T2	<input type="checkbox"/> Ignore	<input type="checkbox"/> All	<input type="checkbox"/> No
T3	<input type="checkbox"/> Ignore	<input type="checkbox"/> All	<input type="checkbox"/> No
T4	<input type="checkbox"/> Ignore	<input type="checkbox"/> All	<input type="checkbox"/> No
T5	<input type="checkbox"/> Ignore	<input type="checkbox"/> All	<input type="checkbox"/> No
T6	<input type="checkbox"/> Ignore	<input type="checkbox"/> All	<input type="checkbox"/> No
T7	<input type="checkbox"/> Ignore	<input type="checkbox"/> All	<input type="checkbox"/> No

CSR32C5 min/max threshold: 0.0500 **SEC Ingate state:** 0

Synchronization **Timing**

Sync Inatches: ☐ Sync ☐ Zero offset: 150 **Blanking:** 10000 turns

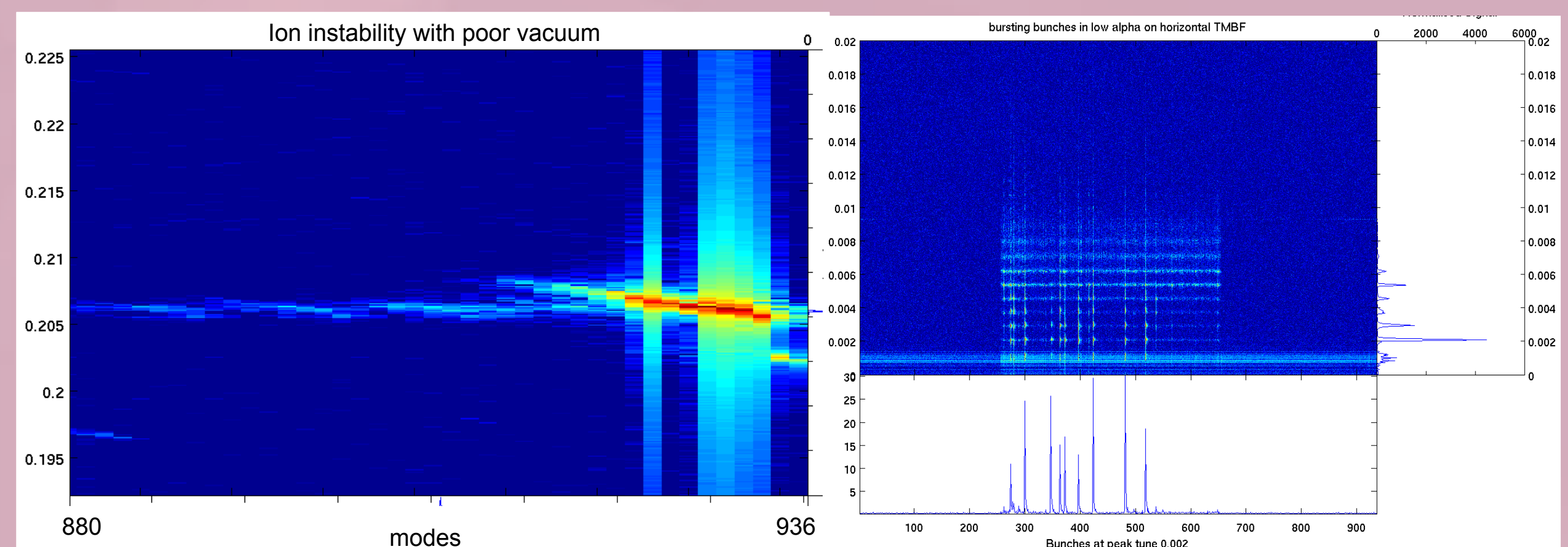
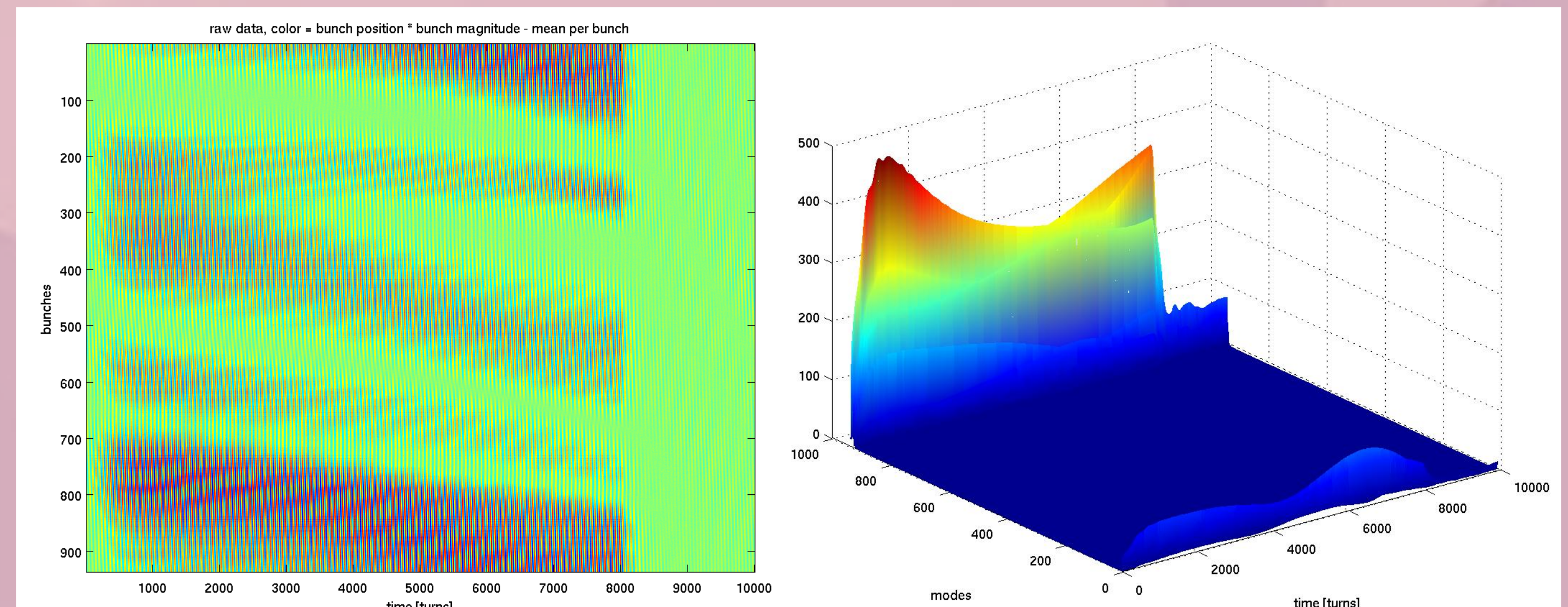
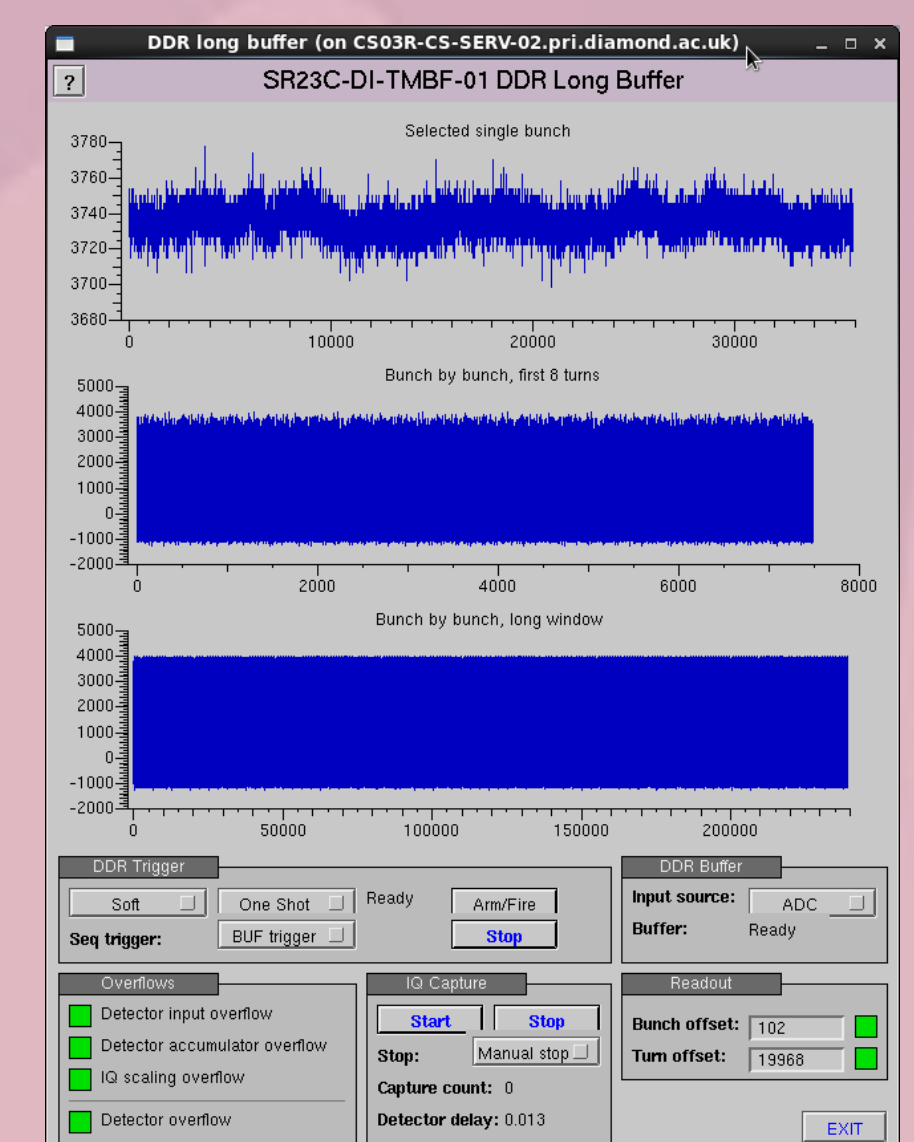
Reset sync: ☐ Reset **ARM:** 2 bits **Source:** ☐ SCUX Input ☐ turn

Sync Status: 15 Status: Synchronized

Trigger Status

Phase: 14 **Arm:** 0.0 **Count:** 19778939

after count: 6741 **0.082 %**



Control Configuration on C1030-C3-S1W422pf.dml (auto) x									
SR3C2-C1-TMSP-01 Sequencer Setup									
Input	Output	Input	Output	Input	Output	Input	Output	Input	Output
7	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1	1	1	1	CE	Disabled	Discard	Discard	Discard	Discard
6	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1	1	1	1	CE	Disabled	Discard	Discard	Discard	Discard
5	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1	1	1	1	CE	Disabled	Discard	Discard	Discard	Discard
4	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1	1	1	1	CE	Disabled	Discard	Discard	Discard	Discard
3	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1	1	1	1	CE	Disabled	Discard	Discard	Discard	Discard
2	0.00000	0.00000	0.00000	0.00000	0.00000	-15dB	Bank 1	Bank 1	Bank 1
PSD	0	1	1	CE	Disabled	Discard	Discard	Discard	Discard
1	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
PSD	0	1	1	CE	Disabled	Discard	Discard	Discard	Discard
1	0.16000	0.00000	0.26000	0.26000	0.26000	-24dB	Bank 1	Bank 1	Bank 1
ADSR	2	100	Blocking	Windowed	Windowed	Windowed	Windowed	Windowed	Windowed
Start	1	1	Stop	Copy count:	4056	Steady	Bank 0	Bank 0	Bank 0
Input	1	1	Stop	Copy count:	1761	Steady	Bank 0	Bank 0	Bank 0
Input	1	1	Stop	Copy count:	4056	Steady	Bank 0	Bank 0	Bank 0

