NSLS-II BPM & Fast Orbit Feedback



Om Singh NSLS-II Instrumentation IBIC2013, SBS, University of Oxford, UK





Outline

Overview

RF BPM

Detector/ support

- RF button optimization
- Chamber HOM coupling
- Button chamber support
- Electronics AFE, DFE, PTC
- Controls architecture
- Performance with beam
- Integrated tests



Summary





NSLS- II Key Parameters

GUN		-	
100 kV Electron Gun 40-150 bunches; 2 ns Bunching systems		Storage Ring	Nominal Value
		Energy	3.0 GeV
		Stored Beam (top up > 1 minute)	$500 \text{ mA}; \Delta I/I = 1\%$
		RF frequency	499.68 MHz
LINAC Energy Single-bunch Charge Multi-bunch Charge Emittance Energy spread	200MeV e 10 pC-0.5 nC 20 nC 55 mm-mrad 0.5% - 1.0 %	Circumference	792 m
		Revolution period, T ₀	2.642 µs
		Harmonic number	1320
		Number of bunches filled -	1056 (~80%)
		(bunch to bunch variation = 20%)	
		Tunes - Q_x , Q_y	33.36, 16.28
Типпксу		Emittance Bare Lattice ε_0 (H/V)	2.0 /0.01 nm-rad
Booster		Emittance with 8-DWs ε (H/V)	0.60/0.008 nm-rad
Circumference	158m	Bunch length – (3 rd Harmonic	15-30 ps
Harmonic Number 264 Revolution Time 0.528 µs Ramp Cycle 1 Hz		bunch length cavity)	
		Long & short straight sections –	15/15 (30 cells)
		(2 RF & 1 injection in long SS)	
Ramp Energy	200 MeV -3GeV		
Bunch Length (σ)	15ps		
Semi-turn key		9, 2013; NSLS-II BPM & Fast Orbit Feedback - Om Singh 3	BROOKHAVEN



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SR Lattice & Electron Beam sizes/divergences



NSLS-II BPM Performance Requirements

Injection System	Parameters/ Subsystems	Conditions	Vertical	Horizontal
- Rep Rate = 1Hz	Injector - single bunch	0.05 nC charge	300 µm rms	300 µm rms
Bunch Specing - 2no		0.50 nC charge	30 µm rms	30 µm rms
- Burien Spacing – Zhs	Injector - mult-bunch	15 nC charge	10 µm rms	10 µm rms
- B. Frev= 1.89MHz	(80-150 bunches) (measured)		(3 µm rms)	(4 µm rms)

Parameters/ Subsystems		Conditions	*Multipole chamber RF BPM Resolution Requirement @ 500mA stored current		* ID straight RF BPMS requires better resolution
			Vertical	Horizontal	
BPM Receiver Electronics	Turn by Turn	Data rate = 378 kHz	3 µm rms	5 µm rms	
	Assuming no contribution from bunch/ fill pattern effects	0.017 Hz to 200 Hz	0.2 µm rms	0.3 µm rms	
		200 Hz to 2000 Hz	0.4 µm rms	0.6 µm rms	
		1 min to 8 hr drift	0.2 µm peak	0.5 µm peak	
	Bunch charge/ fill pattern effects only	DC to 2000 Hz	0.2 µm rms	0.3 µm rms	Storage Ring
					- Frev = 378KHz
BPM button support assembly	Vibrations	50 Hz to 2000 Hz	10 nm rms	10 nm rms	
		4 Hz to 50 Hz	25 nm rms	25 nm rms	- Frf = 499.68MHz
	Thermal	1 min to 8 hr	0.2 µm peak	0.5 µm peak	





RF BPM Button – Geometric Optimization



BPM Heating/ Coupled bunch instability issues



Multi-pole Chamber - Resonance modes optimization(RF shield)



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RF buttons assembly support - thermal optimization



In-House Electronics

- Motivation Why design our own BPM?
 - Technology \rightarrow Use latest technology for World Class Synchrotron
 - System Architecture \rightarrow Create generic architecture
 - In-House Expertise \rightarrow Expertise resides in-house for all system aspects
- Design Decisions
 - Build two separate boards \rightarrow AFE and DFE
 - Integrated test tone Pilot tone combiner (PTC)
 - No Fan \rightarrow Leverage NSLS-II thermally stable racks, +/- 0.1°C
 - Long-Term Stability \rightarrow Combination of stable thermal rack and tunnel
 - Use Soft-Core Microprocessor \rightarrow Design Portability
 - TCP/IP Interface \rightarrow Direct EPICS and Matlab communication
- Time Line Start program in August 2009

		Injection	Storage Ring
1	Production start	August, 2011	January, 2012
2	Installation/Integration completion	April, 2013	November, 2013
3	Commissioning start	November, 2013	March, 2014





RF BPM Hardware







System Architecture - AFE



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Receiver S-Parameter Characterization



To

Digital Front End Board (DFE)

Features:

- Virtex-6 FPGA (LX240T)
- Embedded MicroBlaze soft core µP
 - Xilkernel OS and IwIP TCP/IP stack
- Gigabit Ethernet
- 2Gbyte DDR3 SO-DIMM
 - Memory throughput = 6.4 GBytes/sec
- Six 6.6Gbps SFP modules
 - Embedded Event Receiver
 - Fast Orbit Feedback
- Fixed Point DSP Engine
- 1Gbit FLASH memory
- Utilized in Cell Controller and FOF
 processor
- Currently upgrading to 7-Series Zynq part for Photon BPM
 - Hard 1GHz Dual Core ARM Cortex A9 Processor



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System Architecture – DFE FPGA

2 Gbvtes DDR3 Memory

- FPGA Implemented using a combination of VHDL, Verilog, System Generator (for DSP block) and EDK for Microblaze processor - Digital Signal Processing implementation using Matlab-Simulink Model Based design flow.
- External DDR3 Memory permits long simultaneous storage of different data streams - 32 Msamples Raw ADC, 5Msamples TbT data, 5Msamples FA data, 80 Hrs of 10Hz data



System Architecture – FPGA Signal Processing

- Under-sample 500 MHz RF signal generated by "ringing" band-pass filter.
- Coherent Signal Processing phase locked to Frev
- "Single bin" DFT position processing at TbT rate

$$X[h_{IF}] = \sum_{n=0}^{hSample-1} x[n] e^{\frac{-i \cdot 2\pi \cdot h_{IF} \cdot n}{h_{Sample}}}$$
$$n = 0..h_{Sample} - 1$$

Example numerology:

NSLS-II

Storage

Ring

499.68

MHz

1320

310

80

NSLS-II

Booster

499.68

MHz

264

62

16



System Architecture – Control System

- IOC located outside of BPM in IBM Server
- GigE communication to BPM
- Serial terminal connection to BPM via RJ45
- Embedded Event Link Receiver in FPGA
- FOFB communication using 6Gbps SFP via bidirectional "SDI" Link
- TCP/IP communication via LWIP protocol stack
- Fully developed EPICS drivers
- Simultaneous EPICS and Matlab communication



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- Performance with beam
- Integrated Tests





BPM Performance – @ ALS (single bunch); 02/2011



BPM performance - @ ALS (80% fill - 246 bunch-10/2011)

- Analysis of 1-million samples of raw ADC data
 - 1. NSLS-II RF BPM mounted in ALS rack with 10dB pad on each channel input at BPM
 - 2. Buttons combined and split in ring to remove beam motion



BPM Performance – @ NSLS-II Linac BPMs (04, 2012)

1st measured beam with RF BPM (all 5 LINAC BPMs) 120pC Single-Bunch - ~1200 Peak ADC Counts (4% FS)



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BPM Performance - @ NSLS-II Linac multi-bunch 17nC; 5/2012



RF BPM Production - Test

Phase Noise Test Port @ ADC RF BPM Burn-In: "20-units" in Thermal Test Rack RF BPM Laboratory Unit Test Setup (Bench #1) Phase Noise (Jitter) Measurement 117.34 **Gonal Cevel** -6.82 d8r 29.991 ross Corr. Mod Phase Noise [dBc RF Atten Matlab - Generate test 500MHz MO 700fs (RMS) Timing Report (15min test time) System Test Bench #2 R&S FSUP8 1 KHz Frequency Offset 35×10⁴ BPM Horizontal Stability: 8-BPMs in Thermal Test Stand over 8hrs Stability Test ADC Histogram (Coherent Sampling) BPM(1-8): 1-Million Pt. FF1 Ch A Histogram Ch B Histogram 8hr Stability (um) 2.5 150 1000 100 0.3488 0.2082 500 500 0.1435 0.1342 -0.5 0 0.5 -0.5 0 0.5 0.1248 0.1230 Frequency (MHz) CH.C Frequency (MHz) CH.D Ch D Histogram Ch C Histogram 0.1685 0.1132 100 2000 U.S. DEPARTMENT OF 500 1500 100 1000 500 20 40 Frequency (MHz) Frequency (MHz) Xpos(µm) -0.5 D.5 -1 -0.5 0 Π. 0.5

In-situ Integration Test using Pilot Tone



In-situ noise observation & mitigation



The 500 Hz spurious signals at ~100 nm level are observed in the FA data spectrum due to noise pickup in AFE from DFE via metal top cover.

The spurious signals have been eliminated after installation of a 4"x6 " micro-wave absorber onto the top cover.





Fast Orbit Feedback

Kiman Ha Li-Hua Yu Yuke Tian





External Noise Sources - Mitigations

Mitigated by improved design

& temperature regulation

- Magnet & RF system power supply noise / ripple
- Thermal effects (Tunnel air / water temperature)
- Earth tides changes circumferences RF frequency feedback
- Insertion device gap change effects due to magnetic field errors
- NSLS-2 site floor vibration –



FOF AC Functional Requirements

- Noise reduction @ low freq = 100 (DC gain ~= 100)
- Noise reduction @ 100 Hz > 2.5
- FOF gain cross over Frequency = 300 Hz







Fast Corrector Requirement vs Noise Sources







Orbit Correction Magnets



Slow corrector magnets (Qty=6)

Slow response – 2 Hz
Strong strength – 800 µrad
Utilized for slow orbit fdbk

Fast corrector magnets (Qty=3)
Fast response – 2 kHz
Weak strength – 15 µrad
Utilized for fast orbit feedback







NSLS-II FOFB algorithm – Compensation for each eigenmode

- Fast orbit feedback system is a typical multiple-input and multiple-output (MIMO) system. For NSLS-II, there are 180 BPM readings and 90 fast corrector set points in each plane. The BPMs and correctors are coupled together. One BPM reading is the results of many correctors. One corrector kick can also affect many BPM readings. It is difficult to design a compensator for all noises with different frequencies.
- It is desirable if we can decouple the BPM and corrector relationship so that the MIMO problem can be converted into many single input single output (SISO) problems, for which control theory has many standard treatments.
- Fortunately, SVD already provides a solution: it projects the BPMs input into the eigenspace, where each component is independent. We can design many SISO type compensators (one for each eigenmode) and apply the standard SISO control theory to treat each eigenmode problem in frequency domain without affecting other eigenmodes.





Model and solving the calculation problem



 $c_1, c_2, ..., c_N$ is the input projections in the eigenspace. $Q_1(z), Q_2(z), ..., Q_N(z)$ is the compensator for each eigenmode.





Simulation of Orbit Feedback results vs # of Eigen Modes



FOFB Key Requirements

- **1.** Goal is to deliver BPM data to a *place* that orbit calculation module have directly access.
- 2.Similarly, goal is to deliver corrector setpoint from a *place* that orbit calculation module have directly access.
- **3.** It seems we need a *place* that can:
 - → Receive local BPM data;
 - \rightarrow Tx/Rx BPM data to/for other cell;
 - \rightarrow Carry out FOFB calculation;
 - \rightarrow Tx corrector setpoints to PS control system.

A Cell Controller is designed for this purpose





Cell Controller Architecture



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Topology of a Cell



EVG

Topology of the FOFB network



Power Supply Controller & Interface Hardware

PSC – power supply controller







PSI – power supply interface





Cell Controller Hardware



NSLS-II Fast Orbit Feedback Status

- The hardware design (PCB, chassis) for cell controller and PSC are all done. The production units are being installed in the storage ring.
- PSC, FPGA firmware, EPICS drivers and database development are all done.
- All cell controller blocks (SDI, FOFB etc) are all done. The cell controller integration is in progress.
- Since we have the fast fiber SDI to deliver data around the ring, cell controller's SDI link will also be used as fast machine protection system that deliver critical system (such as the vast valve signal from vacuum system) around the ring within much less than 1ms. This latency is impossible for PLC to achieve.





Summary – RF BPM

- RF BPM detector and support optimization carried out successfully
- The Multipole vacuum chamber RF buttons (LA) installed
- Insertion device RF buttons (SA) production unit delivery this month
- The RF BPM electronics
 - Injector installation/ integration completed
 - SR installation completed; integration to complete by 11/2013
- Performance results with beam at ALS & NSLS-II Linac/ Ltb are encouraging
- Commissioning/ plan
 - Linac/ Ltb transport line commissioning completed successfully on 5/2012
 - Remaining injector commissioning to start on 11/2013
 - SR commissioning to start on 3/2014





Summary - FOFB

- NSLS-II's stringent emittance requirements need a efficient fast orbit feedback system. The two tier communication structure and the FPGAbased fast orbit feedback calculation architecture is designed for achieve the requirements.
- Algorithm with individual eigenmode compensation is proposed. The typical MIMO feedback problem is converted into many SISO problems. This algorithm enables accelerator physicists to correct the beam orbit in eigenspace.
- We compared the calculations for FOFB with and without individual eigenmode compensation. We found that the proposed NSLS-II FOFB algorithm needs a large amount of calculations. However, benefited from NSLS-II FOFB architecture, the challenge can be conquered.
- We expect a successful application of the NSLS-II FOFB algorithm during the NSLS-II commissioning and daily operation.





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Collaborators – Mike Chin (LBNL), Greg Portman (LBNL), J. Sebek (SLAC), Jonah Webber (LBNL)





Thank you for your kind attention.





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One Cell BPM/ Controller Rack



Vibration Test Results



Resolution vs Bandwidth @ ALS SR



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Timing Synchronizations



Fast Orbit Feedback Algorithm – Implementation in FPGA



Use FPGA parallel computation features to implement the algorithm (assume 240 BPMs, 90 correctors) U_{1}^{T} , U_{2}^{T} ... U_{90}^{T} : input matrix vector -- download from control system as waveform PV $V_{1}, V_{2}, ... V_{90}$: output matrix vector -- download from control system as waveform PV $Q_{1}(z), Q_{2}(z), ..., Q_{90}(z)$: compensator for each eigenmode -- parameters download from control system



