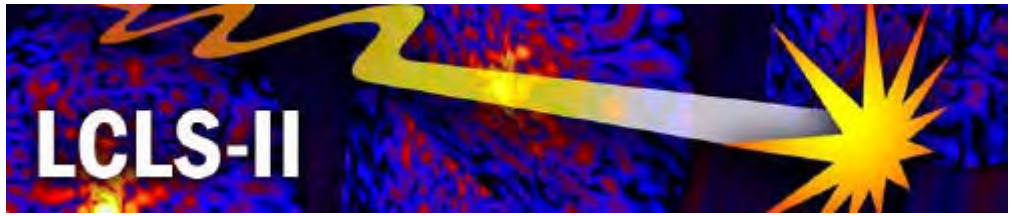

SLAC NATIONAL ACCELERATOR LABORATORY

BERKELEY LAB
Lawrence Berkeley National Laboratory

LCLS-II Cavity BPMs Electronics

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U.S. DEPARTMENT OF ENERGY | Office of Science

LELAND STANFORD JUNIOR UNIVERSITY
DIE LUFT DER FREIHEIT WEHT
1891

Outline

- New Requirements
- New Designs
- MicroTCA
- Discussion points

Specifications

Cavity SPECS

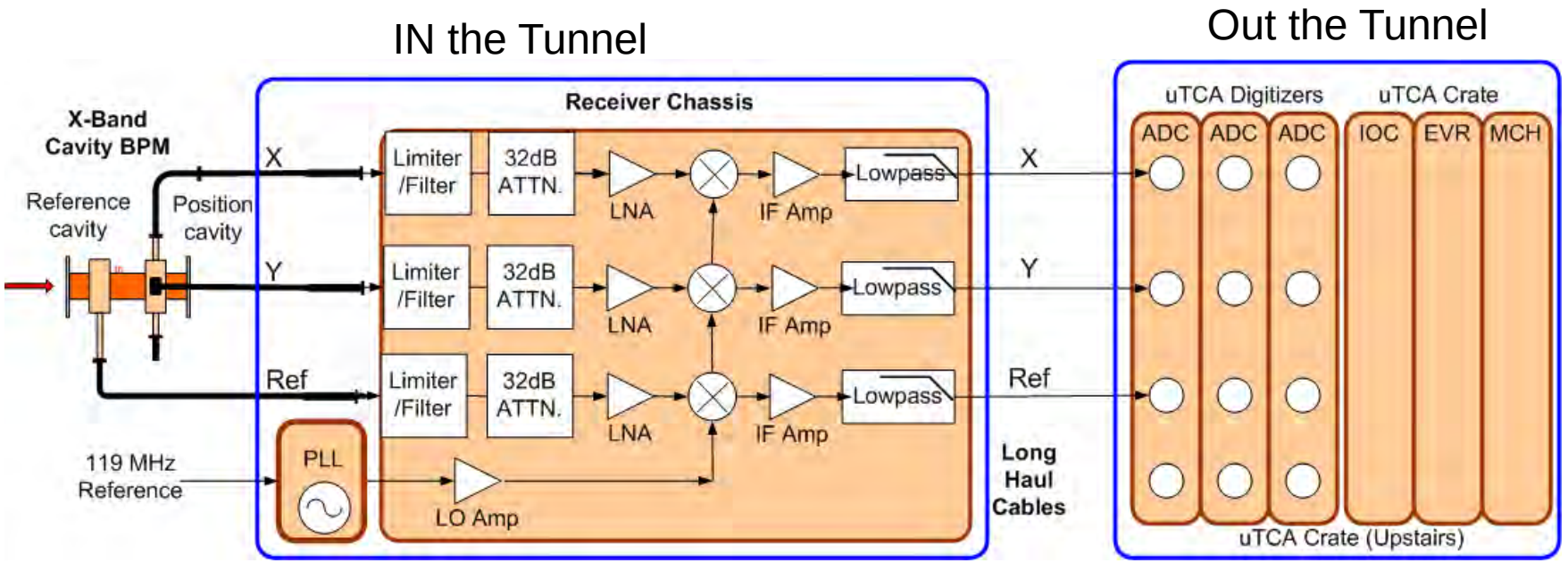
Parameter	Specification Limit
TM110 Frequency Dipole Frequency	11.424 GHz
Loaded Q Factor Dipole Cavity	2000-3000
Q_{ext} (Dipole Cavity)	4131???
R/Q for Dipole Cavity	>2 Ohms/mm^2
Voltage induced in Dipole cavity	5mV/pC/mm
X/Y Cross Talk Dipole Cavity	<-20dB (check)
TM010 Frequency Monopole Cavity	11.424
Loaded Q factor Monopole Cavity	1150???
Q_{ext} (Monopole Cavity)	2000-3000
R/Q for Monopole Cavity	≥ 12 Ω
Voltage induced in Monopole cavity	20mV/pC

BPM Receiver SPECS

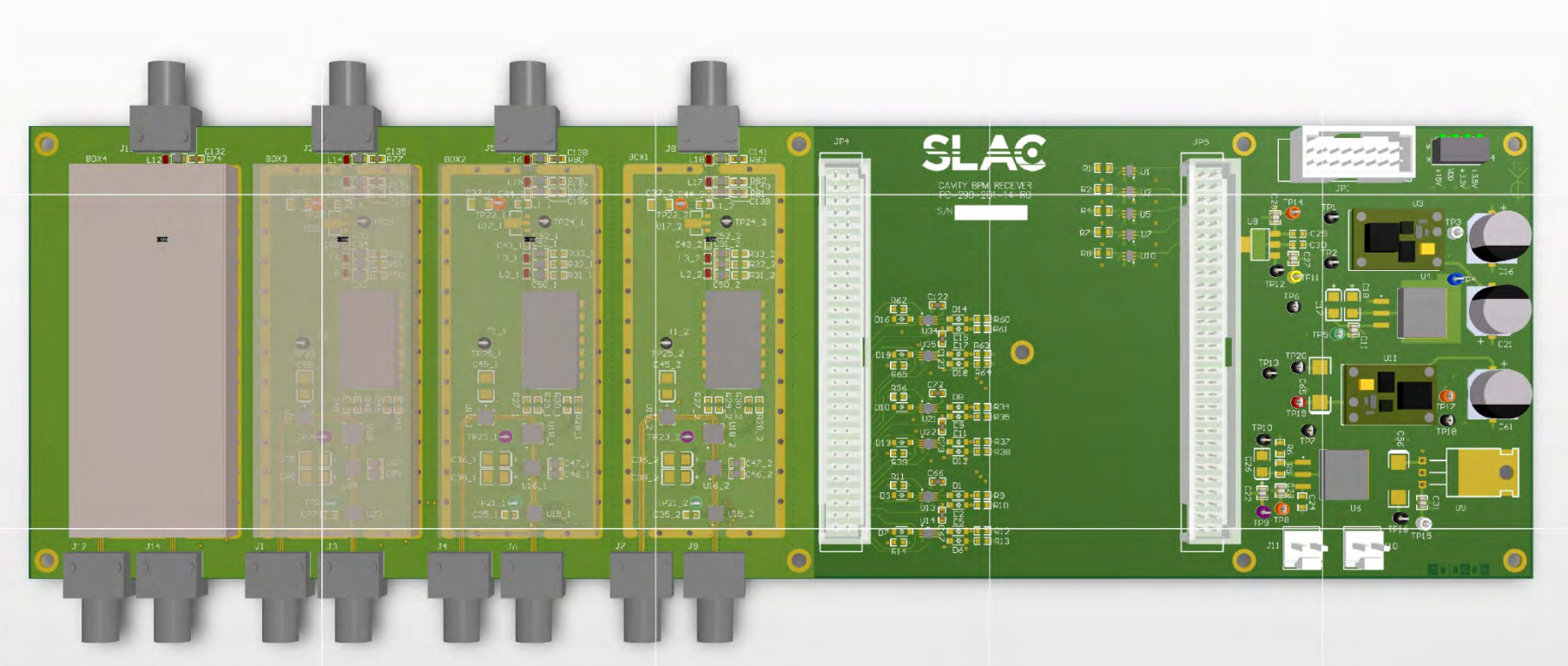
Parameter	Specification Limit
Charge	10pC – 1nC (200pC typ)
Resolution @1pC	100µm
Resolution @250pC	250nm
Offset	+/-5mm
Linear Dynamic	~80dB
Lo Freq	11.384GHz
Operational Frequency Band (RF in)	X-Ku
Typical RF input Frequency	11.424GHz**
Bandwidth at F(RF)	200MHz
IF Bandwidth (119MS/a or 238(Msa/s)	30-60MHz
Max input power	14dBm
P1dB Output power	18dBm
Max LO to RF rejection	45dB
Max LO to IF rejection	20dB

$$V_{peak} = q\omega\sqrt{\frac{Z}{8}\left(\frac{R}{Q}\right)_{\perp}\frac{1}{Q_{ext}}} \qquad P_{out} = \frac{\omega^2}{4Q_{ext}}\frac{R}{Q}q^2$$

New Block Diagram

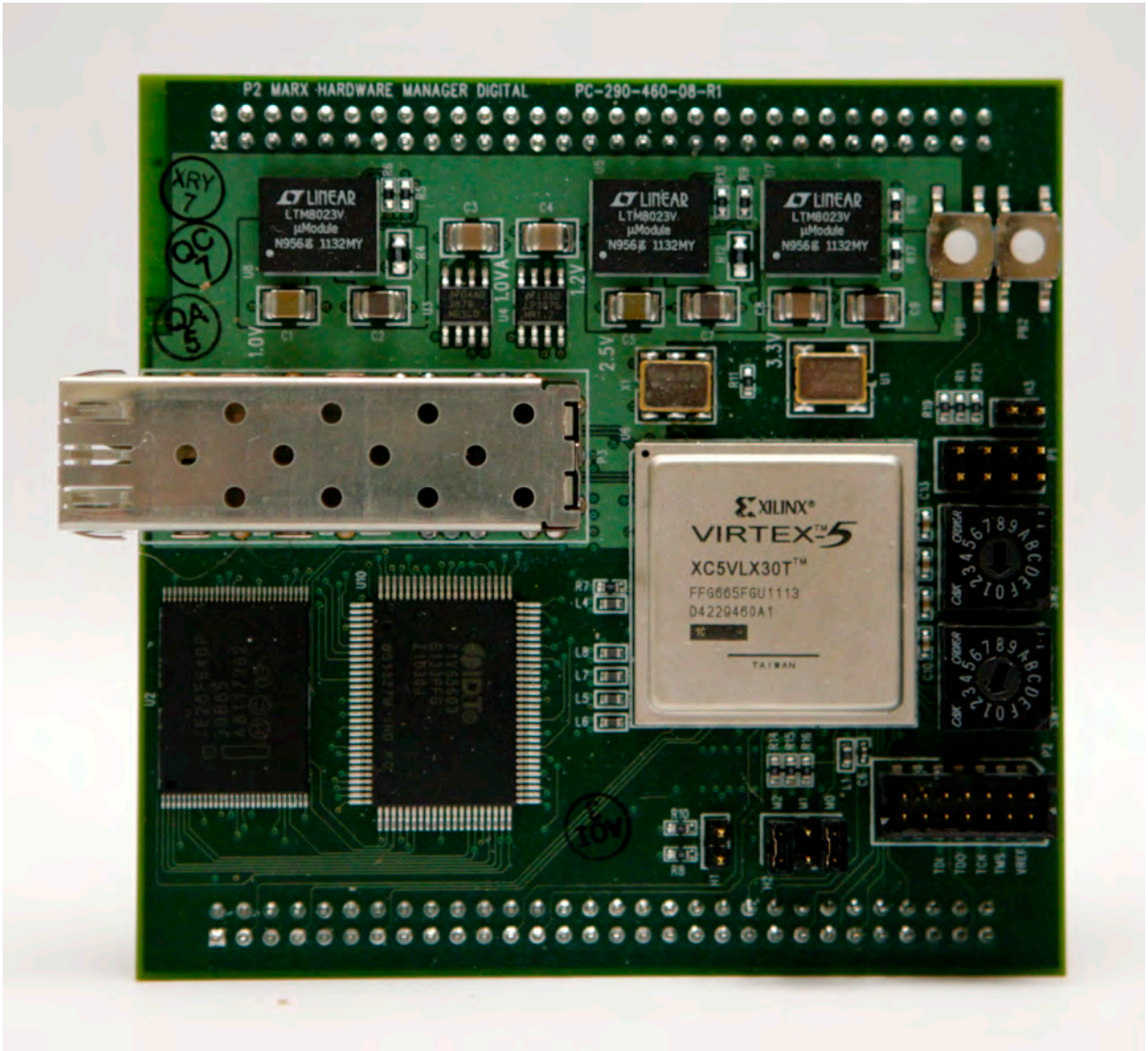


Board Layout



PLL Interface

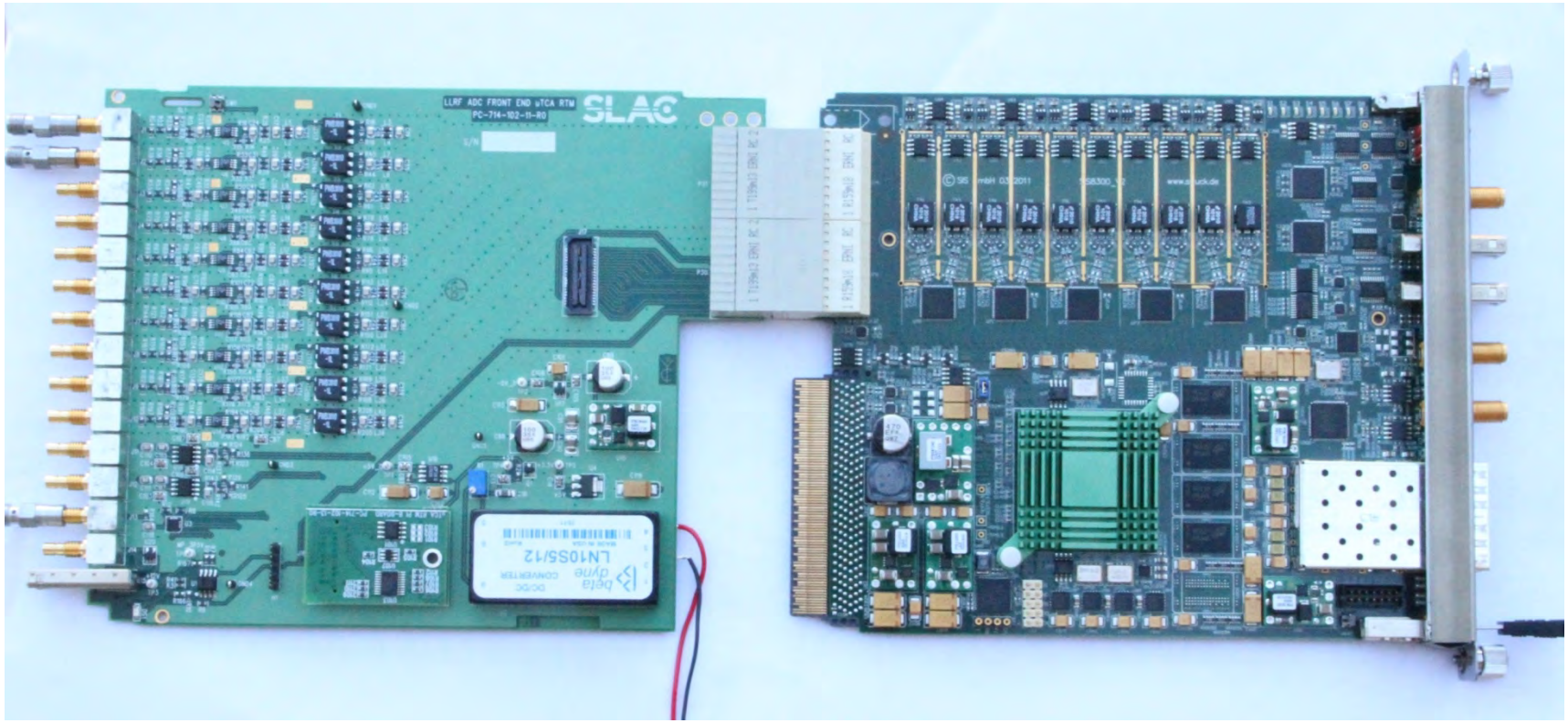
Communication Hardware



Chassis


Cavity BPM Receiver Chassis
RF CH 4 OUT
RF CH REF OUT
RF CH X OUT
RF CH Y OUT
LAN
+24V
RF LO REF IN
290-201-15

µTCA ADC Interface



Using the LLRF RTM board with a modification for MPS interface we can interface with the Struck 119MSa/s ADC. Using the general DIO bit on Zone 3 connector we can design an MPS TTL logic interface.

It is possible to have 2 BPMs interface to the ADC.

Discussion Points

- Downmixing vs Diodes
- PLL vs Oscillators
- VME ADC vs µTCA