



Andrew Young, John Dusatko, Sonya Hoobler, Jeff Olsen, Till Straumann SLAC, Menlo Park, California, Changbum Kim PAL, Pohang, Kyungbuk

## avoung@slac.stanford.edu

SLAC is developing a new X-band Cavity BPM receiver for use in the LCLS-II. The Linac Coherent Light Source II (LCLS-II) will be a free electron laser (FEL) at SLAC producing coherent 0.5-77 Angstroms hard and soft x-rays. To achieve this level of performance precise, stable alignment of the electron beam in the undulator is required. The LCLS-II cavity BPM system will provide single shot resolution better than 50 nm resolution at 200 pC [1]. The Cavity BPM heterodyne receiver is located in the tunnel close to the cavity BPM. The receiver will processes the TM010 monopole reference cavity signal and a TM110 dipole cavity signal at approximately 11 GHz using a heterodyne technique. The heterodyne receiver will be capable of detecting a multibunch beam with a 50ms fill pattern. A new LAN communication daughter board will allow the receiver to talk to an input-output-controller (IOC) over 100 meters to set gains, control the phase locked local oscillator, and monitor the status of the receiver. We will describe the design methodology including noise analysis, Intermodulation Products analysis.

## ndulator BPM Spe

- Undulator orbit critical
- Must keep electrons and photons coincident
- to fraction of beam size

 over	uistan	ice >	gain	lengt	11

	LCLS-I	LCLS-II	Comments
Frequency	11.384 GHz	11.424 GHz	multibunch
Output	Waveguide	coax	More flexible
Tuning	12 tuning stubs	<= 4 tuners	Lower cost
Receiver	14dB I.L. with 28 dB Gain step	<= 3dB I.L. 1 dB step	Improved noise figure and dynamic range
Digitizer	SLAC/VME	uTCA	Lower cost
Ref. cavity	Single output	2 couplers	Improved mode centering



This is a picture of the Cavity Designed by Pohang under a cooperative research and agreement 13-230C with development (CRADA) SLAC. Beam passes through the monopole reference cavity on the right, exciting the  $TM_{010}$ monopole mode signal resonant at 11.424 GHz.





The TM<sub>110</sub> dipole cavity is located 36 mm downstream through the 9diameter beam pipe. The position cavity dipole mode is resonant at 11.424 GHz, its output proportional to the product of beam position and bunch charge. The X and Y position modes are nominally degenerate in frequency, with the appropriate component chosen by the geometry of the couplers. The dipole coupler geometry is chosen to reject (the generally larger) monopole modes [2-6]. The dipole cavity was designed as a 4-port device with two opposing X couplers orthogonal to two opposing Y couplers. This is useful for cold and preserves symmetry. esting Unused ports are terminated with the potential for using them for future diagnostics.

Parameter	Requirement	Conditions
Resolution	< 250 nm	200 pC < Q < 1 nC
		Over ± 1 mm range
	< ±1 micron	1 hour
Offset Stability		$\pm$ 1 mm range, 20 C $\pm$ 0.56 C
	< ±3 microns	24 hour
		$\pm$ 1 mm range, 20 C $\pm$ 0.56 C
Gain Stability	± 10 %	± 1 mm range
		$20 \text{ C} \pm 0.56 \text{ C}$
Aperture	9 mm	



BPMs were designed to a bandwidth of  $\pm 5$  MHz . The performance of the Cavity is illustrated in Figure 2 and Figure 3. The bandwidth of the cavity was measured to be 7 MHz. The Beta of the cavities was measured using a VSWR approach, Measuring the loaded Q each cavity was done using a  $S_{21}$  3dB bandwidth as illustrated in the figures. Another measurement of loaded Q was performed using a full-width-half-maximum and obtained similar results. From these measurements one can calculate the Q external and Q<sub>0</sub> using equation 1.  $Q_{ext} = \frac{1+\beta}{\beta} * Q_L and Q_0 = (1+\beta)Q_L$ (1)

The peak output voltage from the cavity can derived from equation 2. The R/Q was measured using a metal and ceramic bead.  $V_{peak} = q\omega \sqrt{\frac{Z}{8} \left(\frac{R}{Q}\right) \frac{1}{Q_{ext}}}$ 

(2)





- High density plug connectors up to 5 GHz available (mTCA) interface on rear adapters
- High Availability standard architectures (mTCA)
- Hot swap modules demonstrated (mTCA)
- Gigabit communications w/ embedded processor chips, high speed 12-16 bit sampler ADC-DAC commodity products, more to come.....
- IPMI interfaces let you know status of temperatures, power, cooling, module present





An EPICS IOC communicates with the receiver via UDP messages. The receiver acts as a server, responding to commands and requests from the IOC. The IOC polls the receiver periodically for current register values and monitoring signals and provides this data via EPICS PVs. The IOC will control the SPI interface to the PLL, Attenuator control on the receiver board, and I2C interface that monitors temperatures, and power supply voltages.

The two PCB boards (PLL and the Receiver) with other supporting components are integrated into a 19in chassis and installed on a shelf under the cavity BPM and Undulator. The Pohang Cavity was installed at the end of LCLS-I undulator and beam testing will begin later this year when LCLS-I turns back on.



