1. CSNS RCS BPM PICK-UP SIGNAL

- CSNS RCS BPM system adopt the linear-cut pick-up electrode.
- The capacitor C is 366pF, and the load is 50Ω. The equivalent circuit is show in figure 1.
- The pick-up signal in injection and in extraction stage is showed in figure 2.

**Features of pick-up signal:**
- Dynamic range: 5.8mV~32V(75dB)
- Length of signal: 80ns~500ns
- Analog bandwidth: 30MHz
- Revolution frequency: 1MHz~2.4MHz

2. DESIGN OF ELECTRONICS

2.1 Architecture of electronics

- Using digital $\Delta/\Sigma$ method to process the pick-up signal. The four pick-up signal is processed and digitalized individually.
- Bunch-by-bunch position and Closed Orbit position is calculated in FPGA.
- DDR2 for storage.
- CPLD and Flash to implement online configuration.
- VME bus for transportation and configuration.

2.2 the design of analog circuit

- The circuit consists of three stage amplifier.
- The first stage amp. has a gain of 0.5 to receive all pick-up signal.
- The second stage amp. is variable gain amplifier(VGA), with gain varying from *16 to 1/16.
- The third stage amp. convert the signal to differential signal to provide to ADC.
- LPF is placed between the second and the third stage, with bandwidth 30MHz.

3. SIGNAL PROCESSING

- Digital signal is aligned to each other.
- Bunch-by-bunch and COD position is calculated in real time.
- The bunch-by-bunch position is sent to DDR2 for storage, and the COD position is sent our through VME bus.
- Waveform recording & Auto Gain Control.

4. TEST

- Bunch-by-bunch position resolution: 0.9mm@10mV
- Closed Orbit position resolution: 50um@10mV
- Primary test @ laboratory

CONCLUSION

- CSNS RCS BPM electronics implemented by $\Delta/\Sigma$ method;
- Propose a VGA circuit that can process the pick-up signal with dynamic range of 75dB;
- Bunch-by-bunch resolution: 0.9mm@10mV
- COD resolution: 50um@10mV