The Design of BPM Electronics for CSNS RCS

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ABSTRACT

The challenge of designing the CSNS RCS BPM electronics is to acquire and process the signal with large dynamic range (5.8mv~32V) and changing width (80ns to 500ns). The analog circuit described in this paper, which is constructed of single-stage amplifier and analog switch, can cover the pick-up signal with large dynamic range. Because of the minimum bunch length (80ns) and the requirement of position resolution, a 14 bit 250MHz ADC is adopted to digitalize the signal. Besides, the algorithm developed in FPGA is able to make Bunch-by-Bunch position calculation and Closed Orbit position calculation in real time. In addition, some preliminary test results will be presented and discussed, which show that the resolution of Bunch-by-Bunch position is 0.8mm when the input signal is 10mV and the resolution of Closed Orbit position is 50μm.

1, CSNS RCS BPM PICK-UP SIGNAL

- CSNS RCS BPM system adopt the linear-cut pick-up electrode.
- The capacitor C is 366pF, and the load is 50Ω. The equivalent circuit is show in figure 1.
- The pick-up signal in injection and in extraction stage is showed in figure 2.

Features of pick-up signal:

Dynamic range: 5.8mV~32V(75dB)

Length of signal: 80ns~500ns

Analog bandwidth: 30MHz

Revolution frequency: 1MHz~2.4MHz

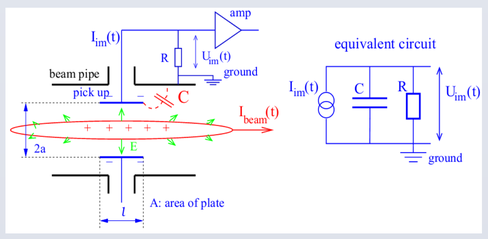

Fig.1: scheme of pick-up electrode and its equivalent circuit

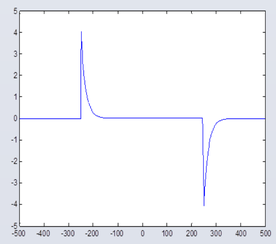

Fig.2-1: Pick-up signal in injection stage

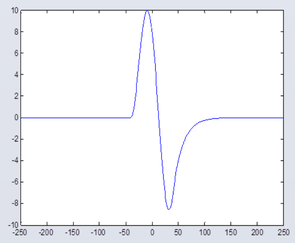

Fig.2-2: Pick-up signal in extraction stage

2, DESIGN OF ELECTRONICS

2.1 Architecture of electronics

- Using digital Δ/Σ method to process the pick-up signal. The four pick-up signal is processed and digitalized individually.
- Bunch-by-bunch position and Closed Orbit position is calculated in FPGA.
- DDR2 for storage.
- CPLD and Flash to implement online configuration.
- VME bus for transportation and configuration.
- External trigger, external clock. Can output beam bunch information.

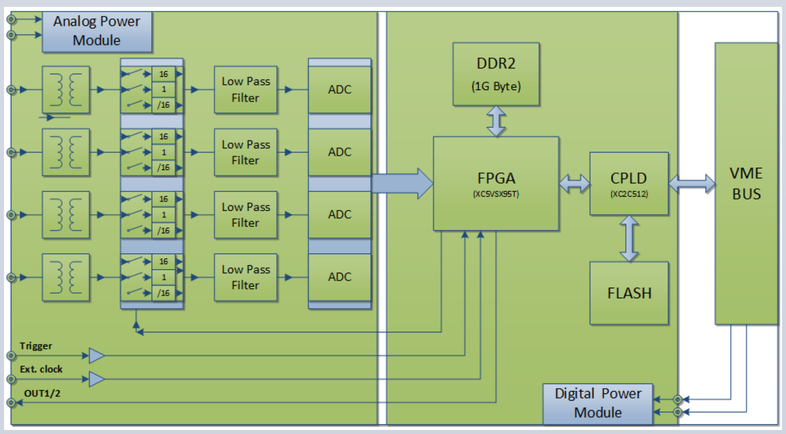

Fig.3: Architecture of CSNS RCS BPM electronics

Fig.4: The PCB board

2.2 the design of analog circuit

- The circuit consists of three stage amplifier.
- The first stage amp. has a gain of 0.5 to receive all pick-up signal.
- The second stage amp. is variable gain amplifier(VGA), with gain varying from *16 to 1/16.
- The third stage amp. convert the signal to differential signal to provide to ADC.
- LPF is placed between the second and the third stage, with bandwidth 30MHz.

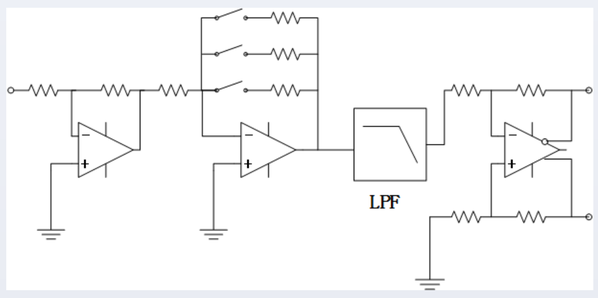

Fig.5: Structure of analog circuit

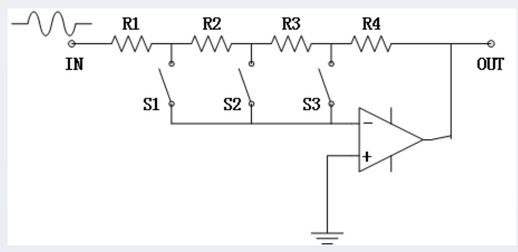

Fig.6: Structure of the second stage amplifier

- For the second stage, it is challengeable to implement gain changing from 16 to 1/16.
- We propose a structure showed in Fig. 6. The resistors has a relationship: R1=R4， R2=R3， R2=7.5*R1. Gain can change from 16 to 1/16.
- Switches are connected to inverting input of the amp. , so the “Off Isolation” performance is not crucial. 30MHz is OK!

3, SIGNAL PROCESSING

- Digital signal is aligned to each other.
- Bunch-by-bunch and COD position is calculated in real time.
- The bunch-by-bunch position is sent to DDR2 for storage, and the COD position is sent out through VME bus.
- Waveform recording & Auto Gain Control.

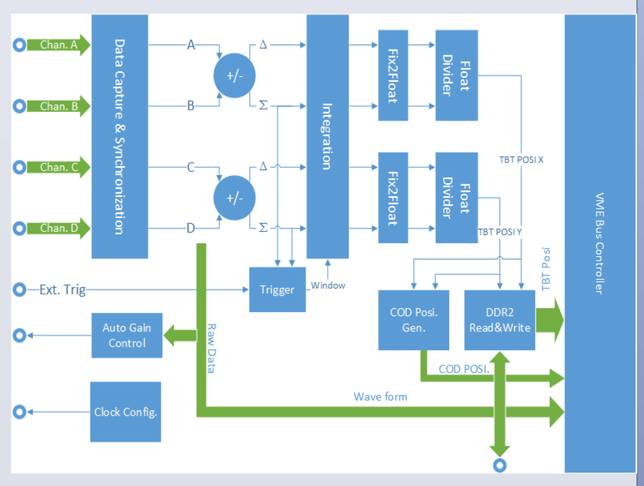

Fig.7: The architecture of the firmware in FPGA

4, TEST

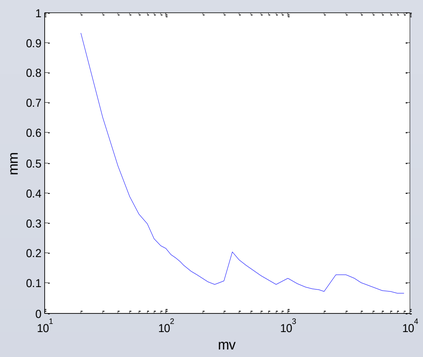

Fig.8: Bunch-by-bunch position resolution

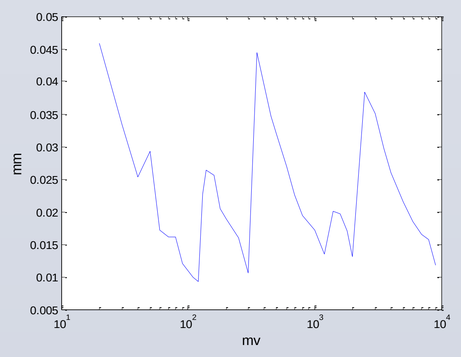

Fig.9: Closed Orbit position resolution

- Bunch-by-bunch position resolution: 0.9mm@10mV
- Closed Orbit position resolution: 50um@10mV
- Primary test @ laboratory

CONCLUSION

- CSNS RCS BPM electronics implemented by Δ/Σ method;
- Propose a VGA circuit that can process the pick-up signal with dynamic range of 75dB;
- Bunch-by-bunch resolution: 0.9mm@10mV
- COD resolution: 50um@10mV