A Gigabit Ethernet Link for an FPGA Based Beam Loss Measurement System.

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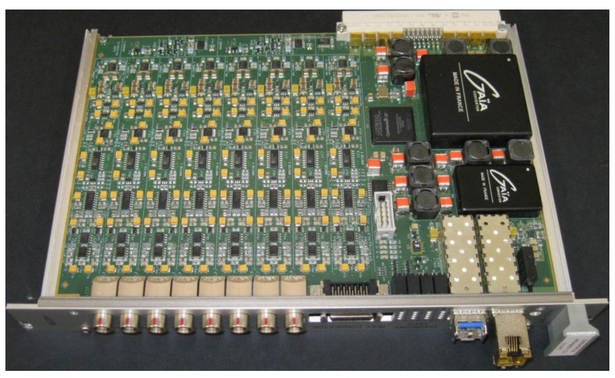
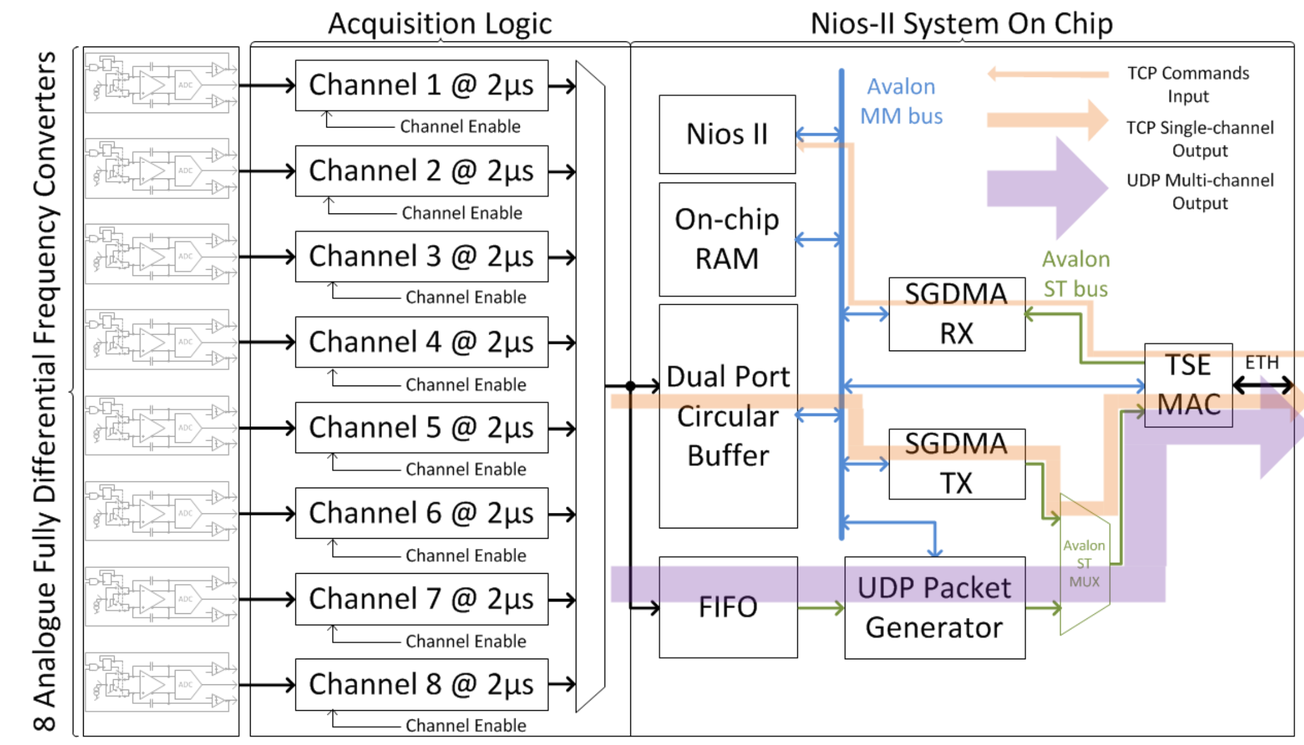
Abstract: A new Beam Loss Measurement (BLM) system is under development at the European Organisation for Nuclear Research (CERN) within the LHC Injector Upgrade (LIU) project. The multi-channel system will measure the beam losses from various types of detectors with a high precision and wide dynamic range. Several modes of data acquisition are supported. The data rate in the single-channel mode is 16 Mbps and in the multi-channel mode 128 Mbps. The Gigabit Ethernet link is implemented in an FPGA, which allows both a high throughput and a quick validation of the digital data processing algorithms using standard PCs in the initial stages of the development. Both TCP and UDP protocols were explored. The implementation of the Ethernet link is flexible and proved to be highly reliable, leading to its planned use in other measurement systems developed at CERN.

Acquisition Card



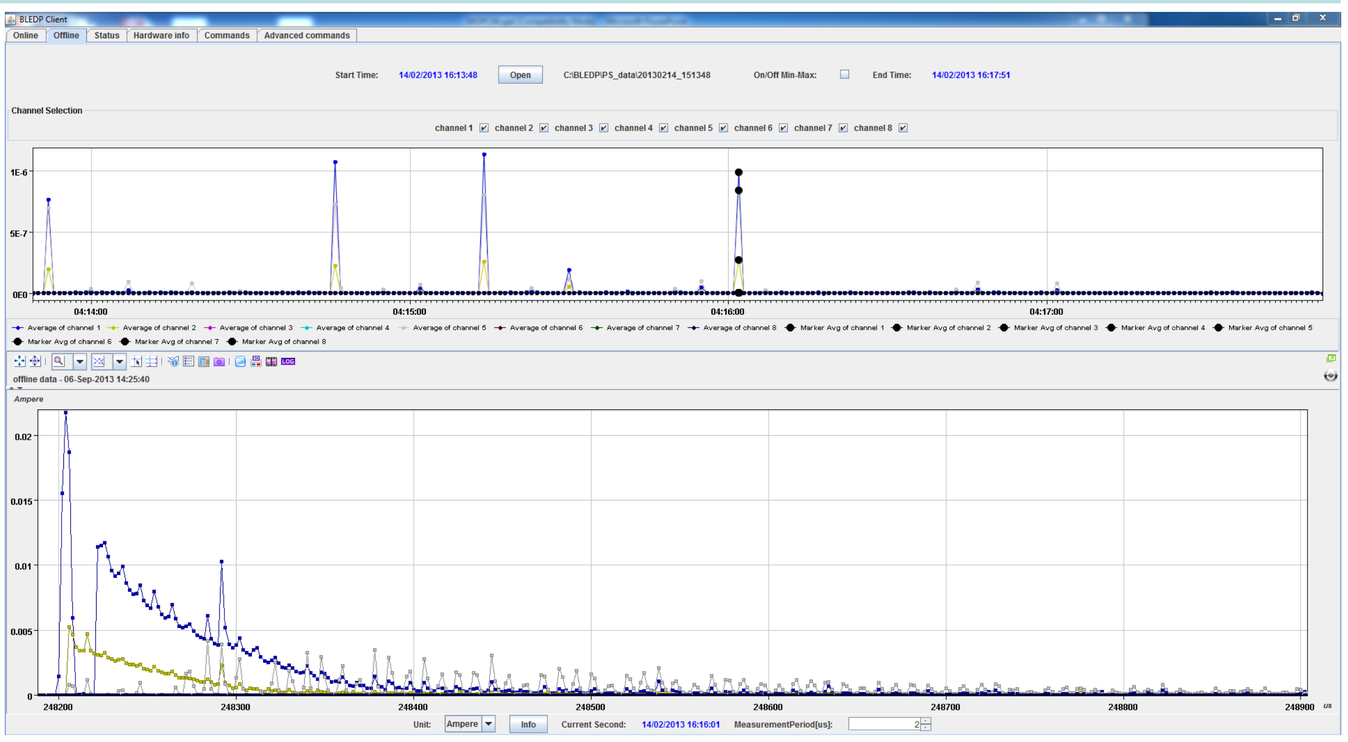
- 8 analogue inputs with wide dynamic range
- Two measurement modes:
  - Direct ADC (DADC) conversion for input current in 100µA - 200mA range
  - Fully Differential Frequency Converter (FDFC) for input current in 10pA - 10mA range
- Measurement every 2µs
- Altera Cyclone 4GX150 FPGA with two 3.125 GBPS transceivers
- Two SFP slots for communication (copper or optical medium, Ethernet or custom protocols)

FPGA Firmware with the Gigabit Ethernet



The FPGA firmware consists of a custom logic and a Nios-II **System-On-Chip** (**SOC**). The custom logic is responsible for data processing from 8 fully differential analogue integrators and ADC converters. The SOC implements communication protocols with the card. The TCP protocol is based on hardware and software **Components Of The Shelf** (**COTS**) provided by Altera and it is used to send commands to the card and acquire data from one channel with the speed of 16Mbit/s. For the multi-channel data acquisition (128Mbit/s) the UDP protocol is used which is implemented fully in the hardware and it does not depend on the software running on the Nios-II processor. The UDP implementation is fast but it requires custom components in the SOC.

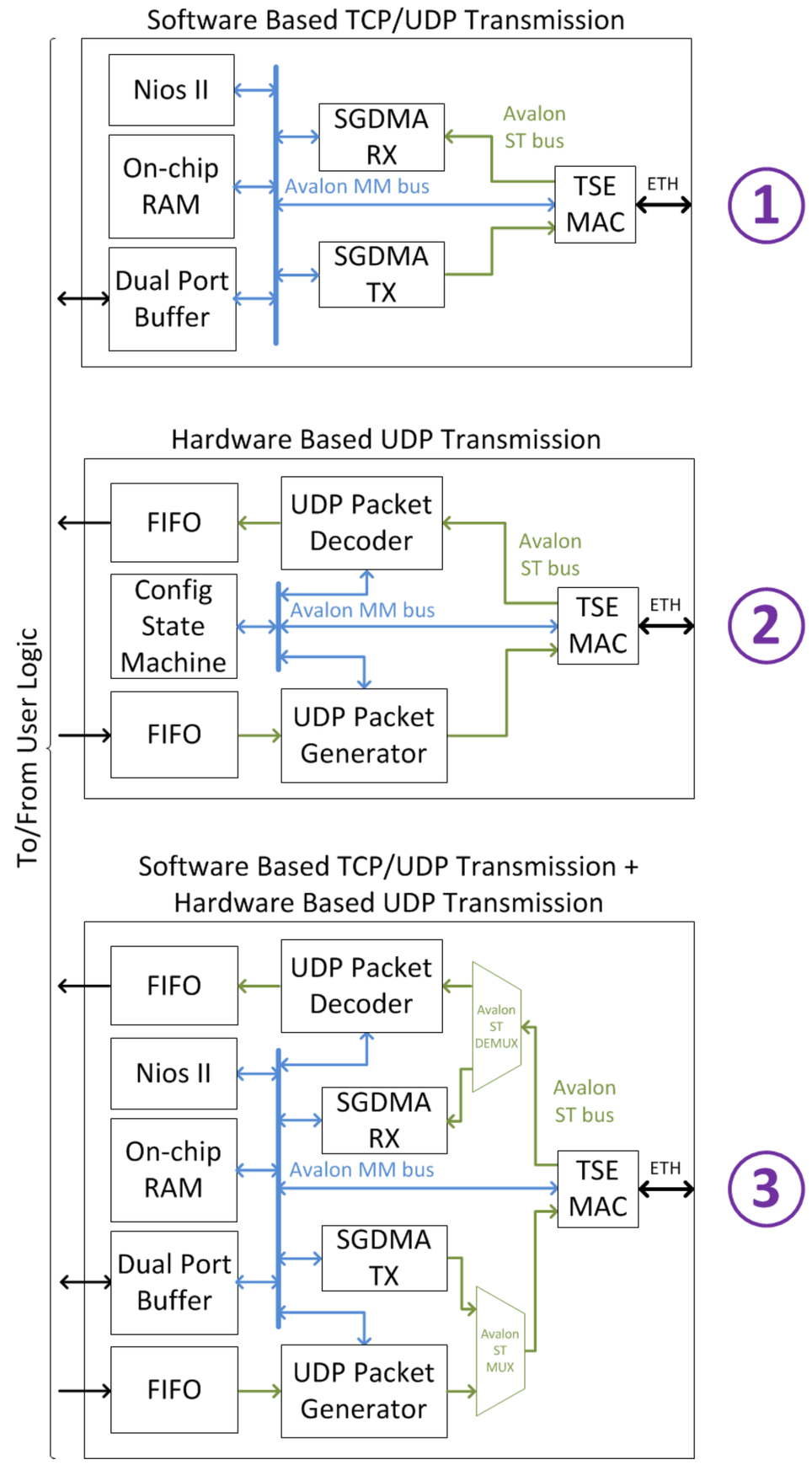
Multichannel Acquisition from a Test Installation in the Proton Synchrotron Accelerator



The multi-mode acquisition capability of the newly developed card allowed analysis of a real data acquired in the Proton Synchrotron (PS) accelerator at CERN (see figure above). The hardware was also verified in the laboratory where cross-talk tests were performed by the analysis of acquired data in the Matlab software. The Ethernet firmware was proven to be reliable and therefore it will be also used in the standalone version of the acquisition crate.

Other Variants of the Ethernet Firmware

A generic board with an Altera FPGA is currently under development in the Beam Instrumentation (BI) group at CERN. The Ethernet firmware can be reused in the other projects realised by the BI. For this reason other variants of the Ethernet implementation were proposed:



1. Standard configuration using only Altera COTS (Nios-II, **Triple Speed Ethernet (TSE) MAC**, **Scatter-Gather DMA (SGDMA)**, Niche TCP/IP Software Stack). It allows implementing TCP and UDP based communication but its speed is limited to around 20-30 Mbit/s by the software running on the Nios-II processor. Owing to ready COTS it can be implemented fast.
2. Fully Hardware UDP communication. It does not require use of the Nios-II or any software. It requires additional custom components:
   - UDP packet generator/decoder and multiplexer/de-multiplexer with the **Avalon Streaming (ST) Bus**
   - Configurator state machine with the **Avalon Memory-Mapped (MM) Bus** to configure the MAC and UDP network parameters.

   Its advantage is the speed which can reach real 1Gbit/s but only with the UDP protocol. The implementation time is longer due to the custom components.
3. The hybrid containing both the software based TCP/UDP and the hardware based UDP data path.

In all 3 cases the data paths can be trimmed to one direction depending on the needs of a given design e.g. only output UDP data stream.

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