The Hardware Implementation of the CERN SPS Ultrafast Feedback Processor Demonstrator

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Abstract

An ultrafast 4GSa/s transverse feedback processor has been developed for proof-of-concept studies of feedback control of e-cloud driven and transverse mode coupled intra-bunch instabilities in the CERN SPS. This system consists of a high-speed ADC on the front end and equally fast DAC on the back end. All control and signal processing is implemented in FPGA logic. This system is capable of taking up to 16 sample slices across a single SPS bunch and processing each slice individually within a reconfigurable signal processor. This demonstrator system is a rapidly developed prototype, consisting of both commercial and custom-design components. It can stabilize the motion of a single particle bunch using closed loop feedback. The system can also run open loop as a high-speed arbitrary waveform generator and contains diagnostic features including a special ADC snapshot capture memory. This paper describes the overall system, the feedback processor and focuses on the hardware architecture, design and implementation.

Introduction and Background

Introduction:

►High Intensity LHC beam in known to cause transverse instabilities driven by the electron cloud effect and Transverse Mode Coupled Instabilities (TMCI) in the SPS.

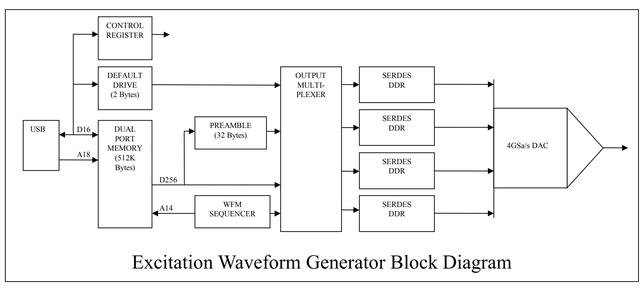
► A research and development effort has been undertaken between CERN and SLAC under the auspices of the US LHC Accelerator Research Program (LARP) to develop techniques for controlling these using feedback.

►Goal: Achieve feedback control of intra-bunch instabilities

Previous Work:

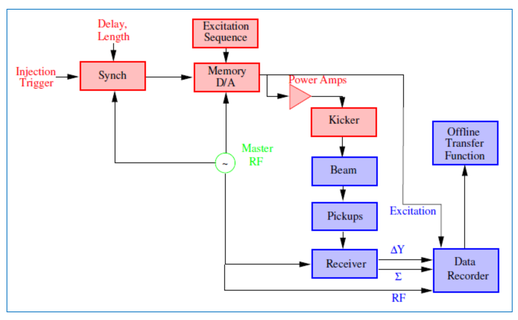
►Simulation and modeling effort based on numerical models and measurements of driven beam motion

►A special Excitation System, essentially a 4GSa/s arbitrary waveform generator, was developed to drive the beam with time-domain stimulus signals:



Excitation Waveform Generator Block Diagram

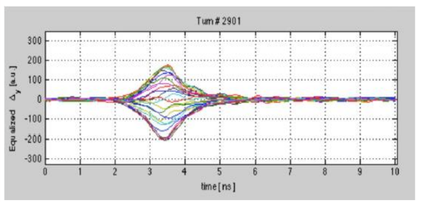
►Measurements made using this Excitation system produced results that were fed back to the numerical models, increasing accuracy and deepening our understanding of the system dynamics



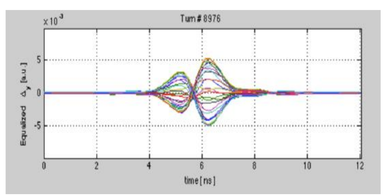
Block Diagram of Excitation System

-- Excitation System Diagram:
- Waveform generator (Memory D/A) drives RF Power Amps to Kicker
- Beam motion measured by stripline pickups, and conditioned by receiver
- Receiver signal digitized by 40GSa/s Tektronix Oscilloscope

Measurements from the Excitation System

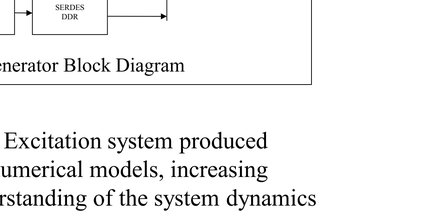


Barycentric Driven Motion

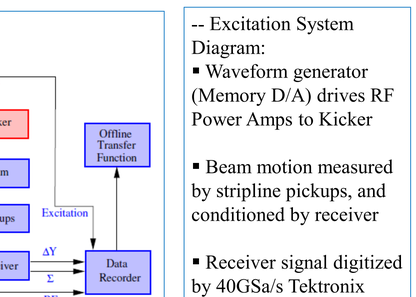


Head-Tail Driven Motion

RF Power Amplifiers in SPS Tunnel



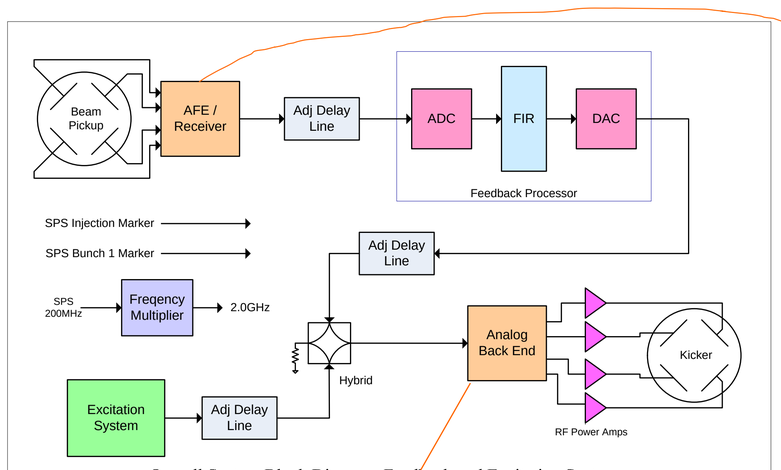
Excitation Waveform Generator Boards



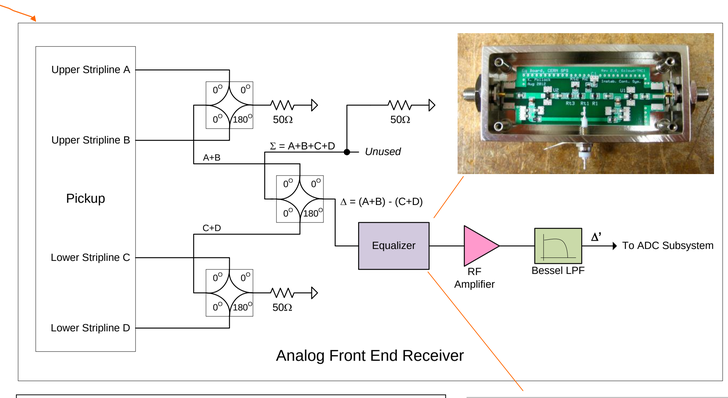
SPS Stripline Kicker Structure

►The above work has enabled us to proceed to the next step: A single-bunch Feedback Demonstrator System

Full System Overview

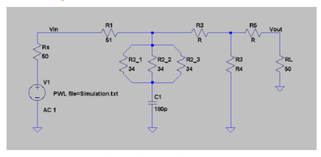


Overall System Block Diagram: Feedback and Excitation Systems

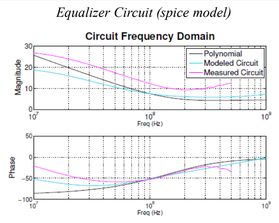


Analog Front End Receiver

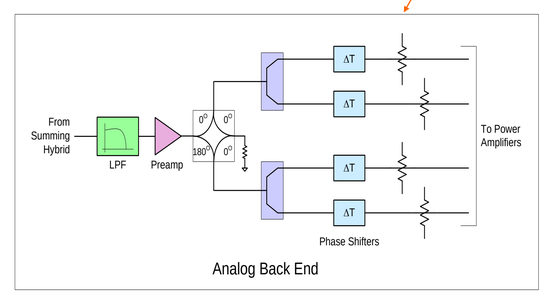
The Equalizer:
An analog equalizer was developed to compensate for amplitude and phase distortions introduced by the pickup and cabling. This compensation is necessary to allow us to properly apply a time-domain correction signal to the bunch. This work was done by K. Pollock, SLAC.



Equalizer Circuit (spice model)



Equalizer Frequency Response

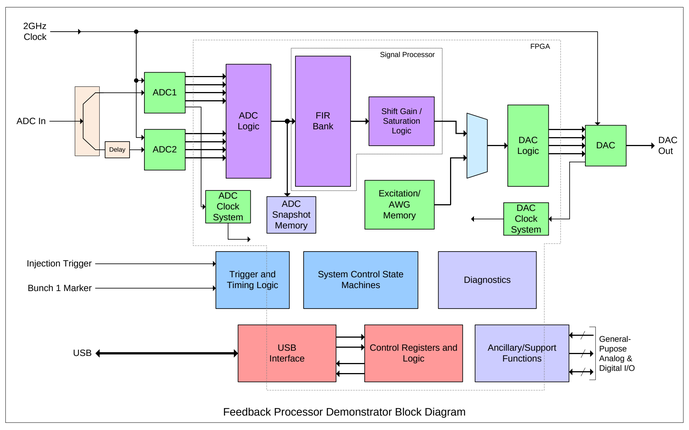


Analog Back End

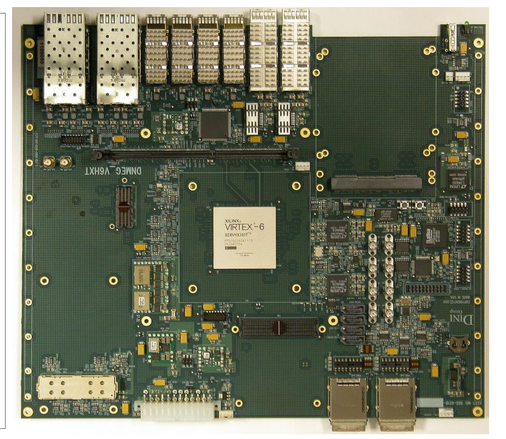
System Overview:

- We have built a single-bunch, ultrafast high bandwidth transverse feedback demonstrator system.
- This feedback system is essentially a high bandwidth re-configurable digital signal processing channel with an input ADC and output DAC capable of sampling at 4GSa/s. An FPGA implements the signal processor and the current design contains a 16-tap FIR bandpass filter.
- The feedback system acquires 16 samples or slices across one bunch, and outputs 16 correction samples, both at the 4GSa/s rate.
- For our measurements in the SPS, we the use Feedback and Excitation systems together, which allow us to drive the bunch into instability and then correct with feedback along the same signal path.
- Both sub-systems receive the RF Clock, Injection and Bunch 1 markers from SPS LLRF and Timing systems / used to synchronize and sequence operations;
- The 200MHz SPS RF Clock is multiplied to obtain the 2GHz sample clock, this clock is then doubled by the ADC and DACs to achieve 4GSa/s.
- Adjustable delay lines are included to align the input sampling, feedback output and excitation output to the beam bunch (10ps dly step resolution).
- RF Power Amplifier Specs: 0.02 to 1 GHz, 80 Watts (derated from 100W) / Manufacturer: Amplifier Research (Modular RF, Bothell, WA USA)

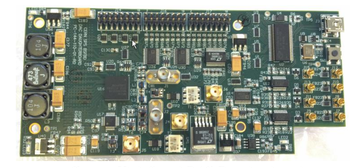
The Feedback Processor



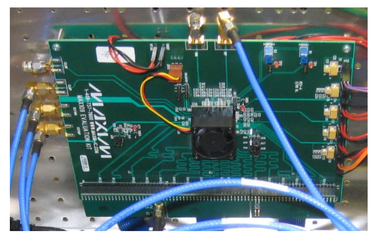
Feedback Processor Demonstrator Block Diagram



Commercial FPGA Motherboard



Custom High-Speed DAC Daughterboard



ADC Eval Board (1 of 2)

Feedback Processor:

- The Feedback Processor is a rapidly developed prototype, implemented using a mixture of commercial and custom-designed hardware. The entire system was designed, constructed and delivered to CERN in less than10 months.
- The design is modular, based around a commercial FPGA motherboard, with a custom-designed DAC daughterboard plus two commercial ADC evaluation boards. The ADC boards connect to the motherboard using a custom high-speed cable assembly, developed commercially (Samtec Corp). This design approach allowed us to quickly develop a solution within the confines of limited time and engineering resources.
- The custom DAC daughterboard contains the high-speed DAC, clocking circuits, trigger circuitry, general purpose analog and digital I/O and a USB 2.0 interface.
- The DAC is a Maxim Semi MAX19693 device (12-bit, 4GSa/s device used in 8-bit mode). The ADC is a MAX109 device (8-bits, 2GSa/s), two ADCs are used in interleaved mode to achieve the effective 4GSa/s rate. We used two MAX109 EVM evaluation boards to implement the ADC subsystem.
- All signal processing is implemented in the motherboard Xilinx Virtex-6, XC6VHX565T FPGA. The present design implements a bank of 16, 16-tap FIR filters. The filters are bandpass type, centered at the betatron frequency. The FIR Filters follow the relation:

$$y(n) = \sum_{k=0}^{15} h(k)x(n-k)$$

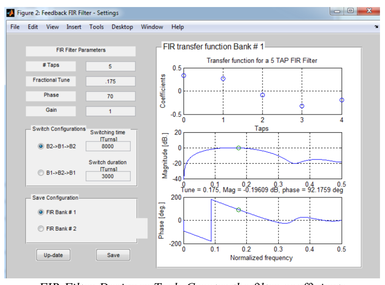
- Diagnostic features include a special ADC snapshot memory that allows us to selectively capture up to 65536 turns of pre-processed ADC data and save for later analysis.
- Feedback Processor can also operate as an excitation driver (arbitrary waveform generator) as well.
- All processing takes place on edges of the SPS RF clock. Acquisition, processing and output operations are sequenced from the SPS Injection and Bunch 1 marker signals.

System Chassis: all boards, cabling, cooling & power supply are packaged inside

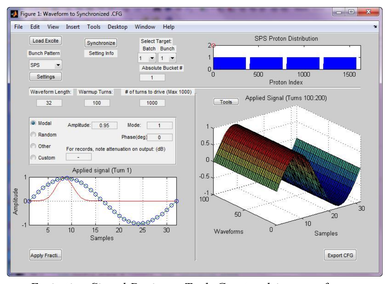
Custom High-Speed ADC cable assembly: mates ADC eval boards to FPGA motherboard

System Software

MATLAB Applications Developed for our System:



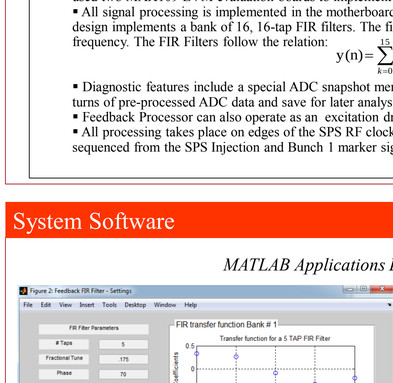
FIR Filter Designer Tool: Creates the filter coefficients



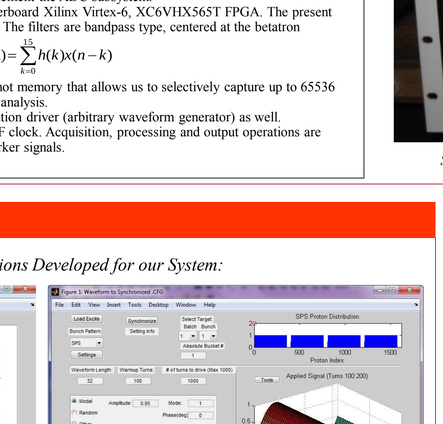
Excitation Signal Designer Tool: Creates drive waveforms

System Software:

The system control and data transfer software is GUI based and developed in Microsoft Visual Basic 2010. The GUIs interface with the system over USB using driver calls. A suite of offline MATLAB-based applications have been developed to facilitate configuration of the feedback mode, generation of excitation data files, design of the FIR filters, and analysis and display of the ADC snapshot data. Transfer between Visual Basic and MATLAB is done using text based configuration and data files, generated automatically by the SW. The Software runs on a Windows 7 PC. All USB I/O uses Windows driver calls. Additional off-line Matlab tools have been developed for data analysis and simulation.

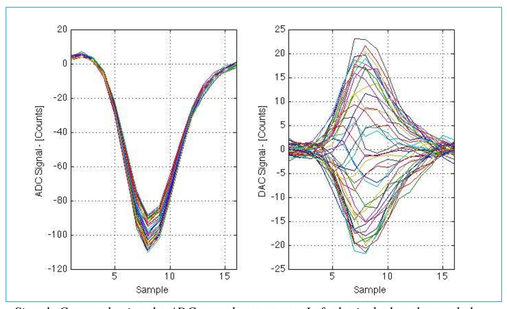


Chassis Setup and Mode Control GUI

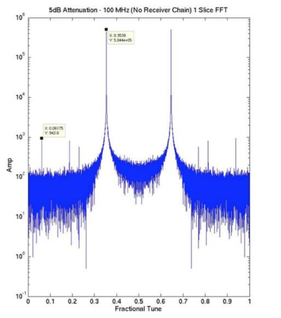


Visual Basic System Control GUIs *FIR Setup GUI*

Results



Signals Captured using the ADC snapshot memory: Left plot is the bunch sampled over 40 turns. Note the Gaussian signal shape and the motion in the bunch. The right plot shows the feedback system DAC output, note the feedback in action: the drive signal is increased based on the motion of the beam. All 16 samples are plotted in each case.



ADC SFDR Test: Single 100MHz tone is injected into the ADC (bypassing the AFE). We find the SFDR to be around 54dB (datasheet shows 61dB).

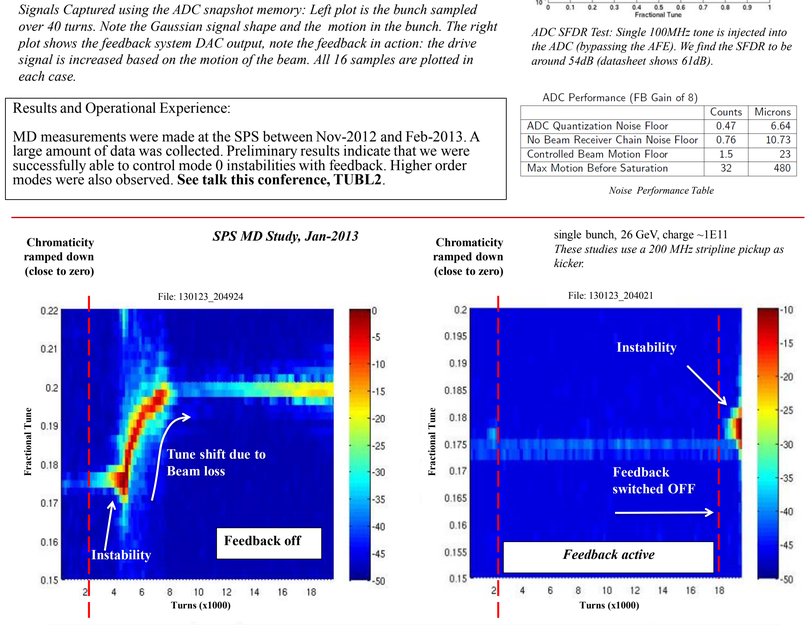
Results and Operational Experience:

MD measurements were made at the SPS between Nov-2012 and Feb-2013. A large amount of data was collected. Preliminary results indicate that we were successfully able to control mode 0 instabilities with feedback. Higher order modes were also observed. **See talk this conference, TUBL2**.

ADC Performance (FB Gain of 8)

	Counts	Microns
ADC Quantization Noise Floor	0.47	6.64
No Beam Receiver Chain Noise Floor	0.76	10.73
Controlled Beam Motion Floor	1.5	23
Max Motion Before Saturation	32	480

Noise Performance Table



single bunch, 26 GeV, charge ~1E11
These studies use a 200 MHz stripline pickup as kicker.

- **Feedback stabilizes the bunch** !
- clearly working for dipole mode
- confirms high sensitivity of receiver circuit
- confirms feedback possible with the very small kick strength of ~1 kV [transverse]

W. Hofle, CERN

►The above work has enabled us to proceed to the next step: A single-bunch Feedback Demonstrator System

2013 International Beam Instrumentation Conference, Oxford UK

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