



# DEVELOPMENT OF THE SIRIUS RF BPM ELECTRONICS

D. O. Tavares, R. A. Baron, F. H. Cardoso, S. R. Marques, J. L. B. Neto, L. M.  
Russo, LNLS, Campinas, Brazil

A. P. Byszuk, G. Kasprowicz, A. J. Wojeński, Warsaw University of Technology,  
Warsaw, Poland

A Beam Position Monitor (BPM) system is being developed for the new low-emittance 3 GeV Brazilian synchrotron light source, Sirius. The Sirius BPM electronics is a modular system based on a [PICMG® MicroTCA.4](#) platform using ADC mezzanine cards in [ANSI/VITA 57.1 FMC form factor](#) and standalone RF front-end boards. It has been designed under the CERN Open Hardware License (OHL) by the Brazilian Synchrotron Light Laboratory (LNLS) in collaboration with the Warsaw University of Technology (WUT).

Sirius is a new 3 GeV synchrotron light source under construction in Brazil [1], targeting a 0.28 nm.rad natural emittance. The commissioning of the storage ring should start in the first quarter of 2016.

In total there will be more than 320 RF BPM pick-ups, from which 240 button BPMs along the 518 meters of the storage ring circumference (12 per super period), 50 BPMs on the booster and more than 30 BPMs on the LINAC and transfer lines.

The development of an RF BPM electronics for Sirius started in the second semester of 2010, following two main directives:

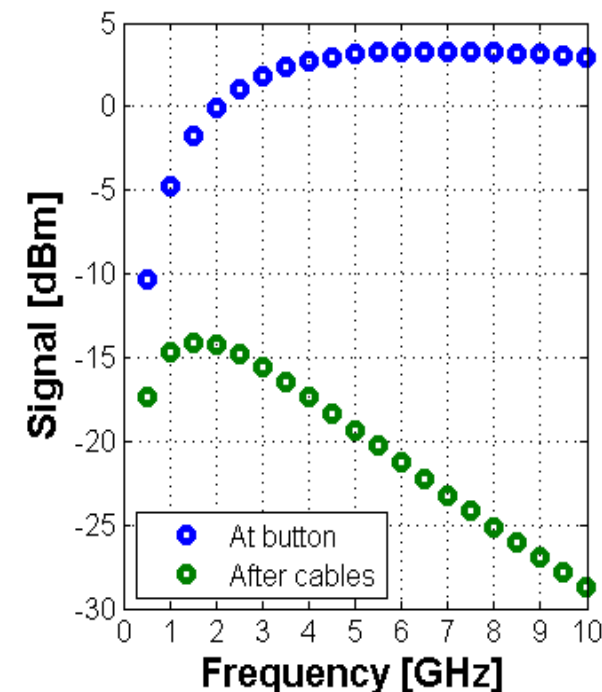
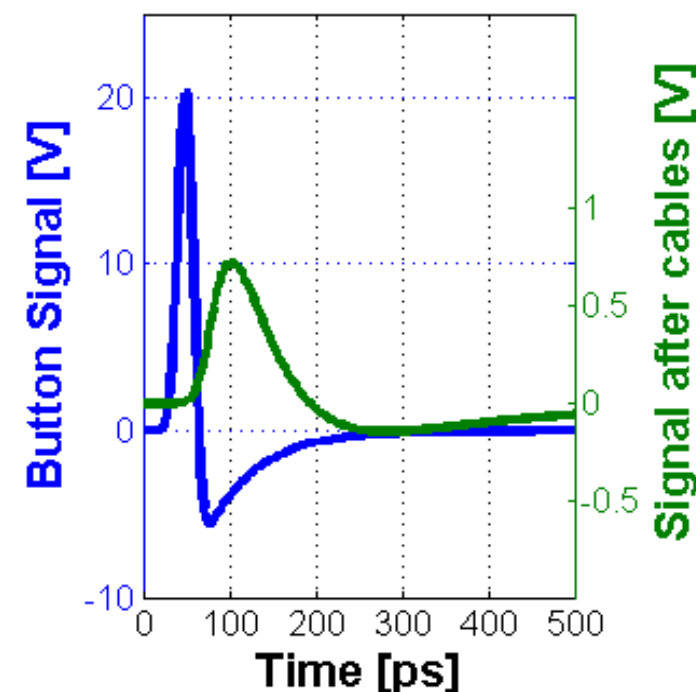
- i) **design a modular and reconfigurable system (hardware and software) to be used in accelerator applications other than BPMs;**
- ii) **adopt a collaborative approach for the development in order to strengthen its performance and usability on the scientific instrumentation community.**

# System Requirements / Beam Signal



General requirements for Sirius's storage ring electron beam stability.

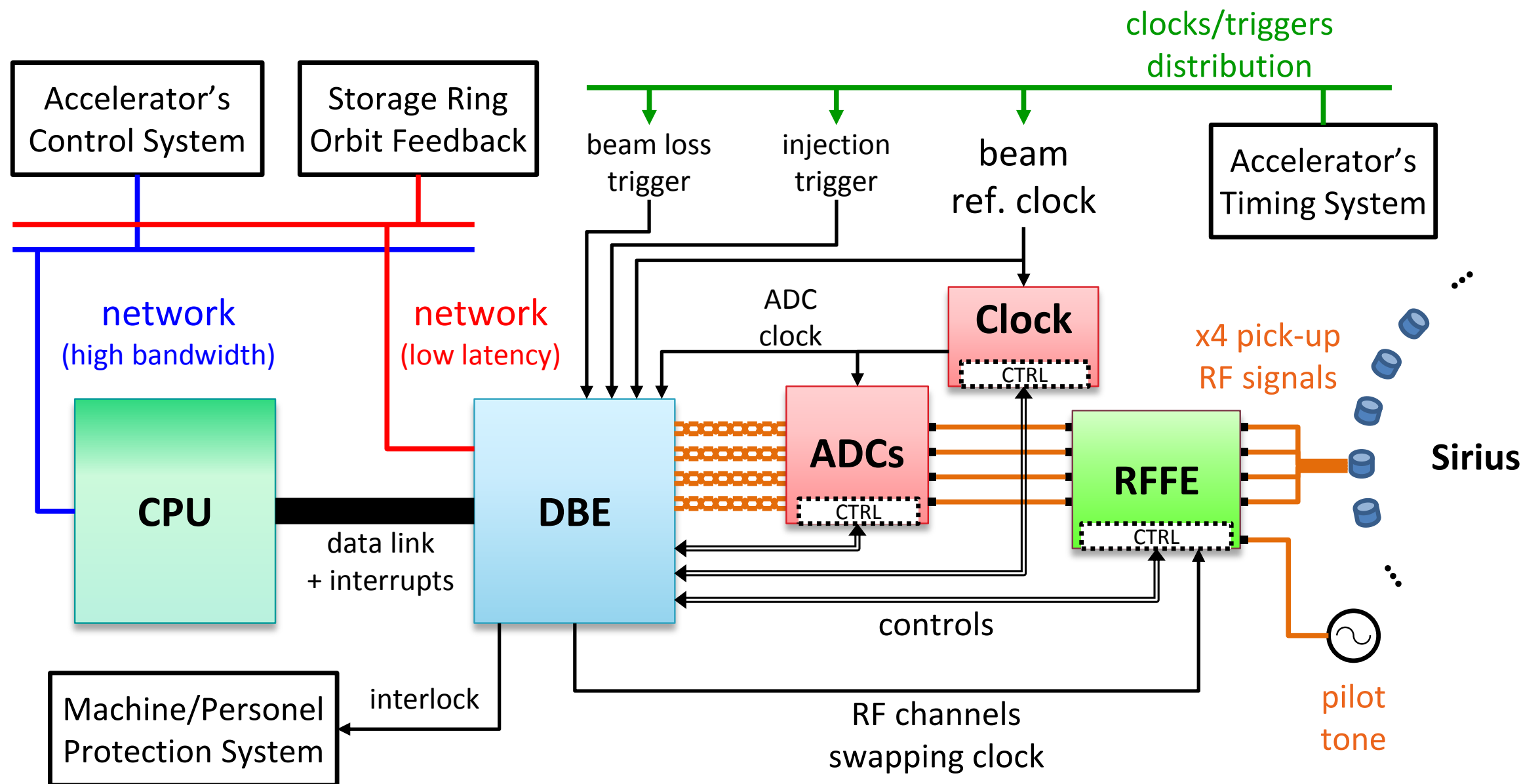
Parameter	Value
Resolution (RMS) @ 0.1 to 1000 Hz	$< 0.14 \mu\text{m}$
Resolution (RMS) @ turn-by-turn full bandwidth	$< 3 \mu\text{m}$
1 hour position stability (RMS)	$< 0.14 \mu\text{m}$
1 week stability (RMS)	$< 5 \mu\text{m}$
Beam current dependence (w/o top-up)	$< 1 \mu\text{m}$
Beam current dependence (w/ top-up)	$< 0.14 \mu\text{m}$
Filling pattern dependence	$< 5 \mu\text{m}$
First-turn resolution (RMS)	$< 0.5 \text{ mm}$
Horizontal/Vertical plane coupling	$< 1\%$



Simulation of the RF voltage signal at button pick-ups and after LMR195 cables of a 500 mA multi-bunch beam with ideal 100% filling: (a) Time-domain; (b) Frequency-domain (RF frequency harmonics).

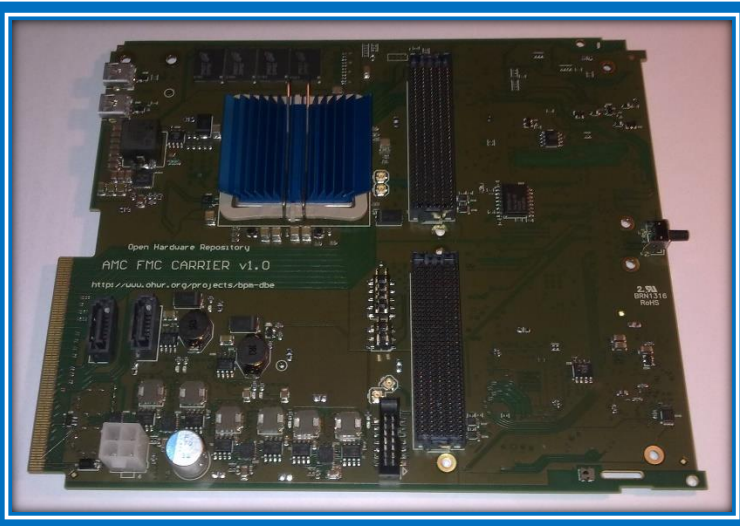


# System Architecture

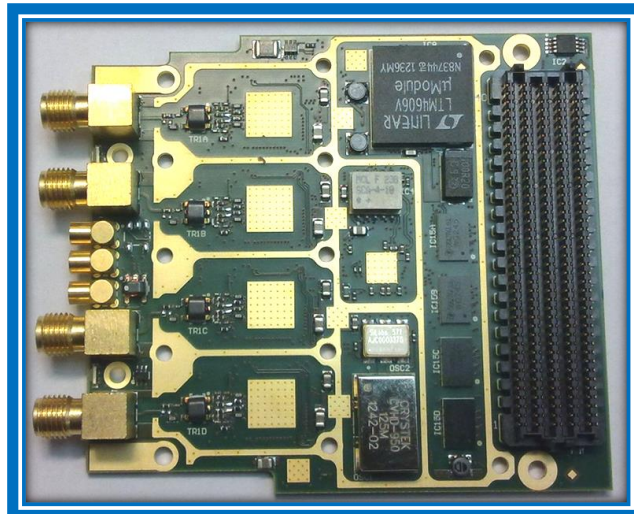


# System Architecture

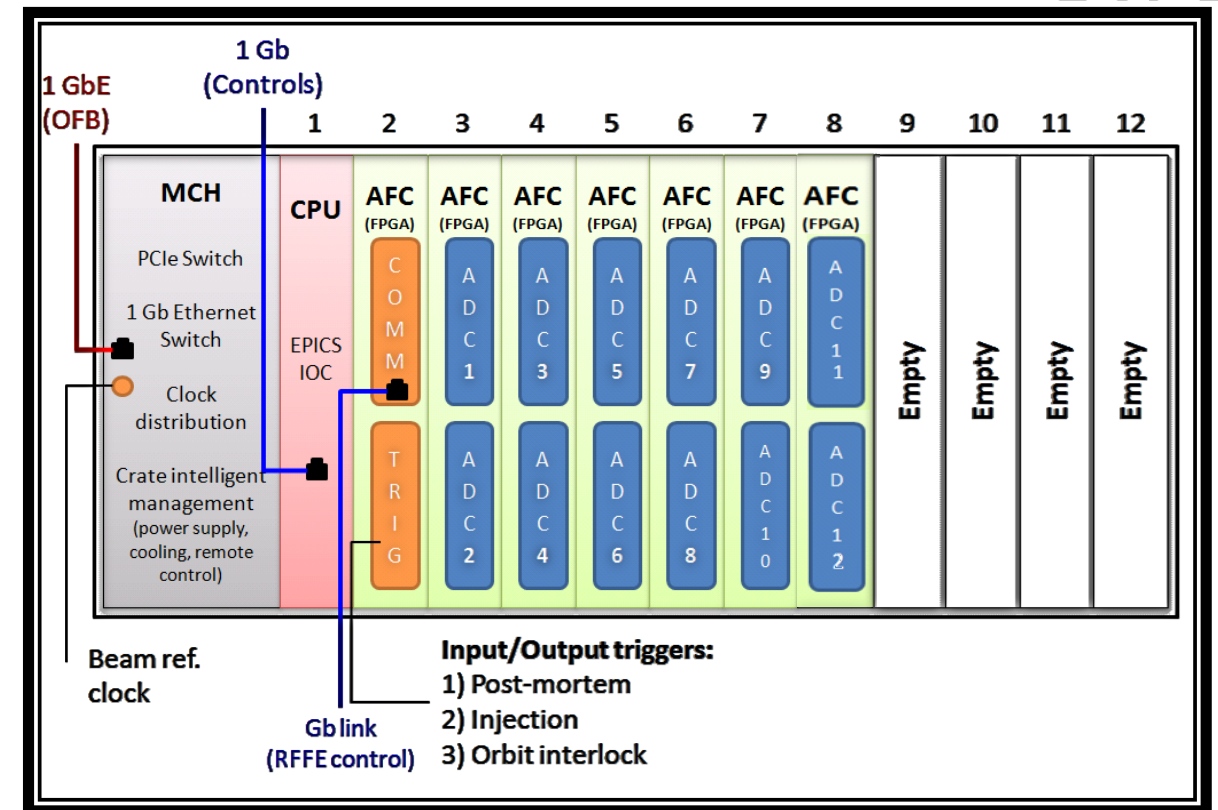
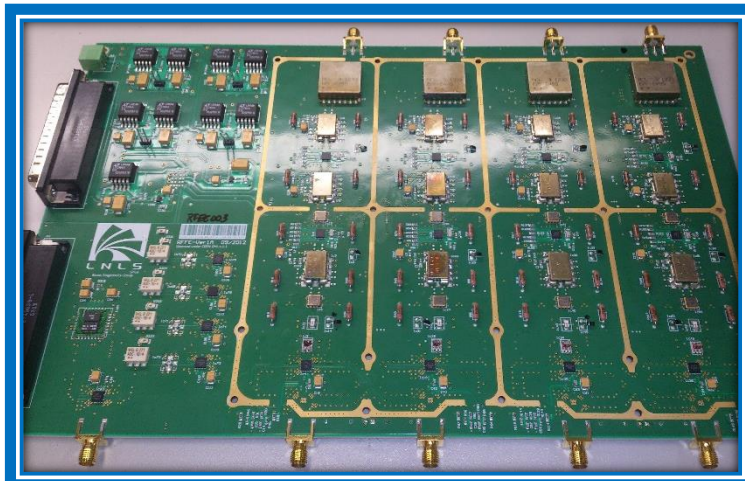
AMC FMC carrier



130 MS/s –LTC2208



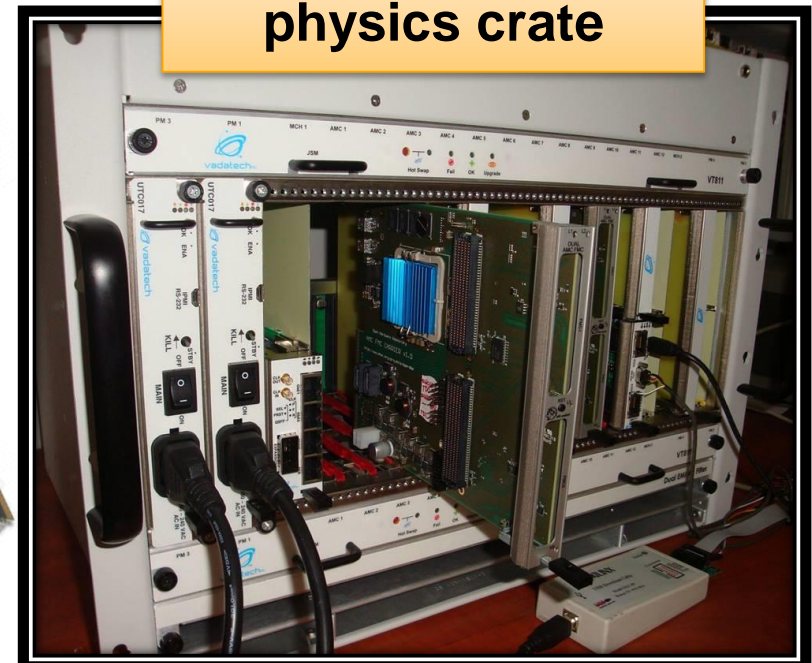
RFFE



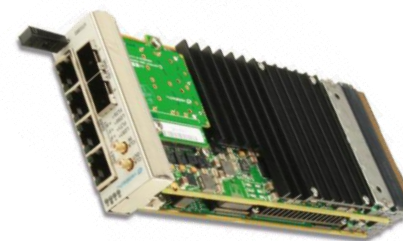
CPU



MicroTCA for physics crate



MCH

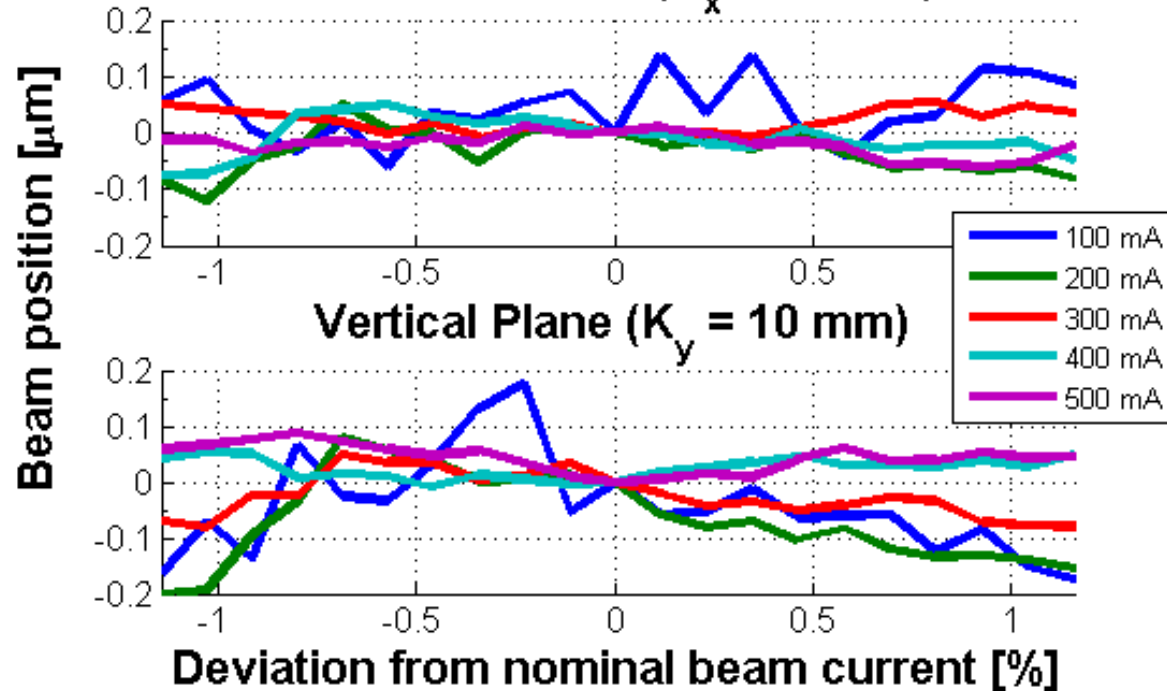




# Laboratory Tests

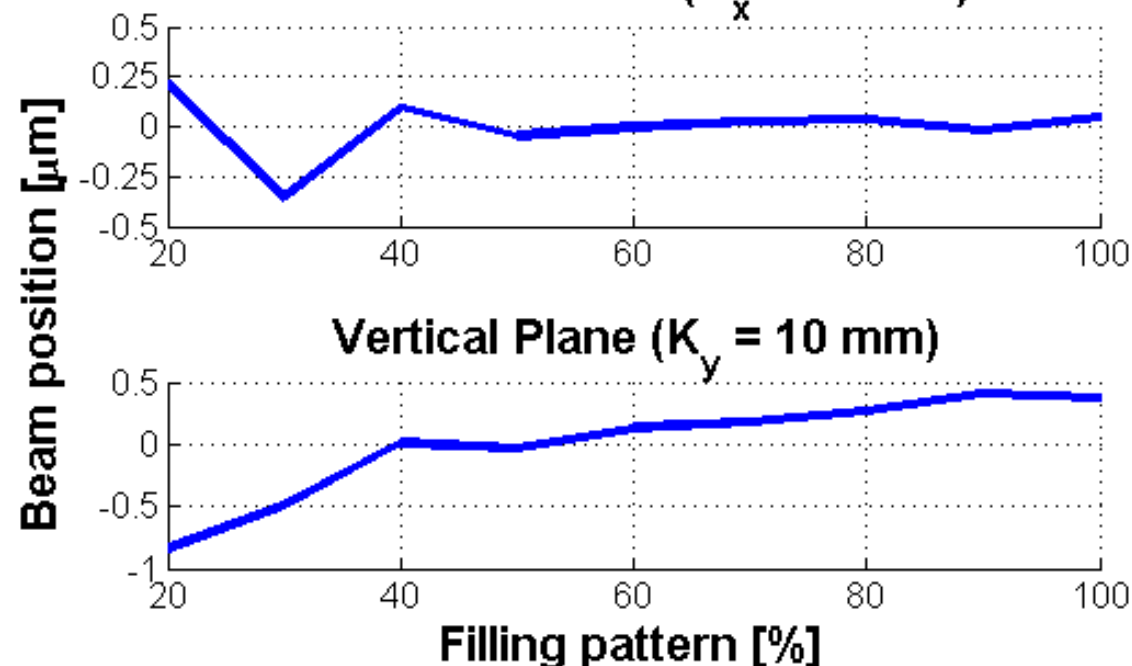
## Beam current dependence (BCD)

Horizontal Plane ( $K_x = 10$  mm)



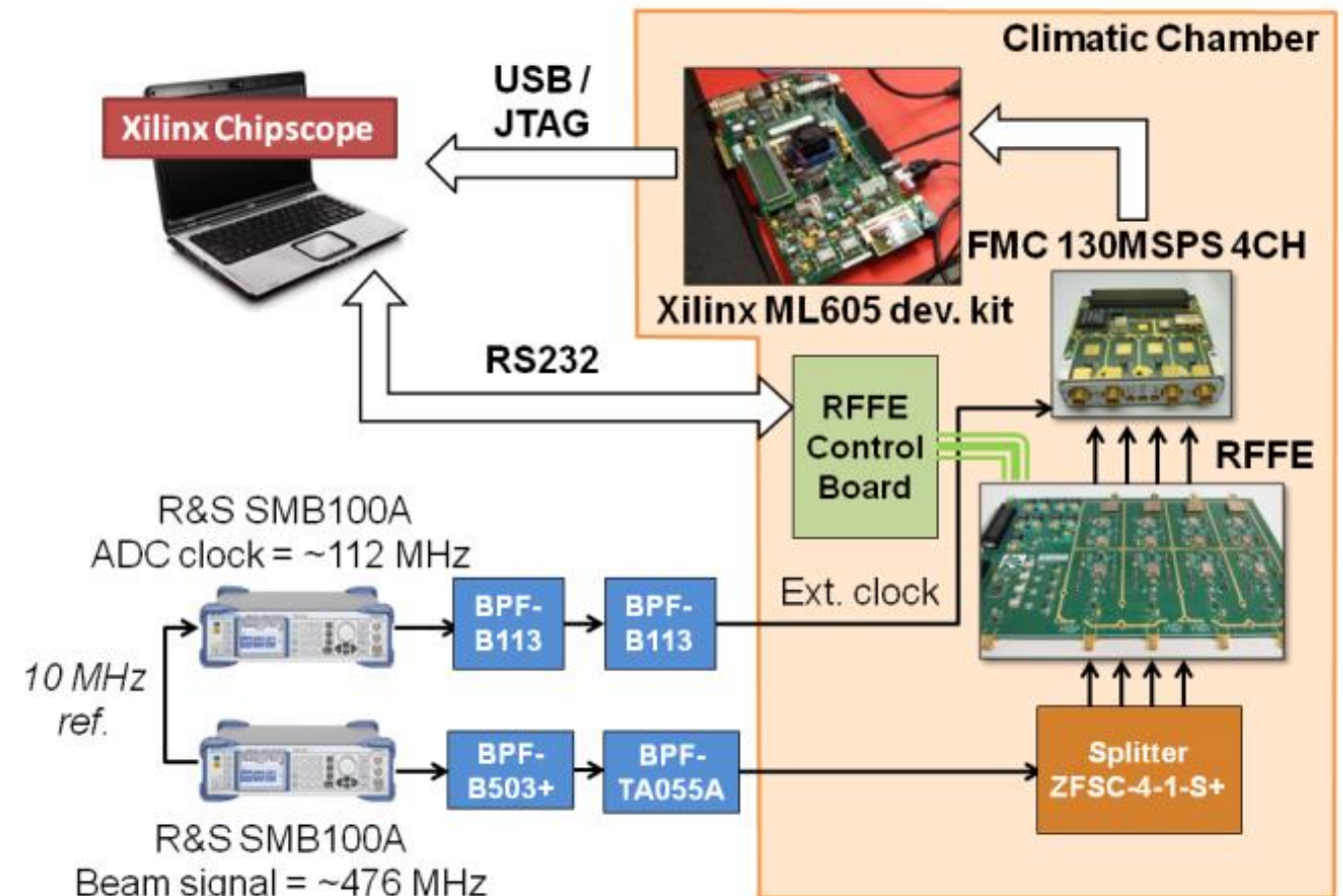
Vertical Plane ( $K_y = 10$  mm)

Horizontal Plane ( $K_x = 10$  mm)



Vertical Plane ( $K_y = 10$  mm)

## Filling pattern dependence (FPD)



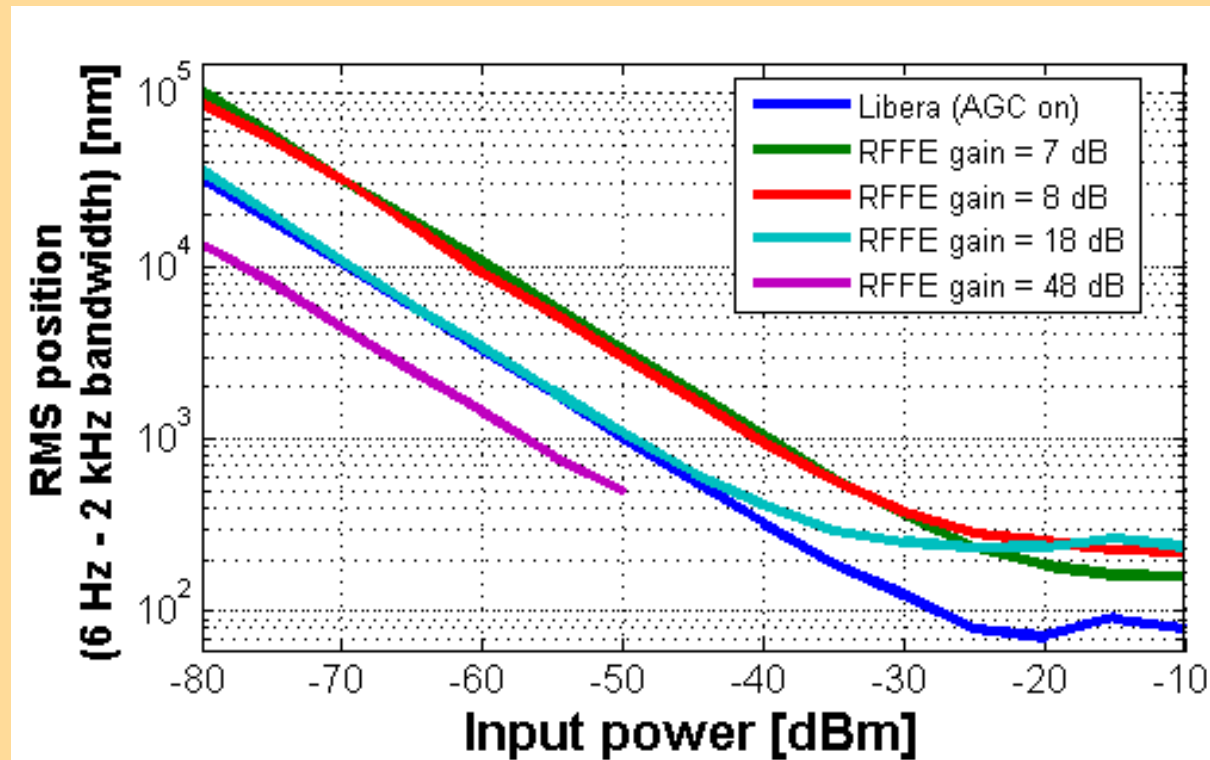
Experimental setup for the Sirius BPM electronics prototype evaluation

The first bench tests results show that the BCD, FPD and long-term stability figures of the Sirius BPM electronics for centered beams are partially or entirely in accordance with the specifications.

# Laboratory Tests



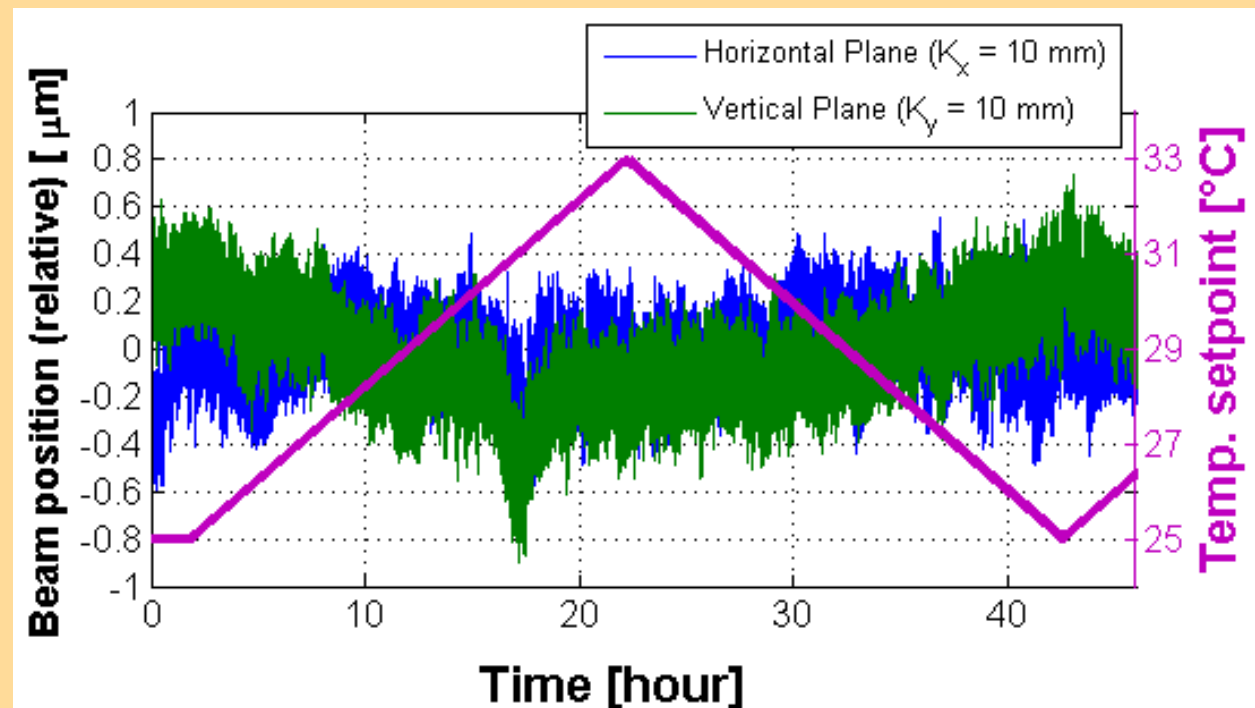
65536 points collected in each run;  
Data rates: 100 kS/s for Sirius BPM / 10 kS/s for Libera;  
Switching OFF;



- RFFE gains of 8 and 18 dB achieve position resolution for higher power inputs that cannot reach values lower than ~230 nm;
- Libera Brilliance+'s lower limit for very similar test conditions is below 100 nm;
- RFFE gain of 7 dB achieve ~160 nm;

When the output attenuation is increased, the signal level at the ADC inputs is decreased without great impact to the overall noise figure

The temperature dependence was kept below 140 nm for the long term run under a temperature variation (8 °C) much larger than expected for the real setup at Sirius ( $< 1$  °C). The requirement of long-term stability and temperature dependence is not a limiting factor of performance for the BPM electronics under consideration.



- BCD, FPD and long-term stability figures of the Sirius BPM electronics for centered beams are partially or entirely in accordance with the specifications;
- Major improvements in the resolution for high input powers must be done;
- Systematic studies must also be carried out with off-centered beams;
- Second version of all hardware is underway. Small impedance matching issues were found on the ADC boards and will be investigated. The RFFE can be still improved by simplifying the calibration schemes, taking the power supply out of the board and with simplification of the onboard temperature control.
- Several FPGA firmware and software functionalities will be implemented:
  - Final port of the digital signal processing chain to the AMC FPGA board;
  - Amplitude and phase compensation;
  - De-spike for switching mode of operation;
  - Automatic gain control;
  - Distribution of the revolution frequency clock;
  - Triggered acquisition support;
  - Integration with the distributed control system;
  - Implementation of the interlock mechanism.