FIRST TESTS OF THE TOP-UP GATING AT SYNCHROTRON SOLEIL

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Abstract

Since 2006, Synchrotron SOLEIL is producing photons. The beamlines became operational for the users in 2008. Until 2012, thanks to the excellent performances of the injection system of the storage ring, the perturbation on the position of the stored beam during Top-up injection was small enough to be accepted by the users. For some specific experiments requesting higher beam stability, few beamlines expressed their wish to be able to freeze the data acquisition during the injection. To fulfill this need, the diagnostics group of Synchrotron SOLEIL designed the "TimEX3" board which was integrated into the timing system in order to allow the gating of the Top-up injection. This design was released as open hardware. Towards this aim, we decided to design it with the open source and free EDA software "KiCad", and to make it available under the CERN's Open Hardware Repository.

INTRODUCTION

Synchrotron SOLEIL, a French 3rd generation synchrotron light source, is delivering a stable photon beam to its users in Top-up mode (continuous injection of electrons in the storage ring). The electron beam current variation in the storage ring is held within a 0.5% boundary. But each new injection in the storage ring affects during a few ms the position of the stored beam. The aim is to keep this orbit perturbation below 1/10th of the beam transverse size.

The injection in the storage ring is made by 4 fast kickers with a very good matching of their magnet fields [1]. Many improvements of the storage ring pulsed magnetic systems allowed to achieve an injection bump which amplitude is 70 µm RMS in horizontal and 40 µm RMS in vertical [2], during a very short time of about 7 ms.

These performances allow most users of SOLEIL to work without noticing any perturbation on the beam during the Top-up injection. But pushing always further the limit of their experiments, some beamlines are now sensitive enough to be disturbed by the residual injection bump effect.

The Top-up gating allows them to stop the data acquisition during the injection or to be able to surround and extract those data before processing their experimental results.

SOLEIL TIMING SYSTEM

The kickers are triggered by the timing system which can be used to signal an injection to the beamlines before it occurs.

SOLEIL's timing system is based on master (CENTRAL) device and slave boards (LOCAL) [3]. The architecture is depicted in Fig. 1. The CENTRAL system generates frames containing the booster clock, the storage ring clock, and events. Up to 255 events may be defined by the user. LOCAL boards receive the optical frames. Each of the 8 outputs of a LOCAL board is configured to trigger upon a given event.

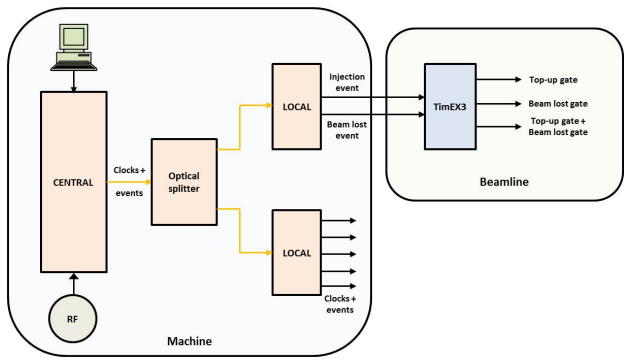

Figure 1: SOLEIL timing system architecture.

THE TOP-UP GATING

Two events are dedicated to the Top-up gating. One to warn before an injection occurs (pre Top-up), and the other one to signal when the beam is lost (figure 2).

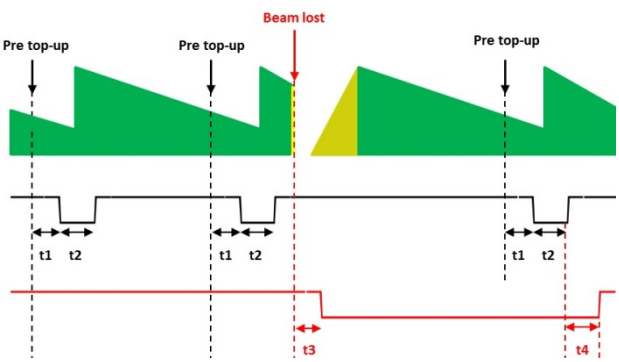

Figure 2: Top-up gating timing.

The pre Top-up event is sent approximately 2 s before the injection. After a hold off delay (t1), the top-up gating signal is activated during t2 seconds. The beam lost event is sent when the current falls below a limit. After a hold off delay (t3), the signal remains activated until the end of the first Top-up injection. Therefore, we don't need a specific event for beam recovery. Additionally, the user may keep the signal activated for an extra delay (t4). This may be useful in case that the beamline needs to stabilize the temperature of some optical devices before starting again the data acquisition.

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ISBN 978-3-95450-127-4

Because the storage ring electron beam current value is also broadcasted over all beamlines, users can use it to stop the data acquisition by software means, without using the gating signals. The choice between the hardware and the software solution depends mainly on the device to drive and whether it is sensitive to the current value or to the injection perturbations.

The timing system at SOLEIL does not allow the Top-up gating described above. It can only provide a 10 µs width pulse for each event with a limited offset delay range. To fulfill the requirements, we developed the TimEX3 board.

TIMEX3 BOARD

The TimEX3 board is a multipurpose compact PCI board designed to perform simple to medium complex logical functions. It is used for the timing system of SOLEIL (signal duplication, Top-up gating, etc.). This board is based on a XILINX's Spartan-6 FPGA (figure 3).

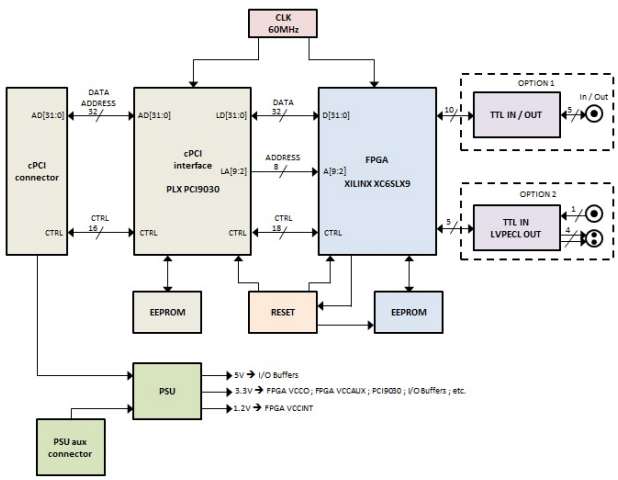

Figure 3: TimEX3 architecture.

The FPGA communicates with the compact PCI bus through a PLX's PCI9030 interface. This chip is connected to the FPGA with a simple 60MHz, 32 bits microprocessor bus. An 8 bit address range and 2 chip selects provide 2kB of memory which is enough for the TimEX3 needs. The IOs can be configured either as inputs or outputs. The configuration is fixed during the manufacturing by soldering the corresponding components. In Top-up gating mode, the board is configured with 2 inputs and 3 outputs. The 2 inputs are connected to the pre Top-up and beam lost event triggers provided by a LOCAL board. The first output provides the Top-up gating, the second the beam lost gating and the third one is the combination of these two signals.

The TimEX3 board was developed as an open hardware project. All source files (CAD, EDA, Gerber, VHDL, etc.) are available on CERN's Open Hardware Repository [4] and may be used under the CERN's open hardware licence [5]. This design was also an opportunity to evaluate the KiCad software [6] for the creation of the schematics and of the printed circuit board. KiCad is free and open source EDA (Electronic Design Automation). Using KiCad instead of usual commercials EDA tools allows us to share more easily and widely our development with the open hardware community as anyone can download and use KiCad without any cost or licence restriction. Even if today KiCad lacks some functionalities to be able to fully replace commercials software, our experience with it was positive and it can be used in a wide range of projects [7].

With the TimEX3 board the users can adjust the delays (t1, t2, t3 and t4) by steps of 1 ms over a range of more than 1000 hours. This board was first used by SMIS beamline, one of the two Infrared beamlines at SOLEIL.

FIRST RESULTS ON SMIS BEAMLINE

SMIS beamline is aiming to deliver an infrared beam of high brilliance in the 1-100 µm spectral range, with a spectral region optimized for investigation between 2.5-100 µm. This synchrotron source is coupled to an infrared microscope and spectrometers. The beamline is dedicated to microscopic analysis of a variety of samples, spanning from polymer films and multilayers, mineral inclusions, biological and biomedical studies, to archaeology. In general, infrared beamlines are very sensitive to instabilities [8].

For such micron-range wavelengths region, a Michelson type interferometer is used instead of a monochromator. The scan time can vary between 0.25 s to several minutes. After the interferogram recording, a fast Fourier processing (FFT) transforms the intensity-time domain into intensity-frequency domain. To improve the signal to noise ratio, scans are accumulated. The total recording time for one spectrum can range between few seconds to minutes, depending upon the number of accumulated scans. Figure 4 shows the injection spikes recorded during a scan.

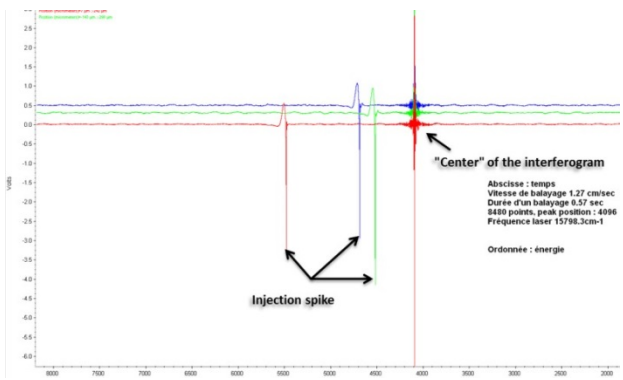

Figure 4: injection spikes recorded during a scan.

During the accumulation, the interferogram is strongly perturbed and degrades markedly the signal quality as it can be seen on the fast Fourier transform in Fig. 5. The red curve is a scan with Top-up gating activated whereas the green one is without gating.

ISBN 978-3-95450-127-4

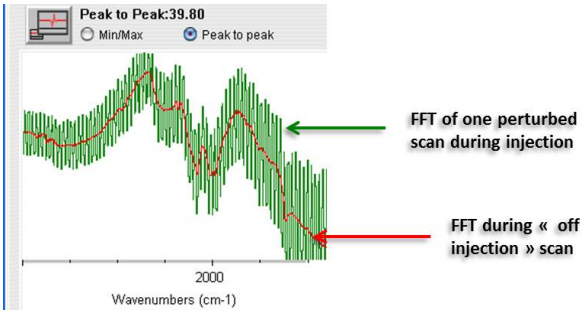

Figure 5: FFT of a scan with and without Top-up gating.

The Top-up gating has improved the signal to noise of the spectrum by a factor of 12 to 15. It's a very significant enhancement for the data quality recorded at SMIS beamline.

CONCLUSION

It took a few years before the Top-up gating becomes required at SOLEIL. SMIS greatly improved some of its acquisitions by using it. Today, it is also used by AILES beamline, and other beamlines are asking for it. The design of the TimEX3 board allows us to meet the needs of the beamlines in a simple and efficient way.

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