PERFORMANCE MEASUREMENTS OF THE NEW X-BAND CAVITY BPM RECEIVER*

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Abstract

SLAC is developing a new X-band Cavity BPM receiver for use in the LCLS-II. The Linac Coherent Light Source II (LCLS-II) will be a free electron laser (FEL) at SLAC producing coherent 0.5-77 Angstroms hard and soft x-rays. To achieve this level of performance precise, stable alignment of the electron beam in the undulator is required. The LCLS-II cavity BPM system will provide single shot resolution better than 50 nm resolution at 200 pC [1]. The Cavity BPM heterodyne receiver is located in the tunnel close to the cavity BPM. The receiver will processes the TM010 monopole reference cavity signal and a TM110 dipole cavity signal at approximately 11 GHz using a heterodyne technique. The heterodyne receiver will be capable of detecting a multibunch beam with a 50ns fill pattern. A new LAN communication daughter board will allow the receiver to talk to an inputoutput-controller (IOC) over 100 meters to set gains, control the phase locked local oscillator, and monitor the status of the receiver. We will describe the design methodology including noise analysis, Intermodulation Products analysis.

BPM REQUIREMENTS

The LCLS-II Project concept has been developed to provide the new facilities with two new, independently controllable x-ray sources in a new undulator hall, it will be possible to simultaneously provide tunable soft and hard x-ray beams, one optimized for 250-2,000 eV photons and the other optimized for 2-13 keV. Each undulator segment will be a variable gap permanentmagnet planar hybrid device with a nominal minimum gap height of 7.2 mm and a total segment length of 3.40 m. The Hard X-ray (HXR) Undulator is made up of 26 individual undulator segments, each with 106 32- mmlong periods. The Soft X-ray (SXR) Undulator is made up of 15 individual undulator segments, each with 61 55mm-long periods. Table 1 illustrates the design differences between LCLS-I and LCLS-II.

| Table 1. Specifications Differences | | | | |
|-------------------------------------|-------------------|-------------|-------------------------|--|
| | LCLS-I | LCLS-II | Comments | |
| Frequency | 11.384 GHz | 11.424 GHz | multibunch | |
| Output | Waveguide | coax | More flexible | |
| Tuning | 12 tuning stubs | <= 4 tuners | Lower cost | |
| Receiver | 14dB I.L. with 28 | <= 3dB I.L. | Improved noise figure | |
| | dB Gain step | 1 dB step | and dynamic range | |
| Digitizer | SLAC/VME | uTCA | Lower cost | |
| Ref. cavity | Single output | 2 couplers | Improved mode centering | |

Table 1: Specifications Differences

*Work supported by U.S. Department of Energy under Contract Numbers DE-AC02-06CH11357 and DE-AC02-76SF00515 and CRADA 13-230C

SYSTEM DESIGN

The major subsystems for the LCLS undulator BPM system are the cavity BPM, receiver, and data acquisition components as shown in Fig. 4. The cavity BPM and downconverter reside in the tunnel while the analog-to-digital converters (ADC) and processing electronics are in surface buildings.

Forty-one BPMs are installed on both HXR and SXR undulator girders while there others placed in the linac-toundulator (LTU) transport line. The BPMs provide stable and repeatable beam position data for both planes on a pulse-to-pulse basis for up to a 120-Hz repetition rate.



Figure 1: BPM Cavity with electric fields of position (dipole) and reference (monopole) cavities.

X-Band Cavity

Figure 1 shows the cavity BPM design by Pohang under a cooperative research and development agreement (CRADA) 13-230C. Beam passes through the monopole reference cavity on the right, exciting the TM_{010} monopole mode signal resonant at 11.424 GHz. The specifications of the Monopole are illustrated in Table 2.

Table 2: Reference Cavity Specifications

| Tuble 2. Reference cuvity specifications | | | |
|--|--|--|--|
| Value | | | |
| 11.424 GHz | | | |
| +-10 MHz | | | |
| $\geq 10 \text{ V/nC}$ | | | |
| \geq 15 Ω | | | |
| ~2438 | | | |
| TM_{110}, TM_{020} | | | |
| | | | |

The TM₁₁₀ dipole cavity is located 36 mm downstream through the 9-mm-diameter beam pipe. The position cavity dipole mode is resonant at 11.424 GHz, its output proportional to the product of beam position and bunch charge. The X and Y position modes are nominally degenerate in frequency, with the appropriate component chosen by the geometry of the couplers. The dipole coupler geometry is chosen to reject (the generally larger) monopole modes [2-6]. The dipole cavity was designed as a 4-port device with two opposing X couplers orthogonal to two opposing Y couplers. This is useful for cold testing and preserves symmetry. Unused ports are terminated with the potential for using them for future diagnostics. Table 3 specifies the position cavity.

Table 3: Position Cavity Specifications

| Parameter | Value |
|-----------------------------|---|
| Frequency TM ₁₁₀ | 11.424 GHz |
| Tolerance TM ₁₁₀ | +-5 MHz |
| Loss Factor | $\geq 13 \text{ V/mm}^2/\text{nC}$ |
| R/Q | $\geq 3.5 \ \Omega/\mathrm{mm}^2$ |
| Q _{ext} | 2000-3000 |
| Mode centering | < 30 micron |
| Offset due to Ref cavity | < 30 micron |
| coupling | |
| Mode frequency splitting | $\Delta F < 2 MHz$ |
| Other modes | TM ₀₁₀ , TM ₀₂₀ , TM ₂₁₀ , |
| | TM_{120} |
| Distance to ref. cavity | >= 4 pipe diameters |

BPMs were designed to a bandwidth of ± 5 MHz. The performance of the Cavity is illustrated in Fig. 2 and Fig. 3. The bandwidth of the cavity was measured to be 7 MHz. The Beta of the cavities was measured using a VSWR approach, Measuring the loaded Q each cavity was done using a S₂₁ 3dB bandwidth as illustrated in the figures. Another measurement of loaded Q was performed using a full-width-half-maximum and obtained similar results. From these measurements one can calculate the Q external and Q₀ using equation 1.

$$Q_{ext} = \frac{1+\beta}{\beta} * Q_L \text{ and } Q_0 = (1+\beta)Q_L \tag{1}$$



Figure 2: Reference Cavity Performance.



Figure 3: Dipole Cavity Performance.

The peak output voltage from the cavity can derived from equation 2. The R/Q was measured using a metal and ceramic bead.

$$V_{peak} = q\omega \sqrt{\frac{Z}{8} \left(\frac{R}{Q}\right) \frac{1}{Q_{ext}}}$$
(2)



Figure 4: System block diagram. The receiver is mounted on the undulator stand while the digitizers are upstairs.

Receiver

Since LCLS turn-on the cavity BPM receivers have been losing gain due to hydrogen poisoning, SLAC has

chosen to design a new receiver for LCLS-II that is low cost and with not have the effects of hydrogen poisoning using off-the-shelf integrated circuits. A four-channel heterodyne receiver (Fig. 7) mixes incoming X-band

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signals to a 25-60 MHz intermediate (IF) frequency. The receiver is designed to detect the beam when the FEL is configured for multi-bunch operation. Each receiver input is limited to a 35 MHz bandwidth around 11.424 GHz. Out-of-band filtering of -60 dB prevents higher from modes saturating the receiver input. Δ programmable attenuator was added to handle the dynamic range of the electronics instead of having a discrete gain switching of the receiver as in LCLS-I. Signals are amplified in a low noise stage (LNA), and then translated to the lower IF by using an image rejection mixer with a local oscillator (LO). Using Agilent Advanced design System (ADS) and S-parameters for the vendor, Fig. 5 illustrates the simulated image rejection of the receiver ~21dB.



Edit Baseband_Fled=(KF_Fled=12.0)

Figure 5: Image rejection of then receiver.

Further improvements have be made in communication with the receiver using a daughter card that contains a small form pluggable that can communicate over the large area network (LAN) to an input-output-controller (IOC) over 100 meters. This will allow the operators to set gains, control the Phase-Lock-Loop (PLL) oscillator, and monitor the status of the receiver.

The receiver is built on a composite board of Rogers material 4350 and FR-4. The Rogers material is the top and bottom cores while the FR-4 is the middle cores. This allows for the board to be rigid but have the dielectric constant for high frequency operation. The LO is generated using a low noise Phase-Locked Loop (PLL) with an integrated VCO were the reference locked to the master oscillator at 119-MHz. This board was designed at SLAC and is on another daughter card in the receiver chassis. It is important to note that the receiver board and the PLL were designed at a very broad frequency range from 11GHz to 13GHz. The PLL can be configured to run in a FracN or Integer mode. The phase noise of the PLL at 100 kHz offset is illustrated in Fig. 6.



Figure 6: Phase noise of the Lo Reference PLL.

The only parts that narrow operating range of the cavity BPM are the input filters which have a bandwidth of 200MHz.

The performance of the receiver has been measured to have a dynamic operating range of greater than 75dB. The output third order intercept is 30dBm.



Figure 7: Four-channel heterodyne receiver board.

ISBN 978-3-95450-127-4

Digitizer

SLAC has upgraded from VME to μ TCA as their new hardware platform. The X, Y, and Reference signals are digitized to 16 bits at a 119 MHz sampling rate in 4-channel μ TCA digitizers designed by SIS. Waveforms are transmitted over the backplane to a μ TCA processor which reduces raw waveforms to beam position and charge. Figure 8 illustrate the μ TCA rear transition module RTM and the digitizer an AMC module.



Figure 8: µTCA RTM and 119 MHz Digitizer.

The initial test on the digitizer has shown to have 11 effective number of bits with noise floor approximately - 120dB.

Software

An EPICS IOC communicates with the receiver via UDP messages. The receiver acts as a server, responding to commands and requests from the IOC. The IOC polls the receiver periodically for current register values and monitoring signals and provides this data via EPICS PVs. The IOC will control the SPI interface to the PLL, Attenuator control on the receiver board, and I2C interface that monitors temperatures, and power supply voltages. These set points PVs are also provided for users to control receiver. This allows the receiver to be configured for different beam currents. The PLL can be remotely configured for FracN or Integer modes of operation. When the IOC detects that the receiver has recovered from an outage, it reconfigures the receiver registers with the correct settings. Figure 9 illustrates the EPICS interface.



Figure 9: EPIC Cavity BPM interface panel.

SUMMARY

The two PCB boards (PLL and the Receiver) with other supporting components are integrated into a 19in chassis and installed on a shelf under the cavity BPM and Undulator. The Pohang Cavity was installed at the end of LCLS-I undulator and beam testing will begin later this year when LCLS-I turns back on.

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