UPGRADE OF THE READ-OUT ELECTRONICS FOR THE ENERGY BEAM POSITION MONITORS AT FLASH AND EUROPEAN XFEL

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Abstract

The dispersive sections of magnetic bunch compressor chicanes at free-electron lasers are excellent candidates for beam energy measurements. In the rectangular beamline sections of the bunch compressors at FLASH, energy beam position monitors (EBPM) with transversely mounted stripline pickups are installed. In this paper, we present the upgrade of the read-out electronics for signal detection of the EBPM installed at FLASH. The system is based on the MTCA.4 standard and reuses already available MTCA.4 compliant modules. This is also true for gateware and software development which fits into standard MTCA.4 framework development. The performance of the instrument was studied at FLASH during user operation and the results are presented.

INTRODUCTION TO THE MTCA.4

The MTCA.4 (Micro Telecommunication Computing Architecture – Enhancements for Rear I/O and Precision Timing) offers a compact environment for transmission and parallel processing of larger amounts of data. A general overview of the form factor and the standard is given in [1].

MTCA.4 Based Energy Beam Position Monitor

In this paper we present a system that uses the MTCA.4 platform for beam energy measurements by performing beam position measurements inside the dispersive section of the bunch compressor chicane. The development philosophy of the instrument follows the idea of having one common framework for the MTCA.4 based instrumentation the group at DESY is involved in. Among which the development of the LLRF for the XFEL is leading the effort (see [2]). Other systems that fall under the same umbrella are laser synchronisation (see [3]) related systems, bunch-arrival monitors, energy beam position monitors and others.

The first proof-of-principle of the EBPM instrument is presented in [4]. The proof-of-principle using the MTCA.4 environment is presented in [5]. In this paper the focus is in presenting the proposal for the final version that will be installed in the XFEL and tentatively at FLASH. FLASH is equipped with two EBPM pick-ups and XFEL will have 3 EBPM pick-ups that are being currently developed [6].

SYSTEM COMPONENTS

The infrastructure components are COTS available and have been tested at DESY and optimized by the corresponding vendors. The CPU is a CCT AM900 (www.gocct.com) i7 Intel 2 core CPU with 128G SSD discs. The MCH is a NAT-MCH-PHYS version of the Gen3 MCH manufactured by NAT and capable of connection over zone 3 to the rear side (www.nateurope.com). The power will be provided by a 600 W Telkoor (www.telkoor.com) AC power supply and the foreseen hosting chassis is the 2U Schroff crate (www.schroff.de). It is planned to use the SIS8300-L digitizer (www.struck.de) which hosts 5 dual channel 16 bit ADCs which can sample up to 125 MSPS. The digitizer is paired with the rear-transition module; a 10 channel down-converter DRTM-DWC10 developed at DESY and licenced by Struck Innovative Systeme. In order to be synchronized to the global machine timing the instrument will also need the X2 timer. Fig. 1 shows one such EBPM unit with only one digitizer.

Figure 1: The MTCA.4 based EBPM.

For proper operation of the system we also need a unit that will generate the sampling clocks and the local oscillator for down-conversion. This same unit will host also the required band-pass filters for proper pulse stretching as described in [5]. Fig. 2 shows the block diagram of the main system components.

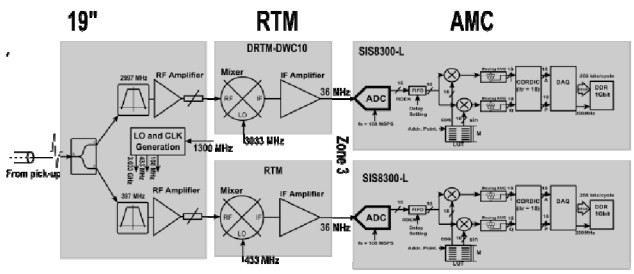

Figure 2: Main system components and their interconnections.

The external components will be placed in a 2U 19” rack mounted unit. There will be up to 5 m long cables that will interconnect the crate and the pick-ups.

PROCESSING OF THE SIGNALS

For the XFEL implementation it is foreseen to have detection at 2 frequencies (2997 MHz and 397 MHz) due to phase ambiguity that are related to the width of the chicane (see [5]). This will require using 2 pairs of SIS8300-L and DWC. One of the DWCs will be designed for detection at lower frequencies (397 MHz). Phase

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information of the main component is lost in case of direct sampling; therefore conversion to an intermediate frequency will be used also for the course/lower frequency channels.

The broadband pulses coming from the pick-ups are first split and fed into the low frequency and high frequency DWCs. Since each pick-up has 4 channels, there will be 4 channels used per DWC-digitizer pair. Each signal is then fed into a band-pass filter (2997 GHz and 397 MHz). The down-converted signal is then sampled. The processing algorithm in the FPGA is described in [5].

RF Front-End Design

The architecture of the external RF front-end unit depends on the expected levels and required resolution of the instrument. Fig. 3 shows the expected signal levels and noise levels at different points through the processing chain.

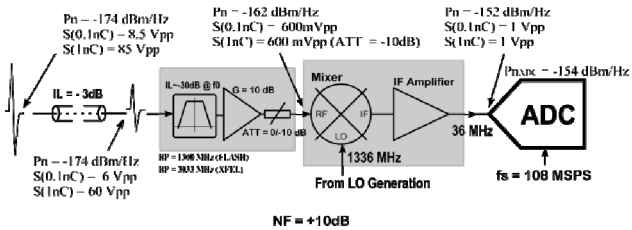

Figure 3: Signal and noise levels through the processing chain of the EBPM.

A signal path analysis shows the expected SNR at the ADC and if the presented layout is used the thermal noise from the RF front-end is noise matched to the noise power of the ADC. This allows the usage of a full specified ADC resolution. This can only be achieved if there is an amplifier after the band-pass filter. In order to keep same resolution at lower charges (100 pC) and at high charges (1 nC) there is a need for a variable attenuators in the chain.

Besides increasing the signal power, the SNR can be significantly improved also by averaging of multiple samples. The band-pass filter plays a crucial role in the SNR since it influences both; pulse amplitude and transient length. A simplified model of the system can be represented with Eq. 1 which shows that for best resolution the aim is to achieve best product between bandwidth and ringing time and maximize the integral of the impulse response of the band-pass filter.

$$SNR_{OUT} = SNR_{IN} \frac{f_{BW}}{f_{BWIN}} \cdot (f_{BW} t_r) \cdot \sum_{n=1}^{M} W[n] \quad (1)$$

Where SNR_{OUT} represents the output signal-to-noise ratio of the detected signal. SNR_{IN} is the input signal-to-noise ratio at the pick-up. The f_{BW} is the bandwidth of the filter and the f_{BWIN} is the input bandwidth of the signal before filtering. The t_r is the transient time. Since the product of the ringing time and the filter bandwidth is for a simplistic model constant, the only parameter that can influence the output signal-to-noise ratio is the integral of the impulse response of the filter $\sum_{n=1}^{M} W[n]$. Due to limitations in repetition rate (the filter should not have responses longer than the spacing between bunches) and noise floor (we can only take samples at a decent level above the noise floor) filters that maximize this integral within the bunch repetition rate are required.

CALIBRATION OF THE EBPM

The absolute calibration of the system was performed by using an OTR camera located by the chicane. After placing the beam position to the middle of the chicane (measured by the OTR camera) a correction factor for the EBPM was measured. After including this correction constant to the EBPM read-out the energy of the first accelerating module was scanned. The results of the measurements are shown in Fig. 4.

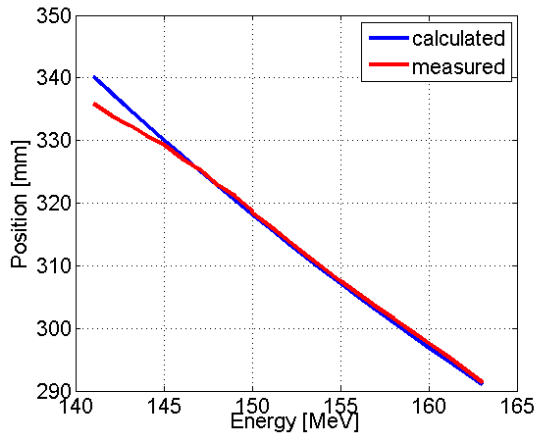

Figure 4: Scan of the beam energy results in position change in the chicane.

The calculated value is based on the formalism developed in [4]. It is not understood why the slope changes for energies lower than 145 MeV. The slope change is by a factor of 1.5.

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