PRECISION SYNCHRONIZATION OF OPTICAL LASERS BASED ON MTCA.4 ELECTRONICS*

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Abstract

Optical laser have become an integral part of free-electron laser facilities for the purposes of electron bunch generation, external seeding, diagnostics and pump-probe experiments. The ultra-short electron bunches demand a high timing stability and precision synchronization of the optical lasers. In this paper, we present the proof-of-principle for a laser locking application implemented on a MTCA.4 platform. The system design relies on existing MTCA.4 compliant off-the-shelf modules that are available on the market or have been developed for other applications within the particle accelerator community. Besides performance and cost, we also tried to minimize the number of out-of-crate components. Preliminary measurements of laser locking of a Yb-fiber laser, developed for electr-optical diagnostics, to an external RF source are presented, and an outlook for further system development in the area of laser-to-RF synchronization is given.

INTRODUCTION TO MTCA.4

The MTCA.4 (Micro Telecommunication Computing Architecture - Enhancements for Rear I/O and Precision Timing) offers a compact environment for transmission and parallel processing of larger amounts of data. The mechanics and connectivity is defined by the standard PICMG MTCA.4 specification [1, 2]. The basic architecture follows the idea of a centralized powerful processing unit that is connected to various AMC I/O boards over several PCIe lanes, gigabit ethernet links, dedicated trigger lines, SATA connections, clock lines and platform related management lines. The AMC backplane offers also 4 ports for low-latency-links connections (eight differential pairs, full-duplex) that can reach up to 10 Gbit/s in order to interconnect boards with fast serial interconnections (e.g. multi-gigabit transceivers). The MTCA.4 is defined as a redundant and highly reliable standard that uses IPMI (Intelligent Platform Management Interface) over I2C for system related management. The platform is managed by the MCH (MTCA Carrier Hub) which takes care of the crate management, PCIe lanes switching and generation of timing signals. In this paper, we present a compact MTCA.4 system for laser synchronization to an external RF source.

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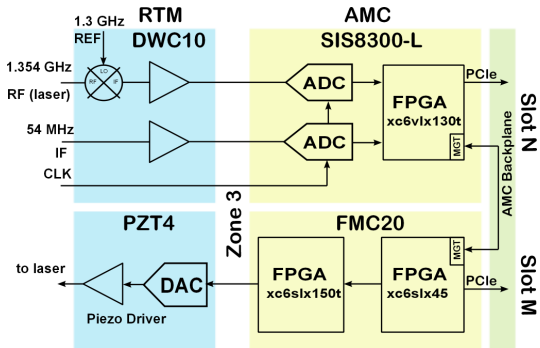

Figure 1: Block diagram of the MTCA.4 board setup.

BASIC CONCEPT AND SYSTEM COMPONENTS

Besides the basic crate infrastructure composed of MCH, CPU, power supply, AMC backplane and cooling, the laser-locking application comprises four boards in MTCA.4 standard that are used for processing analog and digital signals as is illustrated in Fig. 1. The laser pulses are translated to RF and processed accordingly in an external RF front-end 19" chassis. The output is then fed to the down-converter DRTM-DWC10 [3] that is placed as a rear-transition module (RTM) in the MTCA.4 crate. The signals are down-converted and the IF is transmitted via the Zone 3 connector to the AMC side of the crate where it is sampled by a 10-channel digitizer SIS8300-L [3]. The processing algorithm implemented in the FPGA is described in [4]. The processing includes I/Q detection of the sampled signals, amplitude and phase transformation, feedback controller and feed-forward table. In order to achieve suppression of eigen-modes of the piezo, a notch filter has been included. The output of the controller is routed to the DAC outputs on the digitizer (for monitoring purposes) and shipped over low-latency links on the AMC backplane to the neighboring AMC board DAMC-FMC20. The DAMC-FMC20 is a low-cost FMC carrier board which consists of two FPGAs. One FPGA is used for backplane interconnects (PCIe, multi-gigabit transceivers etc.), and the second FPGA is used for interconnecting with the rear-transition module (RTM) over the Zone 3 connector. The RTM module is a MTCA.4 compliant piezo driver called DRTM-PZT4 [5]. The output of the piezo driver is directly connected to the piezo of the laser.

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Ytterbium-Fiber Laser

The Yb-fiber laser was developed at the Paul-Scherrer-Institute PSI for electro-optical bunch length measurements [6] and will also be used at the European XFEL. The entire laser is housed in a 19" chassis with 6 height units. It delivers 1 nJ pulses at a wavelength of 1030 nm with a repetition rate of 54 MHz. The laser consists of a ring oscillator with a fiber and a free space part as is illustrated in Fig. 2. The amplification and pumping is done in fiber while the free space part is necessary for dispersion compensation and the mode locking mechanism, which is based on nonlinear polarization evolution. A piezo stretcher modulates the resonator length and therewith the repetition rate, which is used to synchronize the laser to an external reference RF signal. A motorized stage in the grating compressor can be used for coarse repetition rate tuning. A 10 mW optical monitor signal is split into a fiber to the RF front-end for the laser locking.

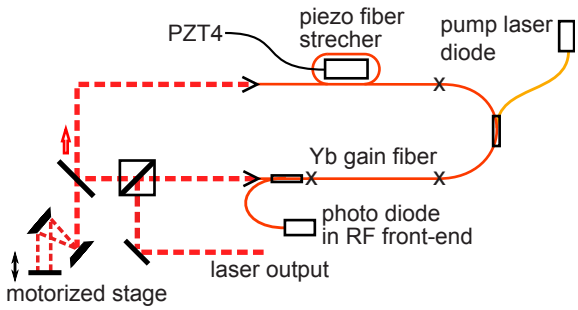

Figure 2: Simplified schematic of the Yb-fiber laser.

RF Front-End

The RF front-end 19" chassis is used as an interface unit between the photodiode signal generated from the laser pulses and the MTCA.4 based electronics developed originally for low-level RF (LLRF) applications [7]. The RF front-end uses a novel approach for signal detection where instead of generating an extra LO signal (RF + IF), we use the generally available reference signal at 1.3 GHz as the LO input. The RF input at 1354 MHz, which is the 25th harmonic of the laser repetition rate, is generated with the help of a fast photodiode signal and a bandpass filter. The basic concept of the RF front-end is depicted in Fig. 3. The down-conversion from 1354 MHz to 54 MHz is done using the MTCA.4 compliant down-converter DRTM-DWC10 (see [2]). Activities have started for unifying the 19" RF front-end and DRTM-DWC10 module into a single RTM board. A proof-of-principle set-up with PCB mounted components has been realized and been used for measurements presented in this paper.

Digitizer SIS8300-L

The digitizer SIS8300-L [3] is a MTCA.4 compliant AMC module designed for the LLRF systems [7] of the accelerators of the FLASH and European XFEL facilities at

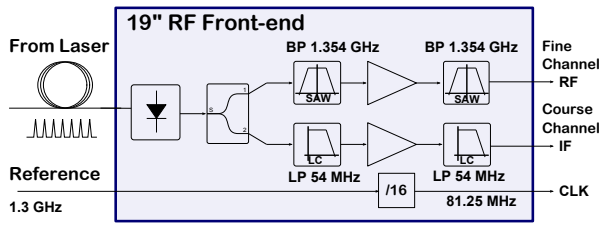

Figure 3: : Block diagram of the RF front-end 19" chassis.

DESY. It consists of 5 dual 16 bit ADCs that sample up to 125 MSPS. All the signals on the digitizer are differentially routed from the Zone 3 connector to the ADCs. The board uses a Virtex-6 XC6VLX130T FPGA for data processing and interconnections. The front panel allows for connections via SFP modules and feeding of external CLKs (both not used in this application). The sampling CLK for the ADCs is generated directly from the 1.3 GHz LO reference with a divider and routed through the DRTM-DWC10 to the ADCs (see Fig. 3).

PZT4 Piezo Driver and FMC20 FMC Carrier

The DAMC-FMC20 is a general purpose FPGA Mezzanine Card (FMC) carrier board compliant to the MTCA.4 standard. The design is based on two Xilinx FPGAs: One Spartan-6 XC6SLX150 manages the FMC and RTM functionality and one Spartan-6 XC6SLX45T works as a PCIe and Gigabit Link bridge. The AMC ports 12-15 are connected to a cross point switch for flexible routing of interconnection between different AMC cards. Figure 4 shows a picture of the MTCA.4 compliant piezo driver RTM module PZT4 [5, 2] is equipped with 4 power amplifiers supplied from internal DC/DC converters (0V÷100V, -100V÷100V). The software programmable span DACs (500 kSPS) have been applied to fulfil all demanded control signal ranges: ±5V, ±10V, 0V÷5V, 0V÷10V. Each power amplifier gain has been fixed to 10 V/V. The RTM module can drive up to four parallel piezos with capacitances of up to 10 μF.

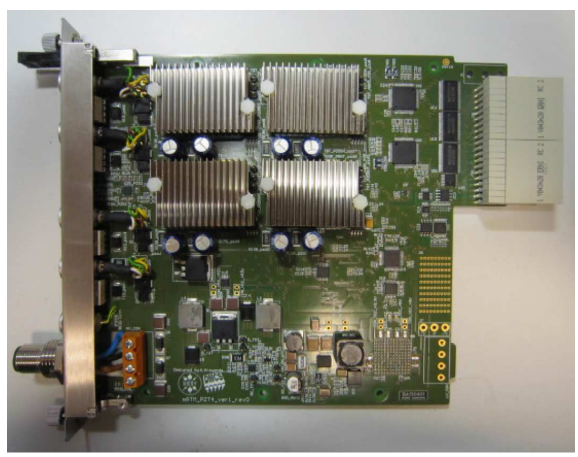

Figure 4: Photograph of the DRTM-PZT4 4-channel piezo driver board.

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Application Server

A dedicated DOOCS server, written as C++ software, has been prepared for users to provide direct communication over the FPGA firmware. The server manages via PCIe a set of registers implemented in the FPGA which control and monitor the feedback loop. Additionally, it implements high-level features such as long-term measurements of phase error, controller input/output and exception handling logic. The piezo element can compensate the laser drifts only in a limited range, thus, a laser coarse tuning with temperature or stepper motors has been implemented.

MEASUREMENT RESULTS

The design allows to check intermediate signal processing in the FPGA. Figure 5 shows a plot of the I and Q detected signals when the feedback loop is unlocked (dotted lines) or locked (solid lines). The beat note corresponds to the frequency offset between the 1.3 GHz LO reference and the corresponding laser frequency. Monitoring points are placed also after the CORDIC [8] algorithm. The feedback acts on the phase component only. The amplitude component is accessible for monitoring.

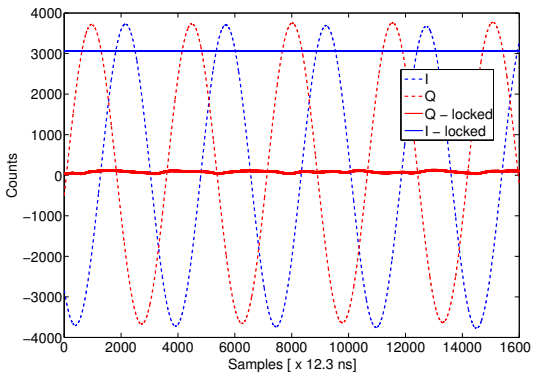

Figure 5: I and Q detected in the digitizer SIS8300-L board.

Phase Noise Performance

The performance of the laser lock is given by the phase noise of the locked laser at the locking frequency. For the measurements, all components, i.e. the Yb-fiber laser, RF front-end and MTCA.4 crate, were placed in the same rack. Figure 6 shows the phase noise of the 1.3 GHz LO reference signal, free-running laser and locked laser.

The measurements show that the system is capable of achieving a good lock up to 100 Hz. There is a stronger peak at 500 Hz which exhibits a correlation to the fans in the MTCA.4 crate and is not fully reduced by the locking system. The measured phase noise of the free-running laser lies above the reference phase noise at all frequencies which can be attributed to a poor performance of the photodiode for frequencies above 10 kHz. We have observed spurious lines at higher frequencies ($\sim$ 200 kHz) which are coupled to the piezo connection. Since the piezo has an internal low-pass filter at 100 kHz we are assuming that these

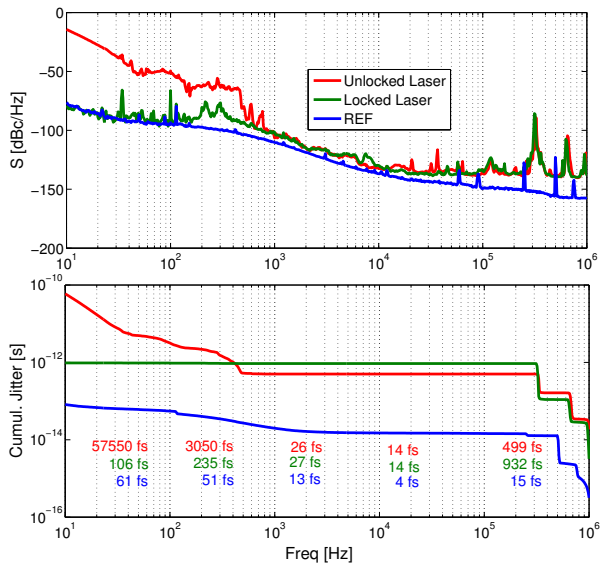

Figure 6: Phase noise (top) and integrated timing jitter (bottom) of the 1.3 GHz reference (blue), free-running laser (red) and locked laser (green). The numbers in the lower plot represent the timing jitter per frequency decade.

lines are caused by EMI interferences propagating over the ground.

CONCLUSION

Synchronization of a laser to an external RF source has been demonstrated for an ultra compact system based on commercially available MTCA.4 components. All system components, i.e. laser, RF front-end and MTCA.4 crate, were placed in one 19" rack. The preliminary results of this proof-of-principle all-MTCA.4-based laser synchronization system demonstrate the successful locking of a laser but show also that further investigations on the phase noise response are required to reach a desired sub-50 fs timing jitter. The RF front-end will be reduced to a compliant form factor after careful investigation in the near future.

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