THE DESIGN STRATEGY OF ORBIT FEEDBACK SYSTEM IN THE TPS

C.H. Kuo, P.C. Chiu, C. Y. Wu, Y. S. Cheng, K. H. Hu, J. Chen, K.T. Hsu
NSRRC, Hsinchu 30076, Taiwan

Abstract

TPS (Taiwan Photon Source) is a 3 GeV synchrotron light source which is being constructed at NSRRC. The BPM electronic is based on micro-TCA platform and used for various requests and function reasons. The orbit feedback system design is based on open structure, modularization and highly integration. There are many advantages that orbit feedback system is embedded in the BPM crate with FPGA modules. High throughput backplane, data transfer and processing support rich function for waveform record, diagnostic, beam study and transient analysis. The design and implementation result of the system will be reported in this conference.

INTRODUCTION

The TPS [1] is a latest generation of high brightness synchrotron light source which has been under construction at the National Synchrotron Radiation Research Center (NSRRC) in Taiwan since 2010. It consists of a 150 MeV electron Linac, a 3 GeV booster synchrotron, and a 3 GeV storage ring. The design of the storage ring has 24 cells. There are 7 BPMs and 7 horizontal/vertical correctors are winding on the sextupoles in each cell. Current generation state of the art BPM electronics is designed and delivered more than 5 years ago. To avoid obsolesce of the components, to take advantages of advanced devices and enhance functionality, it was decided to adopt new design of BPM electronics. To satisfy stringent orbit stability requirement of the TPS, low noise corrector power supply system, and orbit feedback system are also designed.

The design of the storage ring has 24 cells, each cell equipped with 7 BPMs and 7 horizontal/vertical correctors are winding on the sextupoles in each cell. The lattice layout is as Fig.1. The locations of BPM and correctors are to satisfy DC orbit correction under the constraint of installation space. Since vertical beam size at centre of straight section for insertion devices is around 5 μm in sigma, better than 0.5 μm beam stability are required. To meet the tight orbit stability requirement, an orbit feedback system is indispensable. Standard correctors are winding on the sextupole magnets. These kinds of correctors could provide about 600 μrad kick while their bandwidth could be limited only several tens of Hertz due to the eddy effect of the alumina vacuum chamber. The vacuum chamber is 4 mm thick elliptical chamber with 30 mm and 60 mm in minor axis and major axis respectively. Due to eddy current effect, the possible bandwidth in horizontal and vertical plan is around several tens of Hertz. This bandwidth is not sufficient to eliminate perturbation below 100~200 Hz. Therefore, extra four horizontal/vertical correctors per cell will be installed on the bellows site as to obtain higher correction bandwidth. These correctors have fast response but smaller kick strength around 30 μrad. Thus the orbit feedback system is planned to use two kinds of correctors simultaneously. The DC component of the fast correctors will be transferred from fast to slow correctors smoothly and avoid saturation of the fast correctors as well as provide capability to suppress orbit drift.

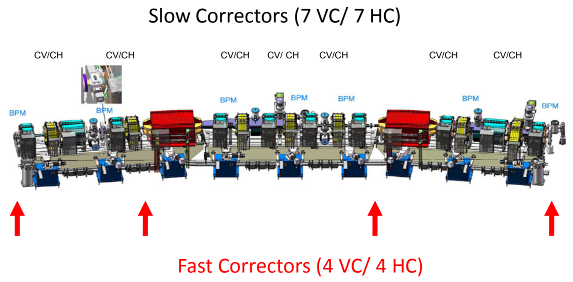

Figure 1: The slow (winding on sextupoles) and fast correctors layout in one cell of TPS storage ring. One cell of 24 double-bend cells for TPS lattice layout.

BPM SYSTEM

BPM Electronics

The TPS BPM electronics was contracted to the Instrumentation Technologies in May 2011 for the Libera Brilliance+ as BPM electronics which is the latest member of the Libera family [2]. The family covers the various requirements and adopted by many modern synchrotron light source. The Libera Brilliance+ delivers unprecedented possibilities for either building powerful single station solutions or architecting complex feedback systems. New electronics allows even more extensive machine physics studies to be conducted due to large data buffers and the new true turn-by-turn position calculation. The instrument also possesses a useful feature which provides two approaches to process from ADC data to turn-by-turn data. One is classic DDC approach; another is time domain processing (TDP). This functionality is useful for peculiar filling pattern.

There are 168 BPM units at the storage ring except some special BPM at straight sections. All 168 BPM electronic modules will be installed at 48 BPM platforms. The first field tests of the new product had been performed on real beam at Taiwan Light Source (TLS) [3, 4] to test validation for the usage for the TPS. Fig. 2 shows the tested installation.

Intensive test for performance and functionality were performed for the prototype to ensure that the new electronics satisfy the requirement of TPS. The test

ISBN 978-3-95450-127-4

combined by using simulated signals from signal generator. The long-term stability has been tested for bench measurement where input power level was set to several power level between -20 dBm and 0 dBm. Position stability is around 100 nm in rms for both planes during one day record. The temperature dependence has also been tested and almost could be ignored while ambient temperature was controlled within ± 0.1˚C. The resolution of FA data at 10 kHz meet specification where σ x and σ y is less than 150 nm. Besides, turn-by-turn data has been achieved 10 μm resolutions for short bunch train.

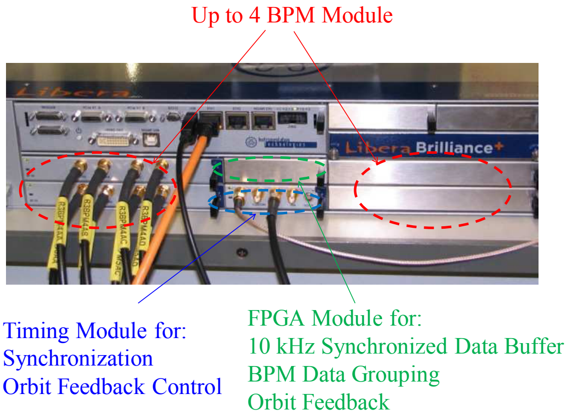

Figure 2: Libera Brilliance+ installation.

For turn-by-turn data, the resolutions are 150 um for 0.5 mA and 10 um for 10 mA respectively. FA data resolution is around 100 nm for 100 mA.

The filling pattern and temperature dependency are also verified. Current dependency is less than 200 nm for 40 dB input power level changes. Different camshaft mode filling patterns are tested to observe position almost not changed (<<100nm). Additionally, temperature dependency are smaller than 100 nm/˚C [5].

BPM Data Access and Grouping

There are several data format flows are provided by the BPM platforms with EPICS interface including of 10 Hz rate data for DC closed orbit correction, turn-by-turn data with software/hardware trigger and on demand access for accelerator physics study, streaming 10 kHz fast data for orbit feedback application. The fast data is also very useful for beam diagnostic.

The BPM platform is composed of a COM Express CPU module running Linux to control up to 4 BPM modules. Embedded EPICS server on this module could deliver 10 Hz rate access of BPM information, includes matrix elements of the orbit feedback system as well as handle the basic configuration.

A FPGA module will be installed at the BPM platform to support 10 kHz synchronized data buffer for 4 BPM modules, and grouped with the other BPM platforms for the whole storage ring together. The fast orbit feedback control and fast corrector interface protocol are also processed in this module. There are four SFP ports on the front panel. There are several LVDS links in the BPM modules that can collect all ring BPM data with 10 kHz rate. The data is through the bi-directional multi-gigabit links to the adjacent nodes. Each FPGA module will serve as one node of the BPM grouping around the ring. We refer to this functionality as BPM grouping. The communication of the grouping is done by two SFP ports. The bitrate of the grouping can be up to 6.25 Gbit/sec. One of the remained SFP port will be used as fast corrector control interface with AURORA protocol. The last SFP port will provide functionality for grouping data output either use AURORA protocol or UDP/IP protocol, to support the slow corrector control or the diagnostic related application. The Ethernet packet supports jumbo frame to satisfy all BPM data grouping. Due to BPM data grouping and orbit feedback control using the same FPGA module, orbit feedback is also a part of BPM platform.

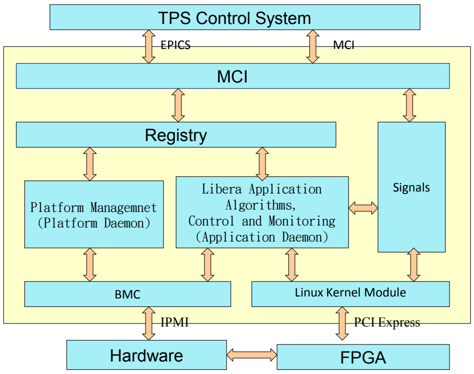

Figure 3: BPM platform software structure.

BPM Platform Software Structure

BPM platform software is organized in a few layers as Fig. 3. In the bottom layer there are BMC library and Linux kernel module which communicate with FPGA and hardware through IPMI (Intelligent Platform Management Interface) and PCI Express respectively. On the top of that there is signal processing library and the application daemon for control and monitor algorithms processing. Besides application, there is also platform management (Platform Daemon), which is responsible for monitoring health status of the hardware. The application and platform daemon communicate with outer world through the MCI (measurement and control interface) which uses registry and signal library underneath for accessing application properties, signals, changing the application behavior, etc.

CORRECTOR POWER SUPPLY CONTROLS

The power supply for both fast and slow corrector magnets are in the range of ±10 Amp corresponding to +/- 30 μrad and 600 μrad maximum kick angle respectively. These power supplies will be controlled by analogue interface directly. The CPSC is dedicated to be designed for both EPICS control system and fast orbit feedback application which is based on AURORA of Xilinx to support high speed settings required for fast feedback.

There will be 8 power supply modules in one crate and the center slot will be plugged in one CPSC. Besides general control, monitor and configuration, the fast correctors will be also applied for the fast orbit feedback. The CPSC with EPICS IOC is therefore dedicatedly designed and the embedded FPGA will handle fast update application. Built-in waveform and synchronization mechanism are also supported. Fig. 4 shows the corrector power supply crate which includes 8 power supply modules and one CPSC at the middle slot. The setting reference of the corrector power supply is generated by 20 bits DAC and readback is from 24 bits ADC. This controller is also embedded EPICS IOC for slow control. Fast setting ports are to receive fast data from orbit feedback FPGA module in BPM platform [7].

Figure 4: Corrector power supply crate. There are 8 power supply regulation modules in one crate and the most left slot will be plugged in one CPSC.

ORBIT FEEDBACK INFRASTRUCTURE

The TPS aluminium vacuum chamber of storage ring is 4 mm thickness that prevents fast orbit correction by standard correctors in both planes which are back winding on 168 sextupole magnets. In order to satisfy fast orbit feedback request, 96 sets of fast corrector at bellows site are added. So, the TPS orbit feedback system is a global orbit feedback system combined fast and slow corrector in one system. Similar implementation were adopted in several facilities [9, 10]

The infrastructure configuration of orbit feedback with fast and slow corrector is shown in Fig. 5. There are 24 cells in the TPS storage ring. Each cell will be equipped with two BPM platforms, include of 7 BPM modules. Each BPM platforms has a slot which can allocate an FPGA module used for communication with the other module in other cells as a clockwise and counter-clockwise multi-gigabit redundancy link to group BPM data for the whole ring. Two FPGA modules of each cell will handle fast orbit feedback control algorithm and control 4 fast correctors in horizontal and vertical plane respectively. Correctors are controlled by a custom designed Corrector Power Supply Controller (CPSC) of each cell [6, 7, 8]. The CPSC module will be installed at the middle slot of power supply crate to control up to 8 modules in the same chassis. At each cell, there are three CPSC modules installed at three power supply crates include of horizontal slow correctors (7 PS modules), vertical slow correctors (7 PS modules), and combined horizontal (4) and vertical (4) fast corrector as Fig. 6 shown.

Besides fast correctors computation executed in FPGA modules, the slow corrector control will be handled from general console via EPICS channel access channel keep away from fast corrector saturation.

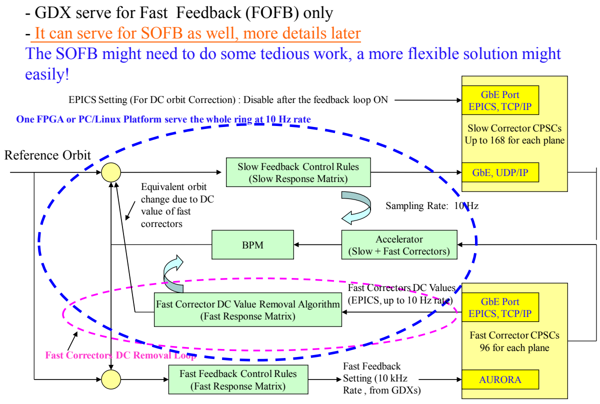

Figure 5: Control infrastructure in one cell of TPS storage ring power supplies.

INTEGRATION BETWEEN FAST AND SLOW ORBIT FEEDBACK

Aluminum vacuum chamber of TPS would prevent fast magnet field penetration. So, two kinds of corrector were designed to stabilize orbit motion from DC to 250 Hz. Slow correctors are winding on sextupole magnets for DC orbit correction and slow orbit compensation. The slow corrector has slow response with high kick angle. The fast correctors installed at bellow sites have fast response with small kick angle. The fast feedback system has capability to suppress fast transient disturbance, but corrector is easily satisfied. Integration of two kind loops will keep from fast corrector extinguishment when meet with large field leakage in the insertion device action.

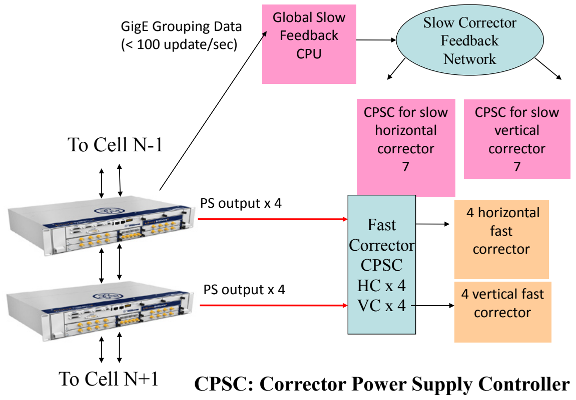

Figure 6: Configuration of global orbit feedback for corrector power supply.

The fast orbit feedback loop will be performed in the FPGA modules in the distributed manner; each FPGA module control four fast correctors. The matrix elements download and feedback parameters will be done by the EPICS IOC located at the platform of the FPGA module. All feedback loop of platform will be synchronized by grouping and external signal, such as feedback on/off. The relation interface FPGA modules are shown in the Fig. 7.

The slow orbit feedback loop processing will use PC running Linux. The general computer can be implemented rich control algorithms in the feedback loop that will enhance system stability. The individual BPM and fast corrector setting value in each cell will be combined in the local net, and concentrated to a waveform type data of EPICS interface to satisfy software real-time access request for slow orbit feedback control. The CPSC is also EPICS IOC that will receive slow setting value from typical EPICS interface. Each CPSC module would extract their setting data by specific address within the packet.

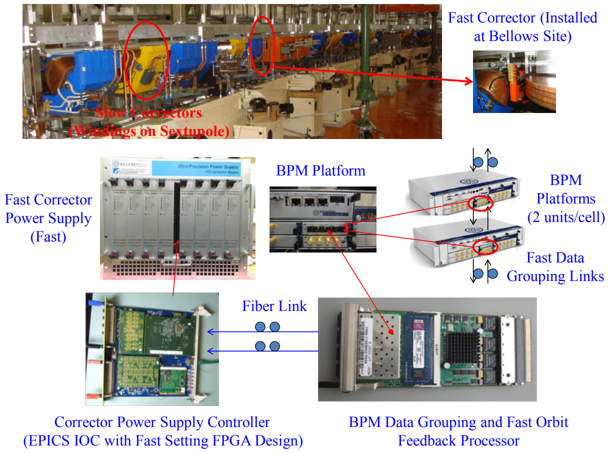

Figure 7: Relationship between major components of the orbit control in one lattice cell.

There are two solutions implemented to deal with orbit feedback. The first solution is to combine fast and slow orbit feedback system together and communicate both loops to prevent interference each other. The second solution is that the fast orbit feedback covers frequency range from DC to 250 Hz. The DC value on the fast corrector will remove to nearby slow corrector by add fast corrector setting information in the slow loop to prevent saturation of the fast correctors.

Concept of the combine fast and slow feedback loops are shown in the Fig. 8. There are two options in the slow feedback loop. Option 1 don't need two response matrix operation, simple processing and avoid unstable probability, but slow corrector selection must be closed to fast corrector. Option 2 is inversed to option 1, but flexible corrector can be selected. In the same time, must be developed robust control to keep system stable. However, corrections for both loops are updated simultaneously.

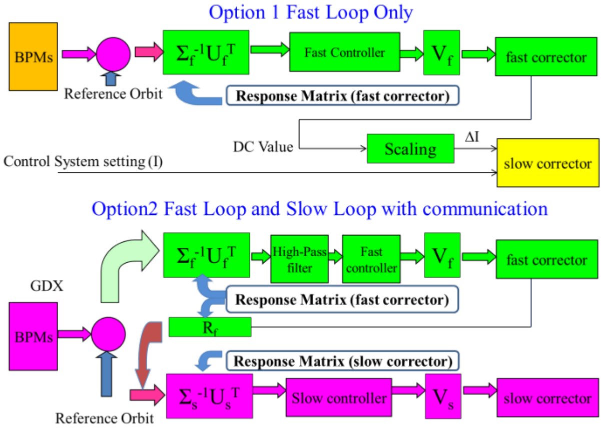

Figure 8: Feedback loop block diagram with slow and fast channel.

SUMMARY

BPM system and corrector power supply control system are ready for installation. Integration test for both systems will be possible in the 2nd or 3th quarter of 2014. Orbit feedback code were development and to do preliminary test. Test with beam can be proceeding in early phase of commissioning. Short deploy is foreseeable.

REFERENCES

[1] http://www.nsrrc.org.tw/english/tps.aspx.
[2] http://www.i-tech.si.
[3] P. Leban, et al., "First Measurements of a New Beam Position Processor on Real Beam at Taiwan Light Source", Proceedings of the PAC 2011, New York, U.S., 2011.
[4] C. H. Kuo, et al., "Preliminary BPM Electronic Testing for the Taiwan Photon Source Project ", Proceedings of the IPAC 2011, San Sebastian, Spain, 2011.
[5] P. C. Chiu, et al., "TPS BPM Electronics Performance Measurement and Statistics" Proceedings of IBIC2012, Tsukuba, Japan.
[6] Specification of the Corrector Power Supply Controller for TPS project. 2010.
[7] P. C. Chiu, et al., "Fast Orbit feedback Scheme and Implementation for Taiwan Photon Source", Proceedings of IPAC2013, Tsukuba, Japan.
[8] http://www.D-Tacq.com.
[9] C. Steier, et al., "Operational Experience Integrating Slow and Fast Orbit Feedbacks at the ALS", Proceedings of EPAC 2004, Lucerne, Switzerland.
[10] N. Hubert, et al., "Commissioning of Soleil Fast Orbit Feedback System", Proceedings of EPAC08, Genoa, Italy.